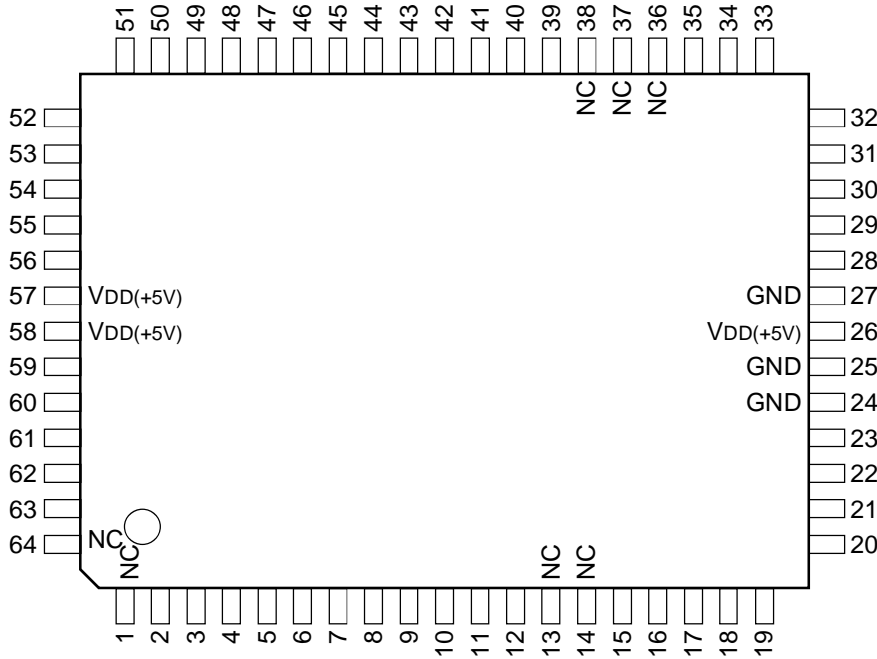
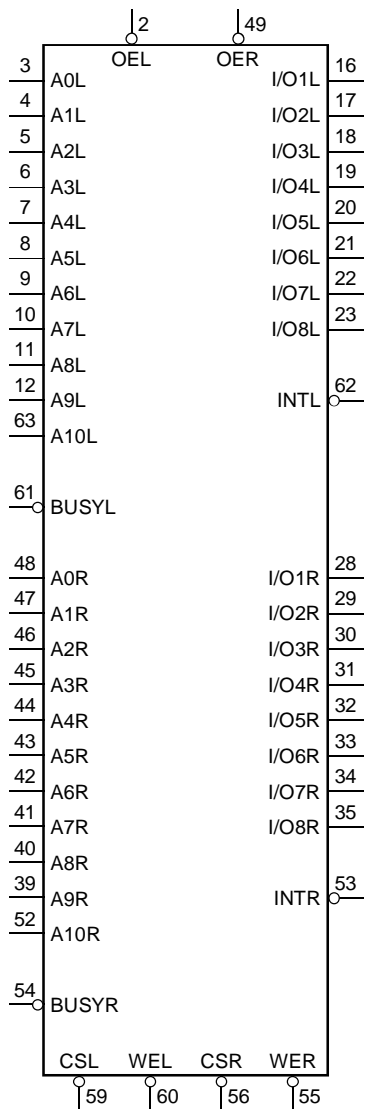

C-MOS 64K-BIT DUAL PORT STATIC RAM
-TOP VIEW-



(VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	A12L	17	I/O	I/O2L	33	I/O	I/O6R	49	I	$\overline{\text{OER}}$
2	I	OEL	18	I/O	I/O3L	34	I/O	I/O7R	50	I	A12R
3	I	A0L	19	I/O	I/O4L	35	I/O	I/O8R	51	I	A11R
4	I	A1L	20	I/O	I/O5L	36	—	NC	52	I	A10R
5	I	A2L	21	I/O	I/O6L	37	—	NC	53	O	$\overline{\text{INTR}}$
6	I	A3L	22	I/O	I/O7L	38	—	NC	54	I	$\overline{\text{BUSYR}}$
7	I	A4L	23	I/O	I/O8L	39	I	A9R	55	I	$\overline{\text{WER}}$
8	I	A5L	24	—	GND	40	I	A8R	56	I	$\overline{\text{CSR}}$
9	I	A6L	25	—	GND	41	I	A7R	57	—	VDD
10	I	A7L	26	—	VDD	42	I	A6R	58	—	VDD
11	I	A8L	27	—	GND	43	I	A5R	59	I	$\overline{\text{CSL}}$
12	I	A9L	28	I/O	I/O1R	44	I	A4R	60	I	$\overline{\text{WEL}}$
13	—	NC	29	I/O	I/O2R	45	I	A3R	61	I	$\overline{\text{BUSYL}}$
14	—	NC	30	I/O	I/O3R	46	I	A2R	62	O	$\overline{\text{INTL}}$
15	O	$\overline{\text{BE}}$	31	I/O	I/O4R	47	I	A1R	63	I	A10L
16	I/O	I/O1L	32	I/O	I/O5R	48	I	A0R	64	I	A11L



A0L - A10L,
 A0R - A10R ; ADDRESS INPUTS
 \overline{BE} ; BUSY OUTPUT ENABLE
 \overline{BUSYL} , \overline{BUSYR} ; BUSY INPUTS
 \overline{CSL} , \overline{CSR} ; CHIP SELECT INPUTS
 I/O0L - I/O10L,
 I/O0R - I/O10R ; DATA INPUTS/OUTPUTS
 \overline{INTL} , \overline{INTR} ; INTERRUPT OUTPUTS
 \overline{OEL} , \overline{OER} ; OUTPUT ENABLE INPUTS
 \overline{WEL} , \overline{WER} ; WRITE ENABLE INPUTS

