

August 1998

54ABT541

Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541 is similar to the 'ABT244 with broadside pinout.

Features

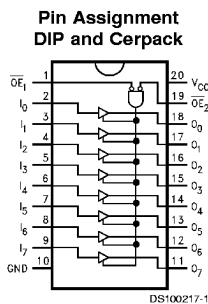
- Non-inverting buffers
- Output sink capability of 48 mA, source capability of 24 mA

- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Flow-through pinout for ease of PC board layout
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9471801

Ordering Code

Military	Package Number	Package Description
54ABT541J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT541W-QML	W20A	20-Lead Cerpack
54ABT541E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagram

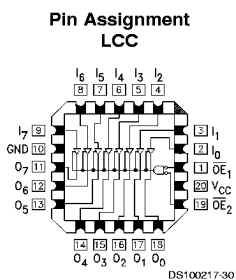


Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active Low)
I_0-I_7	Inputs
O_0-O_7	Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	ABT541
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

© 1998 National Semiconductor Corporation DS100217

www.national.com

54ABT541 Octal Buffer/Line Driver with TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V _{CC}
Current Applied to Output	

in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT541			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = −3 mA
		54ABT	2.0		V	Min	I _{OH} = −24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4)
			5				V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		−5		μA	Max	V _{IN} = 0.5V (Note 4)
			−5				V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current		50		μA	0 – 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I _{OZL}	Output Leakage Current		−50		μA	0 – 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I _{OS}	Output Short-Circuit Current	−100	−275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current		50		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		30		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		50		μA	Max	$\overline{OE}_n$ = V _{CC} ; All Others at V _{CC} or Ground
I _{CC} T	Additional I _{CC} /Input	Outputs Enabled	2.5		mA	Max	V _I = V _{CC} − 2.1V
		Outputs TRI-STATE	2.5		mA		Enable Input V _I = V _{CC} − 2.1V
		Outputs TRI-STATE	50		μA		Data Input V _I = V _{CC} − 2.1V; All Others at V _{CC} or Ground
I _{CCD}	Dynamic I _{CC}	No Load		0.1	mA/ MHz	Max	Outputs Open, $\overline{OE}_n$ = GND, One Bit Toggling (Note 3), 50% Duty Cycle

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.0	V	5.0	T _A = 25°C (Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-1.45	V	5.0	T _A = 25°C (Note 5)

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF		
		Min	Max	
t _{PLH}	Propagation Delay	1.0	5.0	ns
t _{PHL}	Data to Outputs	1.0	5.3	
t _{PZH}	Output Enable Time	1.1	7.2	ns
t _{PZL}		1.5	7.9	
t _{PHZ}	Output Disable Time	1.5	7.5	ns
t _{PLZ}		1.5	7.9	

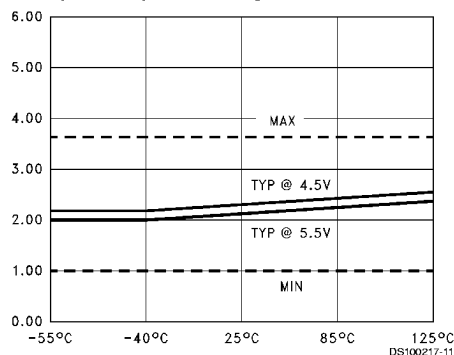
Capacitance

Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0.0V
C _{OUT} (Note 6)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

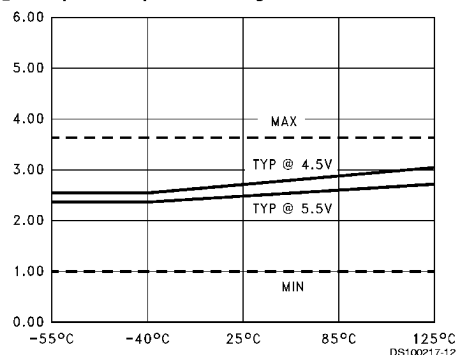
Note 6: C_{OUT} is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

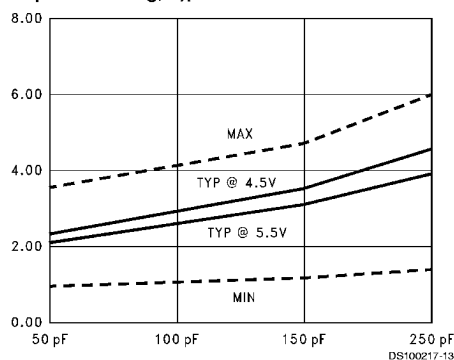
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



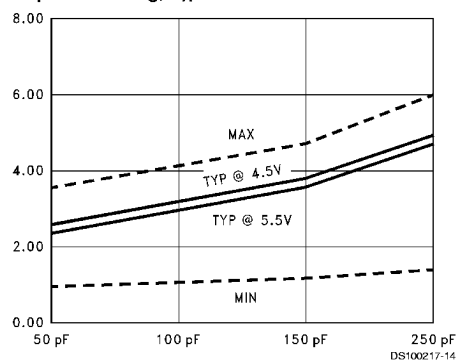
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



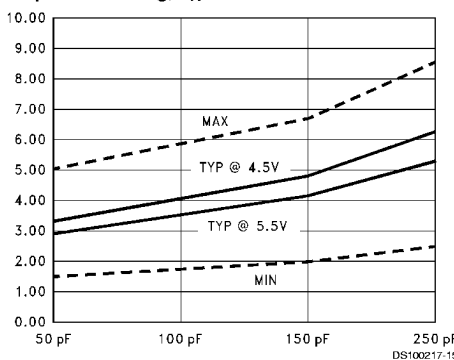
t_{PLH} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$



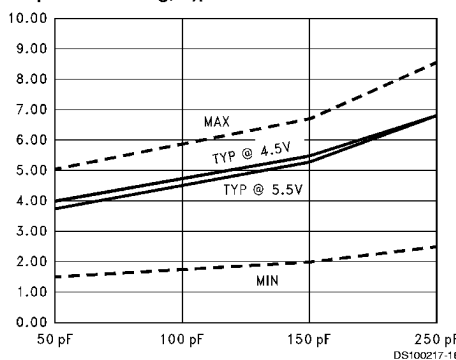
t_{PHL} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$



t_{PLH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$



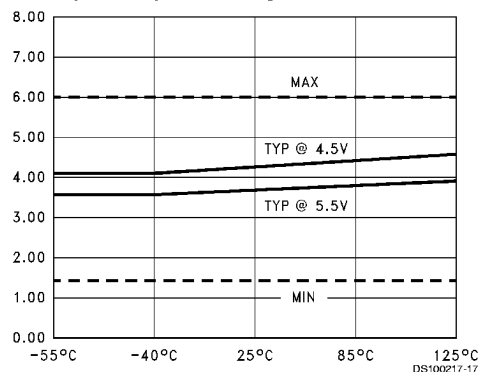
t_{PHL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$



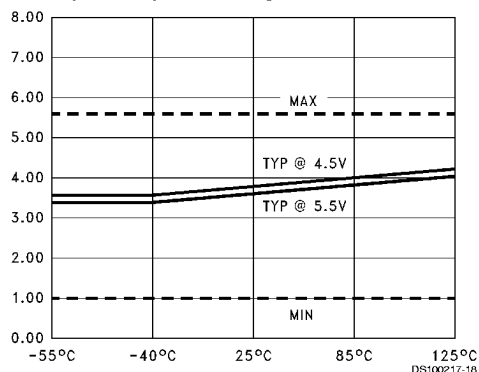
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Capacitance (Continued)

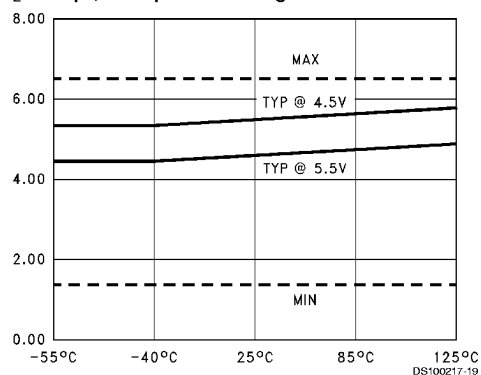
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



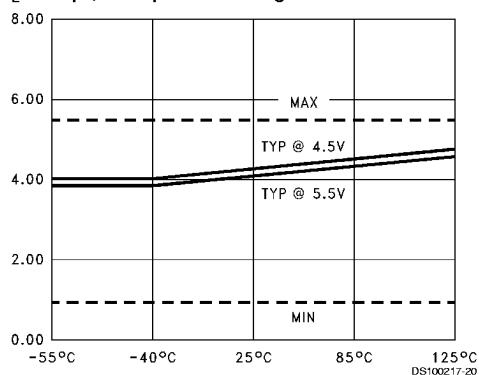
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



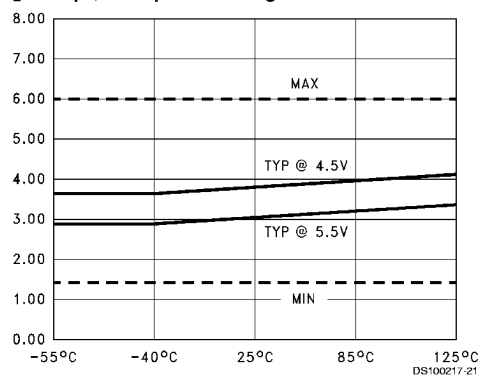
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



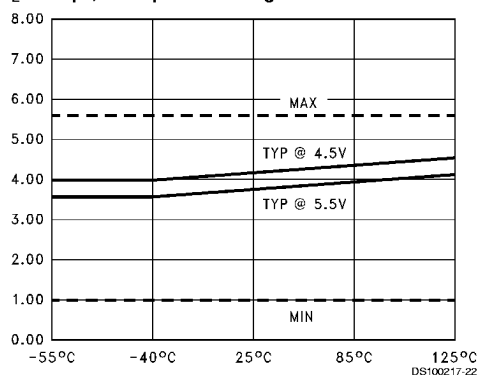
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



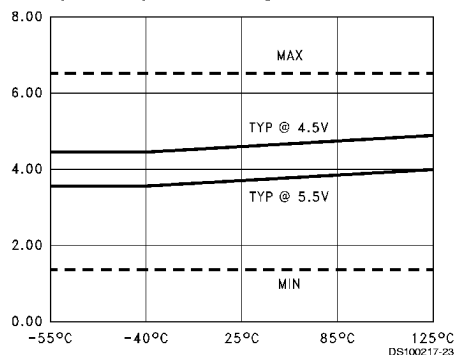
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



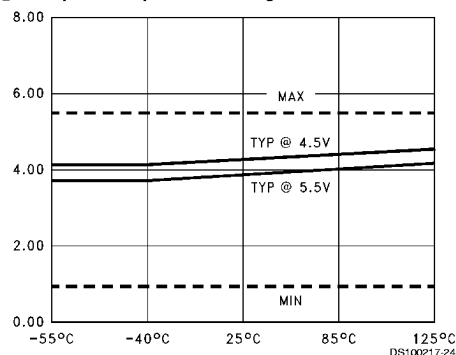
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Capacitance (Continued)

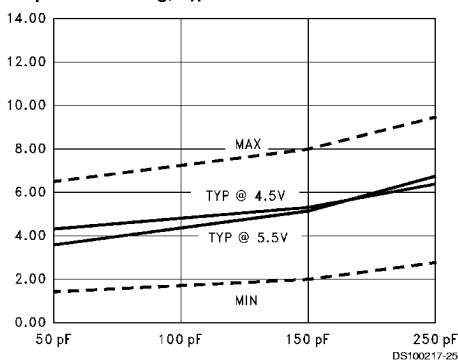
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



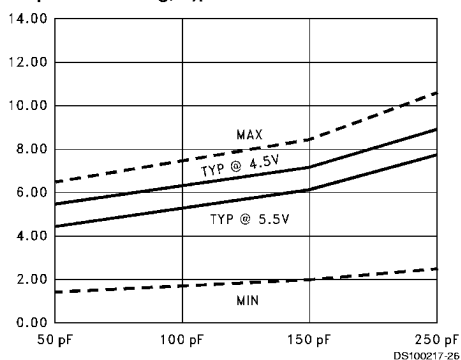
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



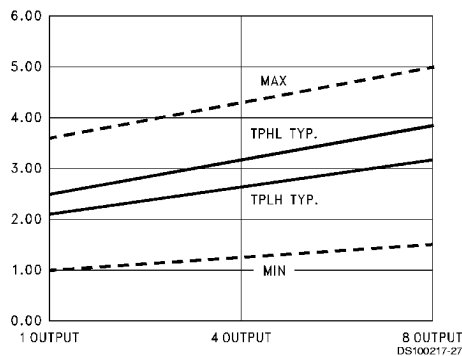
t_{PZH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$



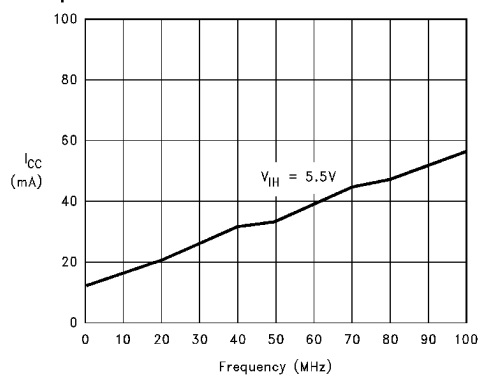
t_{PZL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$



t_{PLH} and t_{PHL} vs Number Outputs Switching
 $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 50$ pF

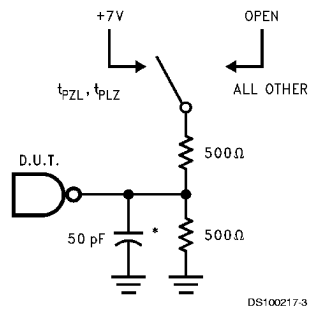


I_{CC} vs Frequency,
 Average, $T_A = 25^\circ\text{C}$,
 All Outputs Unloaded/Unterminated



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

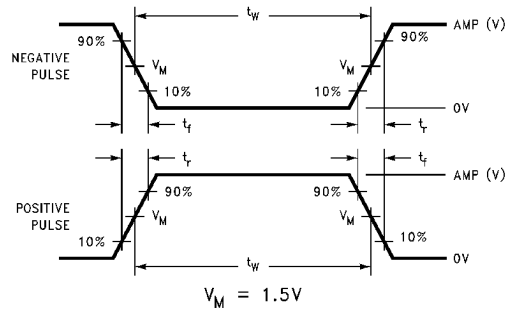


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

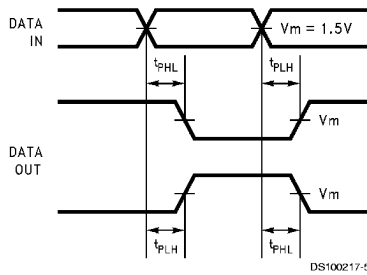


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

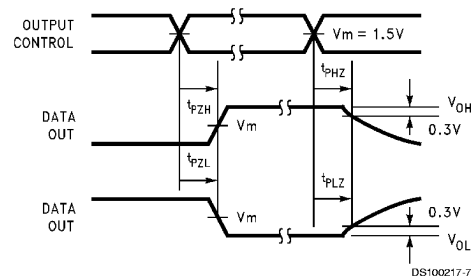
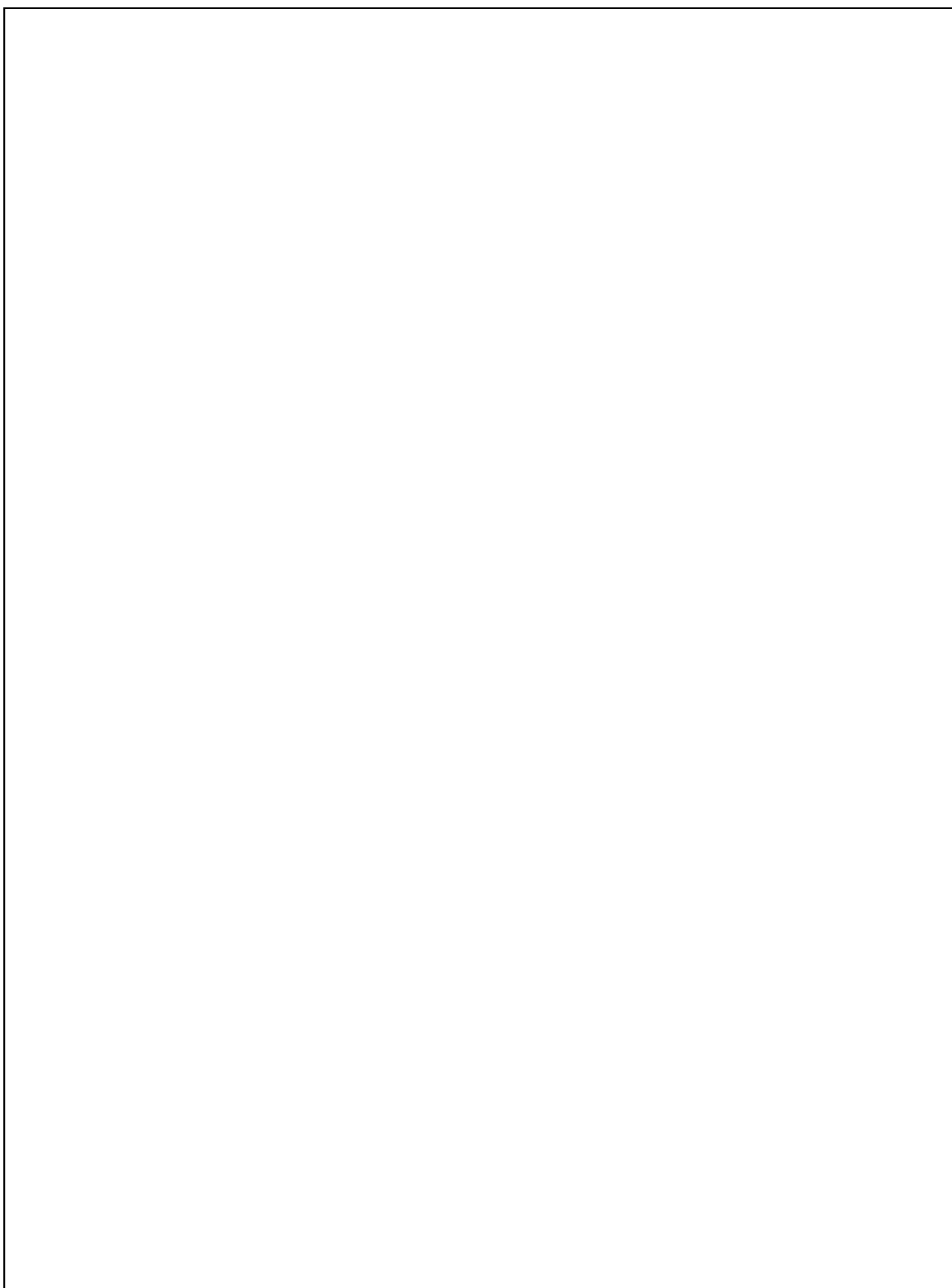
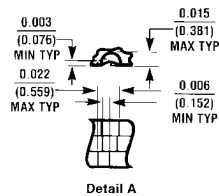
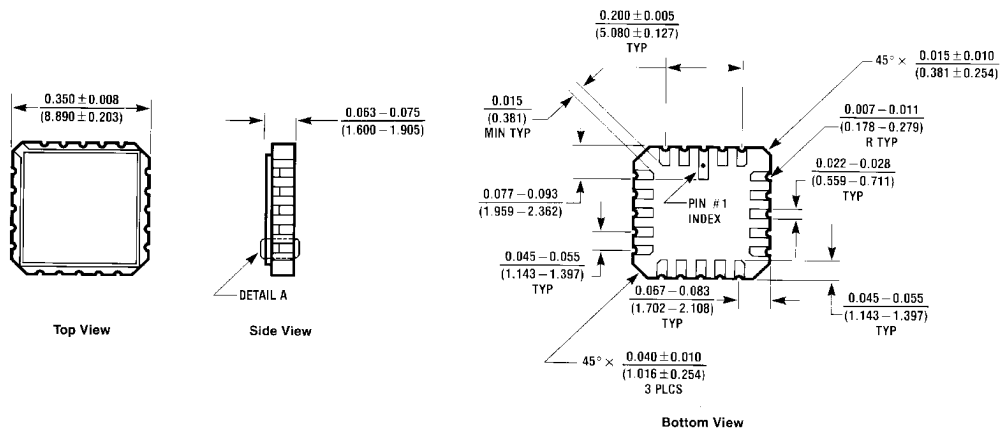


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time

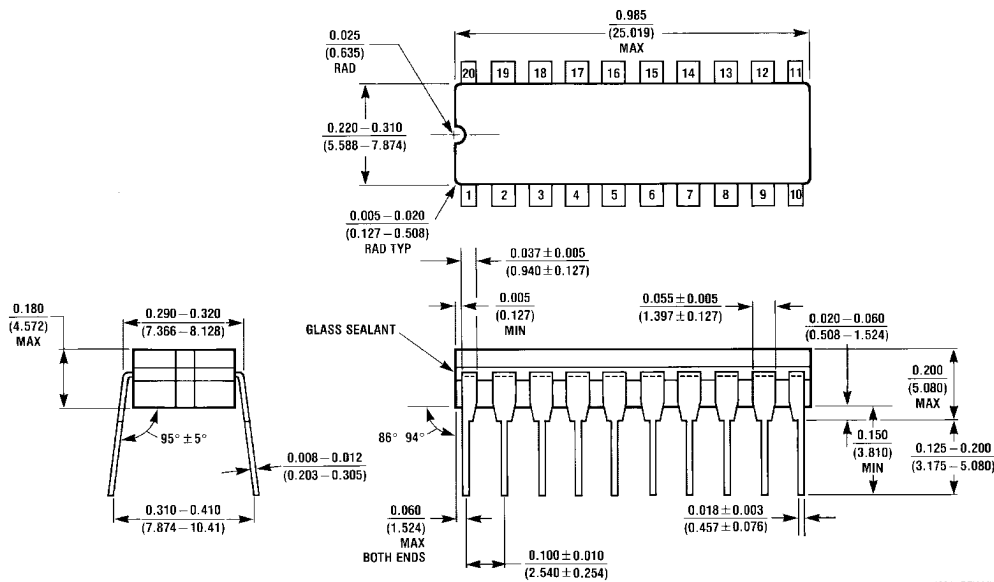
[查询"54ABT541CDM"供应商](#)



Physical Dimensions inches (millimeters) unless otherwise noted

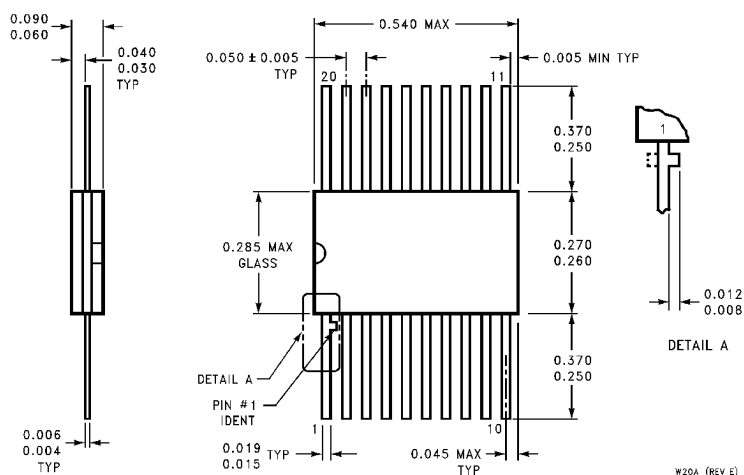


20-Terminal Ceramic Chip Carrier
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpack
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.