查询"5962-8853501QA"供应商

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	1.3, Absolute maximum ratings, changed DC input voltage minimum limit. 1.4, Recommended operating conditions, changed input low voltage minimum limit. Table I, t_{PWH}, device 02, maximim limit corrected. Editorial changes throughout. Table I, footnote 1/, 30 seconds changed to 1 second.	1990 OCT 31	Hackman

REV																							
SHEET																							
REV																							
SHEET																							
REV STATUS OF SHEETS	REV	A	A	A								A	A		A			A	A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Todd D Cook

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 26 MAY 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 4-BIT SLICE MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88535

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1746

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88535	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Cycle time
01	7C901-32, 39C01C	4-bit microprocessor slice	32 ns
02	7C901-27, 39C01D	4-bit microprocessor slice	27 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual in-line package
X	C-5 (44-terminal, .662" X .662" X .120"), square chip carrier package
Y	See figure 1 (42-lead, 1.070" X .650" X .100"), flat package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to +7.0 V dc
DC output current	30 mA
Maximum power dissipation 2/	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q and X	See MIL-M-38510, appendix C
Case Y	10°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Input high voltage (V_{IH})	2.0 V dc to 6.0 V dc
Input low voltage (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated on the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -3.4 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16.0 mA	1,2,3	All		0.4	V
Input high voltage	V_{IH}		1,2,3	All	2.0		V
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V $GND \le V_{IN} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V $GND \le V_{OUT} \le V_{CC}$	1,2,3	All	-40	+40	µA
Output short circuit current 1/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	1,2,3	All	-30	-85	mA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f_{CP} = 10 MHz V_{IL} = 0.8 V, V_{IH} = 2.0 V CP = 50% duty cycle	1,2,3	All		90	mA
Dynamic supply current	I_{CC2}	V_{CC} = 5.5 V, f_{CP} = 10 MHz CP = 50% duty cycle V_{IL} = 0.4 V, V_{IH} = 4.3 V	1,2,3	All		31	mA
Input capacitance	C_{IN}	See 4.3.1c V_{CC} = 5.0 V 2/	4	All		12	pF
Output capacitance	C_{OUT}			All		15	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Functional tests		See 4.3.1d	All	7,8			
A setup time to positive edge of clock 4/	t_{S1}	See figure 4. 3/	01	9,10,11	32		ns
			02		25		
A setup time to negative edge of clock 4/	t_{S2}		01	9,10,11	15		ns
			02		12		
B (source) setup time to positive edge of clock 4/	t_{S3}		01	9,10,11	32		ns
			02		25		
B (source) setup time to negative edge of clock 4/	t_{S4}		01	9,10,11	15		ns
			02		12		
B (destination) setup time to negative edge of clock	t_{S5}		01	9,10,11	15		ns
			02		12		
Data setup time to positive edge of clock	t_{S6}		01	9,10,11	25		ns
			02		16		
C_n setup time to positive edge of clock	t_{S7}		01	9,10,11	20		ns
			02		13		
$I_{0,1,2}$ setup time to positive edge of clock	t_{S8}		01	9,10,11	30		ns
			02		19		
$I_{3,4,5}$ setup time to positive edge of clock	t_{S9}		01	9,10,11	30		ns
			02		19		
$I_{6,7,8}$ setup time to negative edge of clock	t_{S10}		01	9,10,11	10		ns
			02		9		
$RAM_{0,3}$,$Q_{0,3}$ setup time to positive edge of clock	t_{S11}		01	9,10,11	12		ns
			02		9		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
A hold time from positive edge of clock 5/	t_{H1}	See figure 4. 3/	01	9,10,11	2		ns
			02		2		
A hold time from negative edge of clock 5/	t_{H2}		01	9,10,11	2		ns
			02		2		
B (source) hold time from positive edge of clock 5/	t_{H3}		01	9,10,11	2		ns
			02		2		
B (source) hold time from negative edge of clock 5/	t_{H4}		01	9,10,11	2		ns
			02		2		
B (destination) hold time from positive edge of clock	t_{H5}		01	9,10,11	2		ns
			02		2		
Data hold time from positive edge of clock	t_{H6}		01	9,10,11	0		ns
			02		0		
C_n hold time from positive edge of clock	t_{H7}		01	9,10,11	0		ns
			02		0		
$I_{0,1,2}$ hold time from positive edge of clock	t_{H8}		01	9,10,11	0		ns
			02		0		
$I_{3,4,5}$ hold time from positive edge of clock	t_{H9}		01	9,10,11	0		ns
			02		0		
$I_{6,7,8}$ hold time from positive edge of clock	t_{H10}		01	9,10,11	0		ns
			02		0		
$RAM_{0,3}$,$Q_{0,3}$ hold time from positive edge of clock	t_{H11}		01	9,10,11	0		ns
			02		0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Delay from A to Y	t_{P1}	See figure 4. 3/	01	9,10,11		48	ns
			02			33	
Delay from A to F_3	t_{P2}		01	9,10,11		48	ns
			02			33	
Delay from A to C_{n+4}	t_{P3}		01	9,10,11		48	ns
			02			33	
Delay from A to $\overline{G}$ and $\overline{P}$	t_{P4}		01	9,10,11		44	ns
			02			33	
Delay from A to F = 0	t_{P5}		01	9,10,11		48	ns
			02			33	
Delay from A to OVR	t_{P6}		01	9,10,11		48	ns
			02			33	
Delay from A to RAM_0, RAM_3	t_{P7}		01	9,10,11		48	ns
			02			33	
Delay from B to Y	t_{P8}		01	9,10,11		48	ns
			02			33	
Delay from B to F_3	t_{P9}		01	9,10,11		48	ns
			02			33	
Delay from B to C_{n+4}	t_{P10}		01	9,10,11		48	ns
			02			33	
Delay from B to $\overline{G}$ and $\overline{P}$	t_{P11}		01	9,10,11		44	ns
			02			33	
Delay from B to F = 0	t_{P12}		01	9,10,11		48	ns
			02			33	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Delay from B to OVR	t_{P13}	See figure 4. 3/	01	9,10,11		48	ns
			02			33	
Delay from B to RAM_0, RAM_3	t_{P14}		01	9,10,11		48	ns
			02			33	
Delay from data to Y	t_{P15}		01	9,10,11		37	ns
			02			24	
Delay from data to F_3	t_{P16}		01	9,10,11		37	ns
			02			23	
Delay from data to C_{n+4}	t_{P17}		01	9,10,11		37	ns
			02			23	
Delay from data to $\overline{G}$ and $\overline{P}$	t_{P18}		01	9,10,11		34	ns
			02			21	
Delay from data to F = 0	t_{P19}		01	9,10,11		40	ns
			02			25	
Delay from data to OVR	t_{P20}		01	9,10,11		37	ns
			02			24	
Delay from data to RAM_0, RAM_3	t_{P21}		01	9,10,11		37	ns
			02			25	
Delay from C_n to Y	t_{P22}		01	9,10,11		25	ns
			02			18	
Delay from C_n to F_3	t_{P23}		01	9,10,11		25	ns
			02			17	
Delay from C_n to C_{n+4}	t_{P24}		01	9,10,11		21	ns
			02			14	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Delay from C_n to F = 0	t_{P26}	See figure 4. 3/	01	9,10,11		28	ns
			02			19	
Delay from C_n to OVR	t_{P27}		01	9,10,11		25	ns
			02			17	
Delay from C_n to RAM_0, RAM_3	t_{P28}		01	9,10,11		28	ns
			02			19	
Delay from $I_{0,1,2}$ to Y	t_{P29}		01	9,10,11		40	ns
			02			28	
Delay from $I_{0,1,2}$ to F_3	t_{P30}		01	9,10,11		40	ns
			02			27	
Delay from $I_{0,1,2}$ to C_{n+4}	t_{P31}		01	9,10,11		40	ns
			02			26	
Delay from $I_{0,1,2}$ to $\overline{G}$ and $\overline{P}$	t_{P32}		01	9,10,11		44	ns
			02			28	
Delay from $I_{0,1,2}$ to F = 0	t_{P33}		01	9,10,11		44	ns
			02			29	
Delay from $I_{0,1,2}$ to OVR	t_{P34}		01	9,10,11		40	ns
			02			27	
Delay from $I_{0,1,2}$ to RAM_0, RAM_3	t_{P35}		01	9,10,11		40	ns
			02			27	
Delay from $I_{3,4,5}$ to Y	t_{P36}		01	9,10,11		40	ns
			02			27	
Delay from $I_{3,4,5}$ to F_3	t_{P37}		01	9,10,11		40	ns
			02			27	
Delay from $I_{3,4,5}$ to C_{n+4}	t_{P38}		01	9,10,11		40	ns
			02			26	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Delay from $I_{3,4,5}$ to $\overline{G}$ and $\overline{P}$	t_{P39}	See figure 4. 3/	01	9,10,11		40	ns
			02			26	
Delay from $I_{3,4,5}$ to F = 0	t_{P40}		01	9,10,11		40	ns
			02			27	
Delay from $I_{3,4,5}$ to OVR	t_{P41}		01	9,10,11		40	ns
			02			26	
Delay from $I_{3,4,5}$ to RAM_0, $\overline{RAM}_3$	t_{P42}		01	9,10,11		40	ns
			02			27	
Delay from $I_{6,7,8}$ to Y	t_{P43}		01	9,10,11		29	ns
			02			18	
Delay from $I_{6,7,8}$ to RAM_0, $\overline{RAM}_3$	t_{P44}		01	9,10,11		29	ns
			02			21	
Delay from $I_{6,7,8}$ to Q_0, Q_3	t_{P45}		01	9,10,11		29	ns
			02			21	
Delay from A (I = 2XX) to Y	t_{P46}		01	9,10,11		40	ns
			02			26	
Delay from CP to Y	t_{P47}		01	9,10,11		40	ns
			02			27	
Delay from CP to F_3	t_{P48}		01	9,10,11		40	ns
			02			26	
Delay from CP to C_{n+4}	t_{P49}		01	9,10,11		40	ns
			02			26	
Delay from CP to $\overline{G}$ and $\overline{P}$	t_{P50}		01	9,10,11		40	ns
			02			25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Delay from CP to F = 0	t_{P51}	See figure 4. 3/	01	9,10,11		40	ns
			02			27	
Delay from CP to OVR	t_{P52}		01	9,10,11		40	ns
			02			26	
Delay from CP to RAM_0, RAM_3	t_{P53}		01	9,10,11		40	ns
			02			27	
Delay from CP to Q_0, Q_3	t_{P54}		01	9,10,11		33	ns
			02			20	
Delay from $\overline{OE}$ to Y 6/ 7/	t_{P55}		01	9,10,11		25	ns
			02			16	
Delay from $\overline{OE}$ to Y float 6/ 7/	t_{P56}		01	9,10,11		25	ns
			02			18	
Minimum clock low time	t_{PWL}		01	9,10,11		17	ns
			02			15	
Minimum clock high time	t_{PWH}		01	9,10,11		15	ns
			02			13	
Minimum clock period	t_{CP}		01	9,10,11		32	ns
			02			27	

See footnotes on next page.

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1/ For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 1 second.

2/ The capacitance measurement shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV RMS.

3/ AC parameters are tested using input rise and fall times of 3 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V.

4/ The setup time prior to the clock low to high transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock low to high transition, regardless of when the clock high to low transition occurs.

5/ Source addresses must be stable prior to the clock high to low transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock low time.

6/ This parameter if not tested, shall be guaranteed to the limits specified in table I.

7/ Output disable tests performed with C_L = 5 pF and measured to 0.5 V change of output voltage level.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.5 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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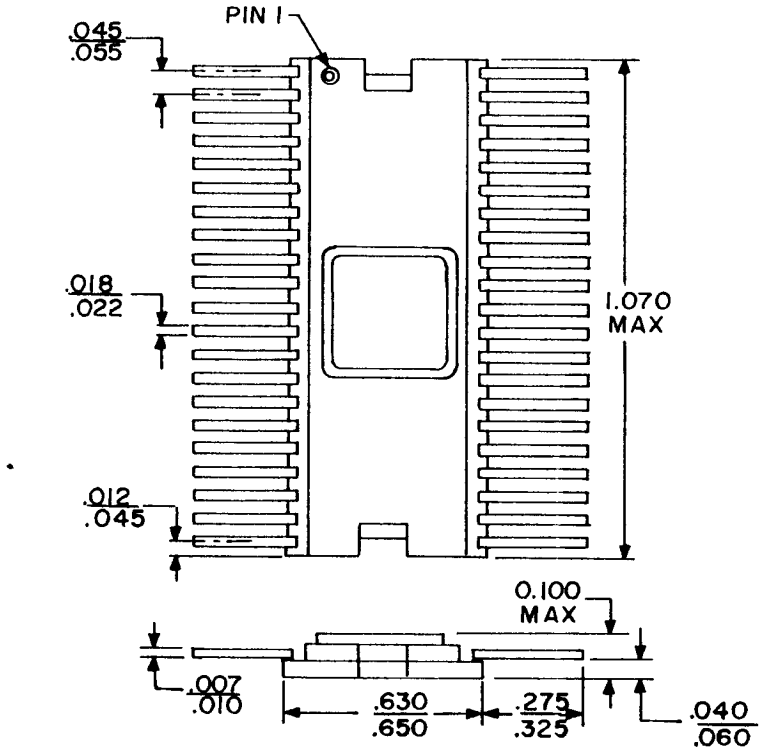

NOTE: All units are specified in inches.

FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88535
		REVISION LEVEL	SHEET 13

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Device types	01 and 02						
Package	Q	X	Y	Package	Q	X	Y
Pin number				Pin number			
1	A_3	A_3	I_8	26	I_3	D_1	C_n
2	A_2	A_2	I_7	27	I_5	D_0	GND
3	A_1	A_1	RAM_3	28	I_4	NC	F_3
4	A_0	A_0	NC				
5	I_6	I_6	RAM_0	29	C_n	I_3	$\overline{G}$
6	I_8	NC	V_{CC}	30	GND	I_5	C_{n+4}
7	I_7	I_8	F = 0	31	F_3	I_4	OVR
8	RAM_3	I_7	I_0				
9	RAM_0	RAM_3	I_1	32	$\overline{G}$	C_n	$\overline{P}$
10	V_{CC}	RAM_0	I_2	33	C_{n+4}	GND	Y_0
11	F = 0	V_{CC}	$\overline{CP}$	34	OVR	F_3	Y_1
12	I_0	F = 0	NC				
13	I_1	I_0	Q_3	35	$\overline{P}$	$\overline{G}$	Y_2
14	I_2	I_1	B_0	36	Y_0	C_{n+4}	Y_3
15	$\overline{CP}$	I_2	B_1				
16	Q_3	$\overline{CP}$	B_2	37	Y_1	OVR	$\overline{OE}$
17	B_0	NC	B_3	38	Y_2	$\overline{P}$	A_3
18	B_1	Q_3	Q_0	39	Y_3	NC	A_2
19	B_2	B_0	D_3				
20	B_3	B_1	D_2	40	$\overline{OE}$	Y_0	A_1
21	Q_0	B_2	D_1	41	-	Y_1	A_0
22	D_3	B_3	D_0	42	-	Y_2	I_6
23	D_2	Q_0	I_3	43	-	Y_3	-
24	D_1	D_3	I_5				
25	D_0	D_2	I_4	44	-	$\overline{OE}$	-

FIGURE 2. Terminal connections.

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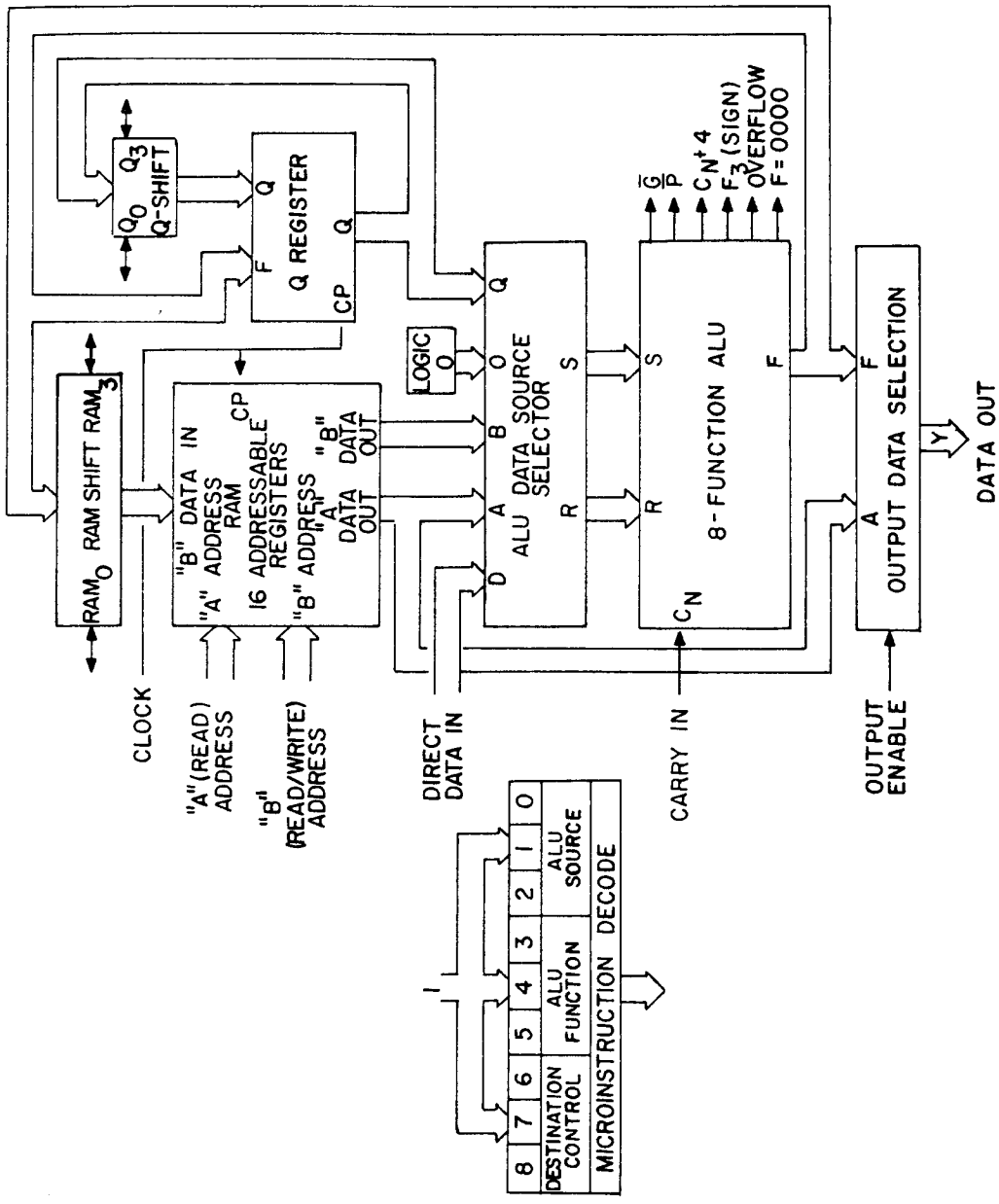

FIGURE 3. Functional block diagram.

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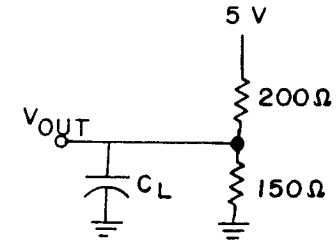
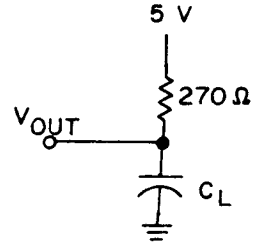


ALL OUTPUTS EXCEPT (F=0)



(F=0)

NOTES:
1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.

FIGURE 4. AC loading test circuits (or equivalent).

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 with zero rejects shall be required.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

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6.6 Pin descriptions.

Mnemonic	Type	Description
A_0 - A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0 - B_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0 - I_8	I	These 9 instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$) and what data is to be written back into either the Q register or the register file ($I_{6, 7, 8}$).
D_0 - D_3	I	These are 4 data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
Y_0 - Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output enable. This is an active LOW input that controls the Y_0 - Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock input.
Q_3, RAM_3	I/O	These 2 lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatable CMOS inputs.
Q_0, RAM_0	I/O	These 2 lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry into the internal ALU.
C_{n+4}	O	The carry out of the internal ALU.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	Overflow. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine.
F = 0	O	Open drain output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW.
F_3	O	The most significant bit of the ALU output.

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6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8853501QX	61772 65786 66579	IDT39C01CDB CY7C901-32DMB WS5901CDMB
5962-8853501XX	61772 65786	IDT39C01CLB CY7C901-32LMB
5962-8853501YX	65786	CY7C901-32FMB
5962-8853502QX	61772 65786	IDT39C01DDB CY7C901-27DMB
5962-8853502XX	61772 65786	IDT39C01DLB CY7C901-27LMB
5962-8853502YX	65786	CY7C901-27FMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology Incorporated 1566 Moffett Boulevard Salinas, CA 93905 Point of contact: 3236 Scott Blvd. Santa Clara, CA 95054
65786	Cypress Semiconductor Corporation 3901 N. First Street San Jose, CA 95134-1599
66579	Waferscale Integration Incorporated 47280 Kato Road Fremont, CA 94538

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