

±200-V COMMON-MODE VOLTAGE DIFFERENCE AMPLIFIER

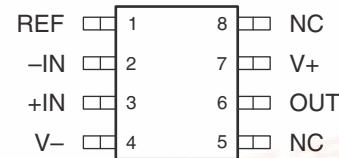
FEATURES

- Qualified for Automotive Applications
- High Common-Mode Voltage
 - 75 V at $V_S = 5$ V
 - ±200 V at $V_S = \pm 15$ V
- Fixed Differential Gain = 1 V/V
- Low Quiescent Current: 260 mA
- Wide Supply Range
 - Single Supply: 2.7 V to 36 V
 - Dual Supplies: ±1.35 V to ±18 V
- Low Gain Error: 0.075% Max
- Low Nonlinearity: 0.002% Max
- High CMR: 86 dB
- Surface-Mount SO-8 (D) Package

APPLICATIONS

- Current-Shunt Measurements
- Differential Sensor Amplifiers
- Line Receivers
- Battery-Powered Systems
- Automotive Instrumentation
- Stacked-Cell Monitors

D PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The INA148 is a precision low-power unity-gain difference amplifier with a high common-mode input voltage range. It consists of a monolithic precision bipolar operational amplifier with a thin-film resistor network.

The on-chip resistors are laser trimmed for an accurate 1-V/V differential gain and high common-mode rejection. Excellent temperature tracking of the resistor network maintains high gain accuracy and common-mode rejection over temperature. The INA148 operates on single or dual supplies.

The INA148 is available in a small SO-8 surface-mount package, and it is specified for operation over the temperature range of –40°C to 125°C.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Reel of 2500 | INA148QDRQ1 | 148Q1 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | |
|---------------|---|----------------------------|----------------|
| V_S | Supply voltage, V_+ to V_- | | 36 V |
| V_{IN} | Input voltage | Continuous | ± 200 V |
| | | Peak (0.1 second) | ± 500 V |
| t_{SS} | Short circuit to ground duration | | Continuous |
| θ_{JA} | Package thermal impedance, junction to free air | | 97.1°C/W |
| T_A | Operating free-air temperature range | | -40°C to 125°C |
| T_J | Maximum operating virtual-junction temperature | | 150°C |
| T_{stg} | Storage temperature range | | -65°C to 150°C |
| T_{lead} | Lead temperature range (soldering, 10 seconds) | | 300°C |
| ESD | Electrostatic discharge rating | Human-Body Model (HBM) | 1500 V |
| | | Machine Model (MM) | 150 V |
| | | Charged-Device Model (CDM) | 2000 V |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|-------|--------------------------------|---------------|------------|----------|------|
| V_S | Supply voltage | Single supply | 2.7 | 36 | V |
| | | Dual supply | ± 1.35 | ± 18 | |
| T_A | Operating free-air temperature | | -40 | 125 | °C |

ELECTRICAL CHARACTERISTICS

 $V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$ (dual supply), $R_L = 10\text{ k}\Omega$ to ground, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------|--|--|-------------------------|--------------|-------------------|-------------|------------------------------|
| V_{OS} | Input offset voltage ⁽¹⁾⁽²⁾ | $V_{CM} = 0\text{ V}$ | $V_S = \pm 15\text{ V}$ | | ± 1 | ± 5 | mV |
| | | | $V_S = \pm 5\text{ V}$ | | ± 1 | ± 5 | |
| $\Delta V_{OS}/\Delta T$ | Input offset voltage drift ⁽¹⁾ | $T_A = -40^\circ\text{C}$ to 125°C | | | ± 10 | | $\mu\text{V}/^\circ\text{C}$ |
| PSRR | Power supply ripple rejection ⁽¹⁾ | $V_S = \pm 1.35\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = 0\text{ V}$ | | | ± 50 | ± 400 | $\mu\text{V}/\text{V}$ |
| V_{CM} | Common-mode voltage range | $V_{+IN} - V_{-IN} = 0$ | $V_S = \pm 15\text{ V}$ | -200 | | 200 | V |
| | | | $V_S = \pm 5\text{ V}$ | -100 | | 80 | |
| CMRR | Common-mode rejection ratio | $V_S = \pm 15\text{ V}$, $V_{CM} = -200\text{ V}$ to 200 V , $R_S = 0\ \Omega$ | | 70 | 86 | | dB |
| | | $V_S = \pm 5\text{ V}$, $V_{CM} = -100\text{ V}$ to 80 V , $R_S = 0\ \Omega$ | | 70 | 86 | | |
| | Differential input impedance | | | | 2 | | M Ω |
| | Common-mode input impedance | | | | 1 | | M Ω |
| V_n | Voltage noise ⁽¹⁾⁽³⁾ | $f = 0.1\text{ Hz}$ to 10 Hz | | | 17 | | μV_{p-p} |
| | Voltage noise density ⁽¹⁾⁽³⁾ | $f = 1\text{ kHz}$ | | | 880 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | Initial gain ⁽¹⁾ | | | | 1 | | V/V |
| | Gain error | $V_O = (V_- + 0.5)$ to $(V_+ - 1.5)$ | | | ± 0.01 | ± 0.075 | % |
| | Gain error over temperature | | | | ± 3 | ± 10 | ppm/ $^\circ\text{C}$ |
| | Gain nonlinearity | $V_O = (V_- + 0.5)$ to $(V_+ - 1.5)$ | $V_S = \pm 15\text{ V}$ | | ± 0.00 1 | ± 0.002 | %FSR |
| | | | $V_S = \pm 5\text{ V}$ | | ± 0.00 1 | | %FSR |
| | Small signal bandwidth frequency response | | | | 100 | | kHz |
| SR | Slew rate | | | | 1 | | V/ μs |
| t_s | Settling time | $V_S = \pm 15\text{ V}$, 10-V step | 0.1% | | 21 | | μs |
| | | | 0.01% | | 25 | | |
| | | $V_S = \pm 5\text{ V}$, 6-V step | 0.1% | | 21 | | |
| | | | 0.01% | | 25 | | |
| | Overload recovery | 50% input overload | | | 24 | | μs |
| V_O | Output voltage | $R_L = 100\text{ k}\Omega$ | | $V_- + 0.25$ | | $V_+ - 1$ | V |
| | | $R_L = 10\text{ k}\Omega$ | | $V_- + 0.5$ | | $V_+ - 1.5$ | |
| I_O | Output current | Short-circuit current, continuous to common | | | ± 13 | | mA |
| C_L | Load capacitance | Stable operation | | | 10 | | nF |
| I_S | Supply current | $V_{IN} = 0$, $I_O = 0$ | | | ± 260 | ± 300 | μA |

(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and V_{-IN}), gain = 1 V/V.

(2) Includes effects of amplifier's input bias and offset currents.

(3) Includes effects of input current noise and thermal noise contribution of resistor network.

ELECTRICAL CHARACTERISTICS

$V_S = 5\text{ V}$ (single supply), $R_L = 10\text{ k}\Omega$ to $V_S/2$, $V_{REF} = V_S/2$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----------------|-------------|------------------------------|
| V_{OS} Input offset voltage ⁽¹⁾⁽²⁾ | $V_{CM} = V_S/2$ | | ± 1 | ± 5 | mV |
| $\Delta V_{OS}/\Delta T$ Input offset voltage drift ⁽¹⁾ | $T_A = -40^\circ\text{C}$ to 125°C | | ± 10 | | $\mu\text{V}/^\circ\text{C}$ |
| PSRR Power supply ripple rejection ⁽¹⁾ | $V_S = 2.7\text{ V}$ to 36 V , $V_{CM} = V_S/2$ | | ± 50 | ± 400 | $\mu\text{V}/\text{V}$ |
| V_{CM} Common-mode voltage range | $V_{+IN} - V_{-IN} = 0$ | $V_{REF} = 0.25\text{ V}$ | | 75 | V |
| | | $V_{REF} = V_S/2$ | | 32.5 | |
| CMRR Common-mode rejection ratio | $V_{CM} = -47.5\text{ V}$ to 32.5 V , $R_S = 0\text{ }\Omega$ | 70 | 86 | | dB |
| | Differential input impedance | | 2 | | M Ω |
| | Common-mode input impedance | | 1 | | M Ω |
| V_n Voltage noise ⁽¹⁾⁽³⁾ | $f = 0.1\text{ Hz}$ to 10 Hz | | 17 | | μV_{p-p} |
| | Voltage noise density ⁽¹⁾⁽³⁾ | | 880 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | Initial gain ⁽¹⁾ | | 1 | | V/V |
| | Gain error | $V_O = 0.5\text{ V}$ to 3.5 V | ± 0.01 | ± 0.075 | % |
| | Gain error over temperature | | ± 3 | ± 10 | $\text{ppm}/^\circ\text{C}$ |
| | Gain nonlinearity | $V_O = 0.5\text{ V}$ to 3.5 V | ± 0.00 1 | | %FSR |
| | Small signal bandwidth | | 100 | | kHz |
| SR Slew rate | | | 1 | | V/ μs |
| t_s Settling time | $V_S = 5\text{ V}$, 3-V step | 0.1% | | 21 | μs |
| | | 0.01% | | 25 | |
| | Overload recovery | 50% input overload | 13 | | μs |
| V_O Output voltage | $R_L = 100\text{ k}\Omega$ | $V_- + 0.25$ | | $V_+ - 1$ | V |
| | $R_L = 10\text{ k}\Omega$ | $V_- + 0.5$ | | $V_+ - 1.5$ | |
| I_O Output current | Short-circuit current, continuous to common | | ± 8 | | mA |
| C_L Load capacitance | Stable operation | | 10 | | nF |
| I_Q Quiescent current | $V_{IN} = 0$, $I_O = 0$ | | 260 | 300 | μA |

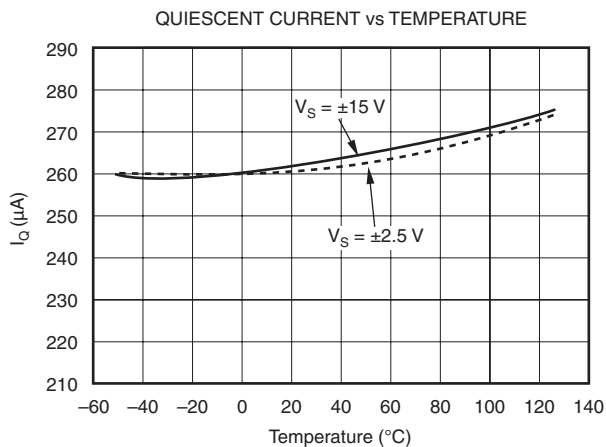
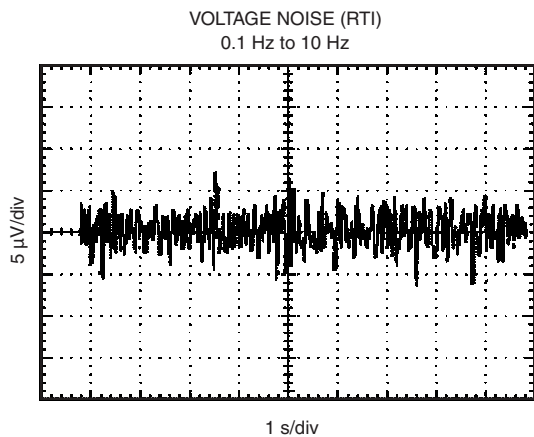
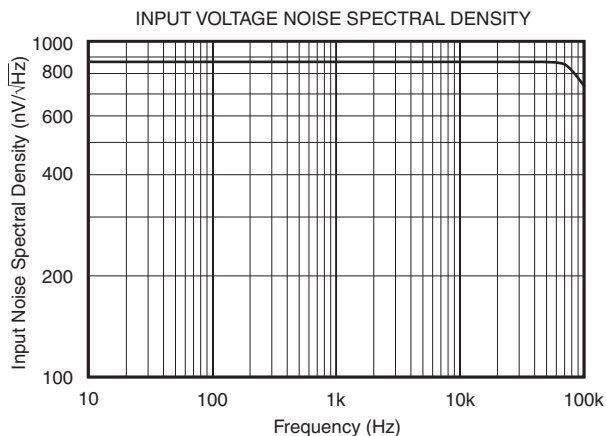
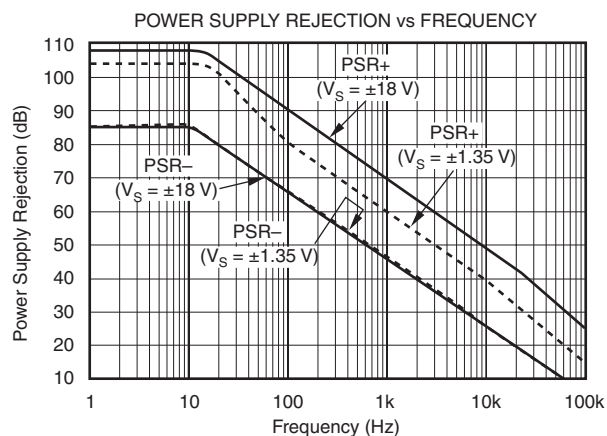
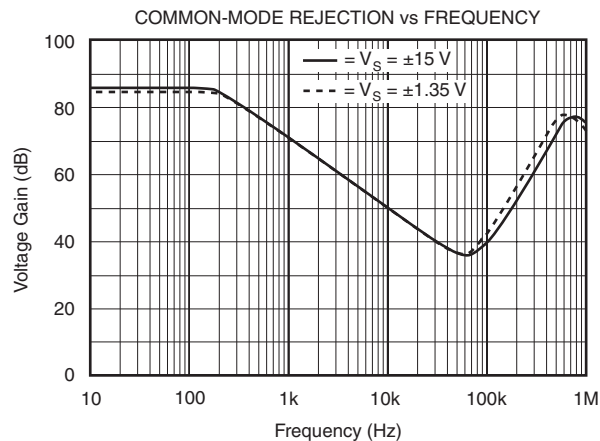
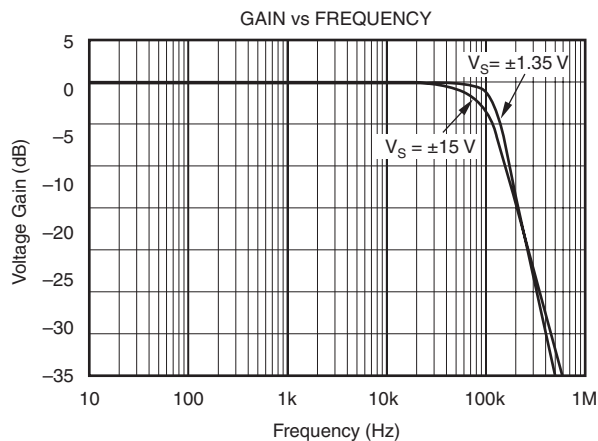
(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and V_{-IN}), gain = 1 V/V.

(2) Includes effects of amplifier's input bias and offset currents.

(3) Includes effects of input current noise and thermal noise contribution of resistor network.

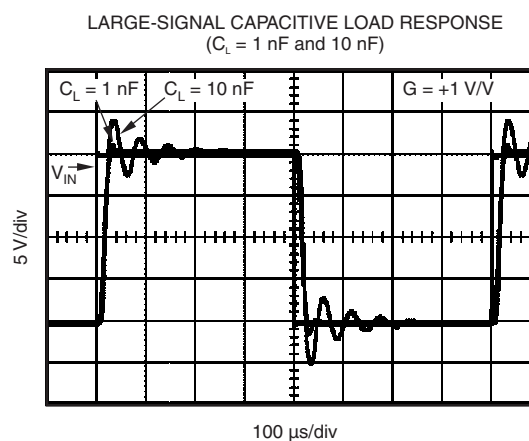
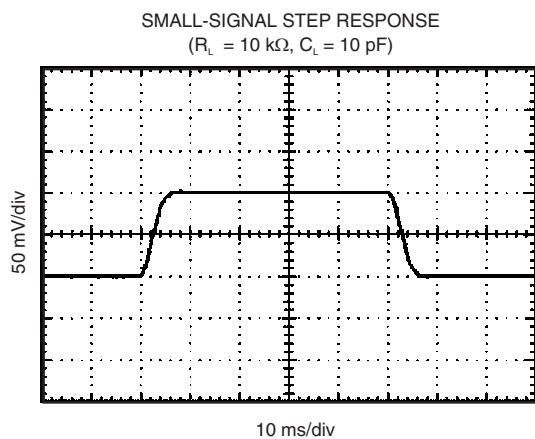
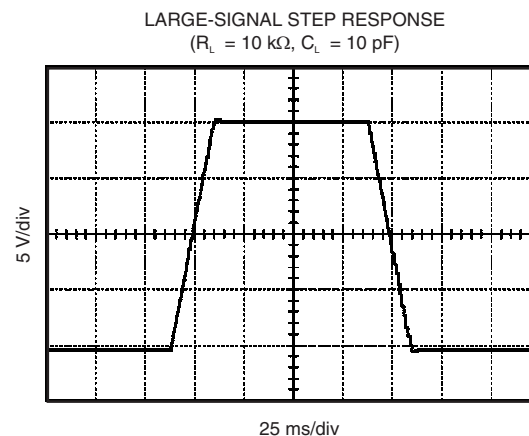
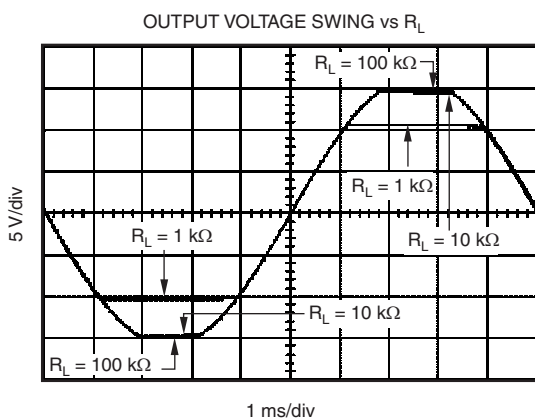
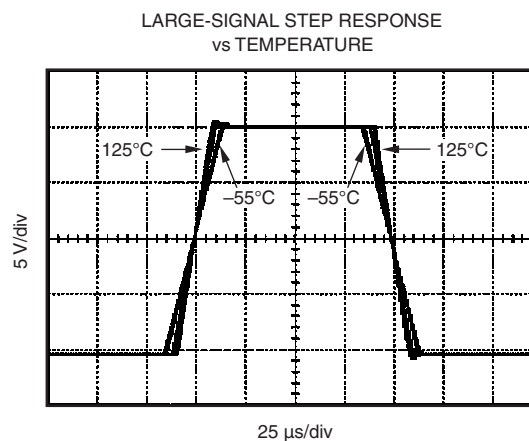
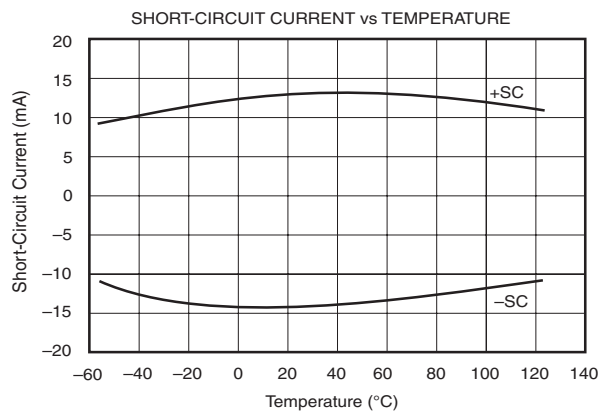
TYPICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to common, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



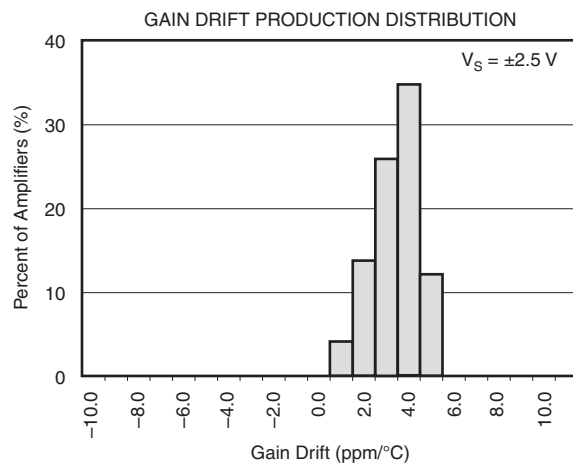
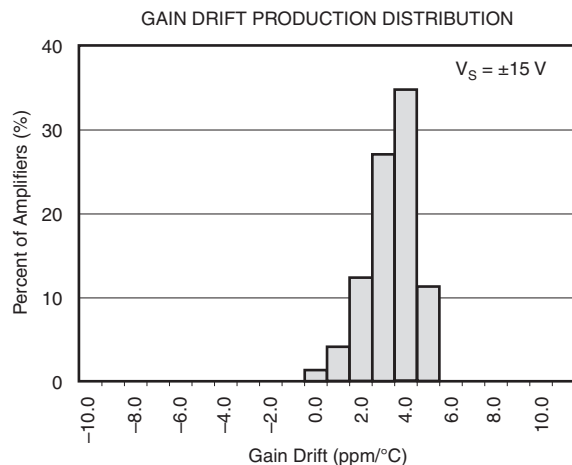
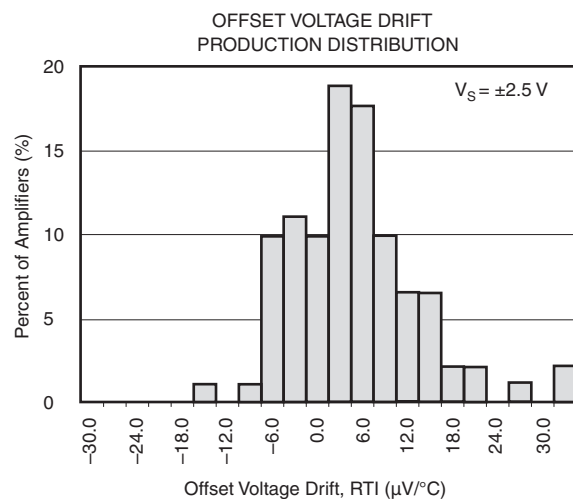
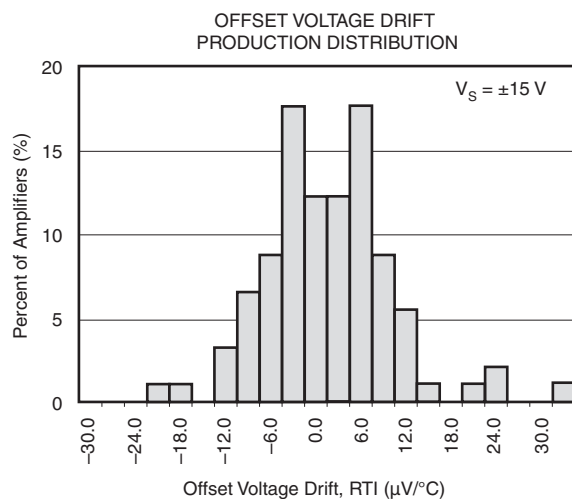
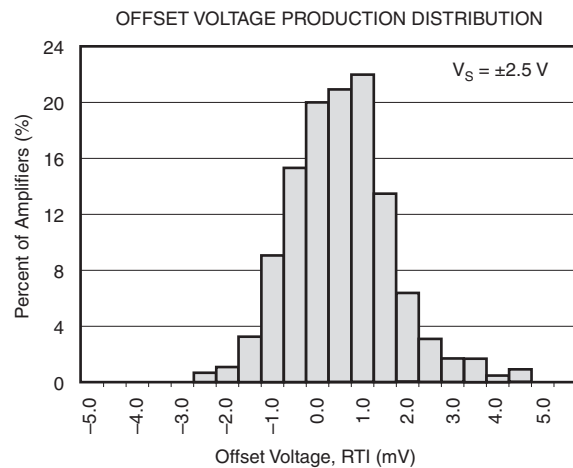
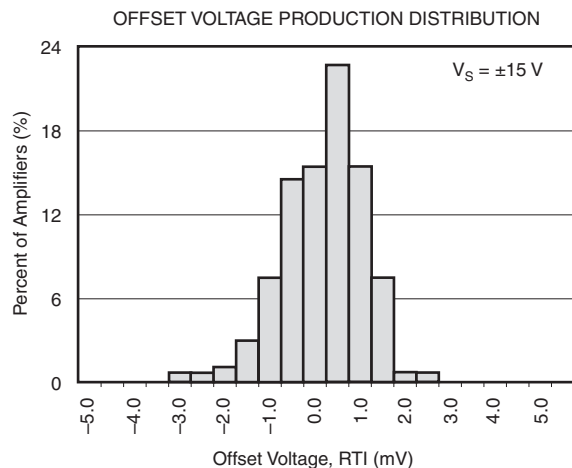
TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to common, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



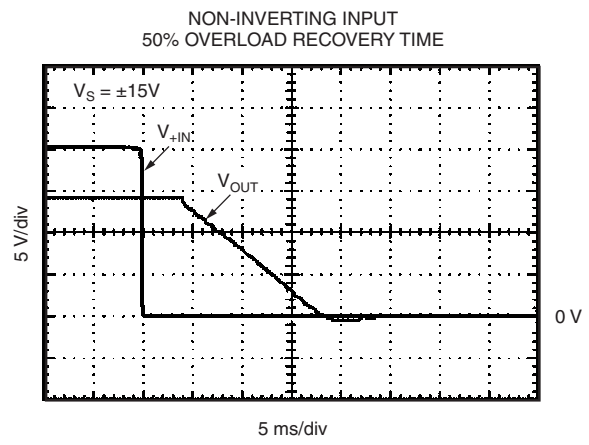
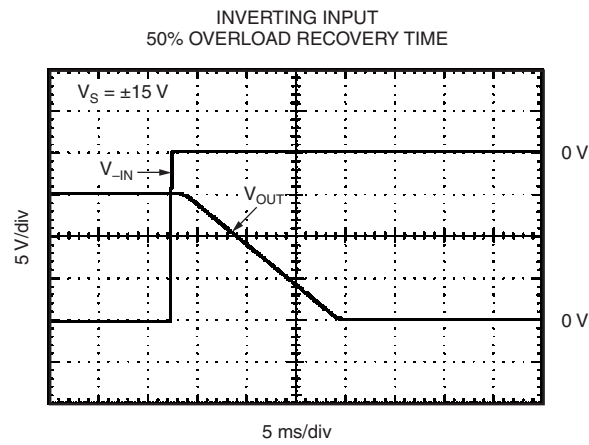
TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to common, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ to common, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



APPLICATION INFORMATION

The INA148 is a unity-gain difference amplifier with a high common-mode input voltage range. A basic diagram of the circuit and pin connections is shown in [Figure 1](#).

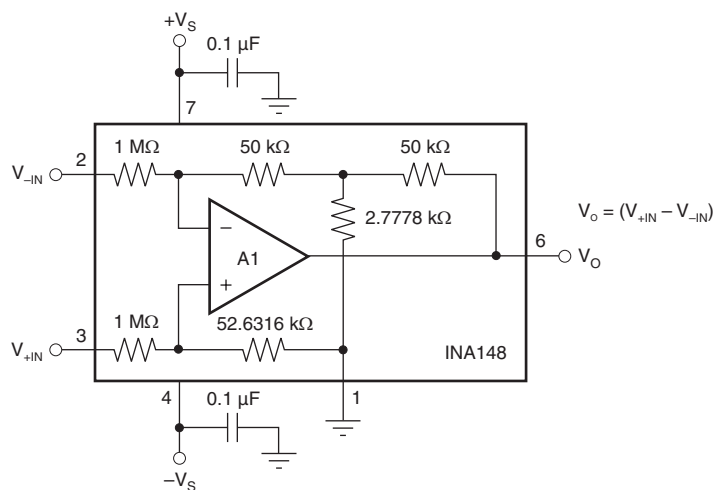


Figure 1. Basic Circuit Connections

To achieve its high common-mode voltage range, the INA148 features a precision laser-trimmed thin-film resistor network with a 20:1 input voltage divider ratio. High input voltages are thereby reduced in amplitude, allowing the internal operational amplifier (op amp) to "see" input voltages that are within its linear operating range. A "Tee" network in the op amp feedback network places the amplifier in a gain of 20 V/V, thus restoring the circuit's overall gain to unity (1 V/V).

External voltages can be summed into the amplifier's output by using the REF pin, making the differential amplifier a highly versatile design tool. Voltages on the REF pin also influence the INA148's common-mode voltage range.

In accordance with good engineering practice for linear integrated circuits, the INA148's power-supply bypass capacitors should be connected as close to pins 4 and 7 as practicable. Ceramic or tantalum types are recommended for use as bypass capacitors.

The input impedances are unusually high for a difference amplifier and this should be considered when routing input signal traces on a PC board. Avoid placing digital signal traces near the difference amplifier's input traces to minimize noise pickup.

Operating Voltage

The INA148 is specified for ± 15 -V and ± 5 -V dual supplies and 5-V single supplies. The INA148 can be operated with single or dual supplies with excellent performance.

The INA148 is fully characterized for supply voltages from ± 1.35 V to ± 18 V and over temperatures of -40°C to 125°C . Parameters that vary significantly with operating voltage, load conditions, or temperature are shown in the *Typical Characteristics* section.

Gain Equation

An internal on-chip resistor network sets the overall differential gain of the INA148 to precisely 1 V/V. Output is accordance with [Equation 1](#).

$$V_{\text{OUT}} = (V_{+IN} - V_{-IN}) + V_{\text{REF}} \quad (1)$$

Common-Mode Range

The 20:1 input resistor ratio of the INA148 provides an input common-mode range that extends well beyond its power supply rails.

The exact input voltage range depends on the amplifier's power-supply voltage and the voltage applied to the REF terminal (pin 1). Typical input voltage ranges at different power supply voltages can be found in the applications circuits section.

Offset Trim

The INA148 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment.

Because a voltage applied to the reference (REF) pin (pin 1) is summed directly into the amplifier's output signal, this technique can be used to null the amplifier's input offset voltage. [Figure 2](#) shows an optional circuit for trimming the offset voltage.

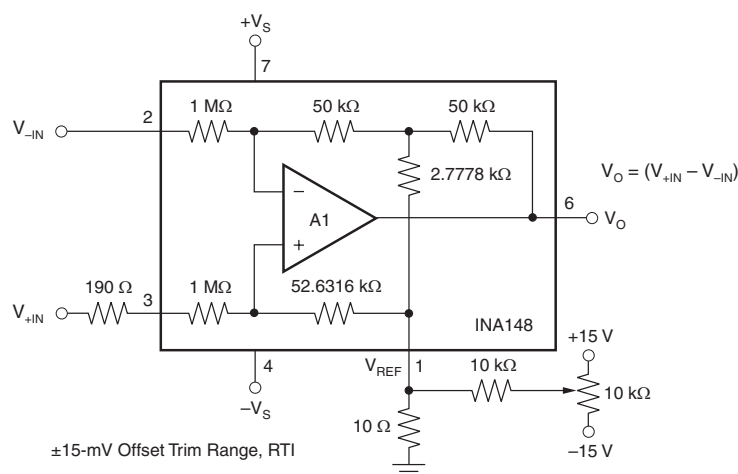


Figure 2. Optional Offset Trim Circuit

To maintain high common-mode rejection (CMR), the source impedance of any signal applied to the REF terminal should be very low ($\leq 5 \Omega$).

A source impedance of only 10 Ω at the REF pin reduces the INA148's CMR to approximately 74 dB. High CMR can be restored if a resistor is added in series with the amplifier's positive input terminal (pin 3). This resistor should be 19 times the source impedance that drives the REF pin. For example, if the REF pin sees a source impedance of 10 Ω , a resistor of 190 Ω should be added in series with pin 3.

Preferably, the offset trim voltage applied to the REF pin should be buffered with an amplifier such as an OPA237 (see [Figure 3](#)). In this case, the op amp output impedance is low enough that no external resistor is needed to maintain the INA148's excellent CMR.

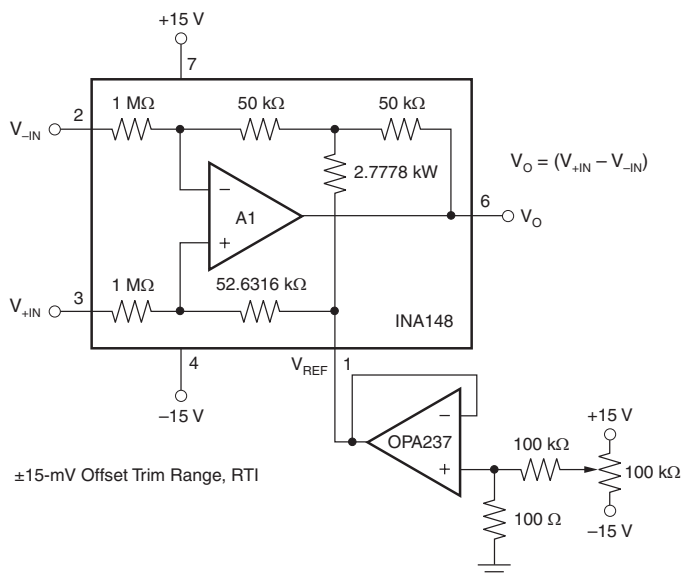


Figure 3. Preferred Offset Trim Circuit

Input Impedance

The input resistor network determines the impedance of each of the INA148 inputs. It is approximately 1 MΩ. Unlike an instrumentation amplifier, signal source impedances at the two input terminals must be nearly equal to maintain good common-mode rejection.

A mismatch between the two inputs' source impedances causes a differential amplifier's common-mode rejection to be degraded. With a source impedance imbalance of only 500 Ω, CMR can fall to approximately 66 dB.

Figure 4 shows a common application—measuring power supply current through a shunt resistor (R_S). A shunt resistor creates an unbalanced source resistance condition that can degrade a differential amplifier's common mode rejection.

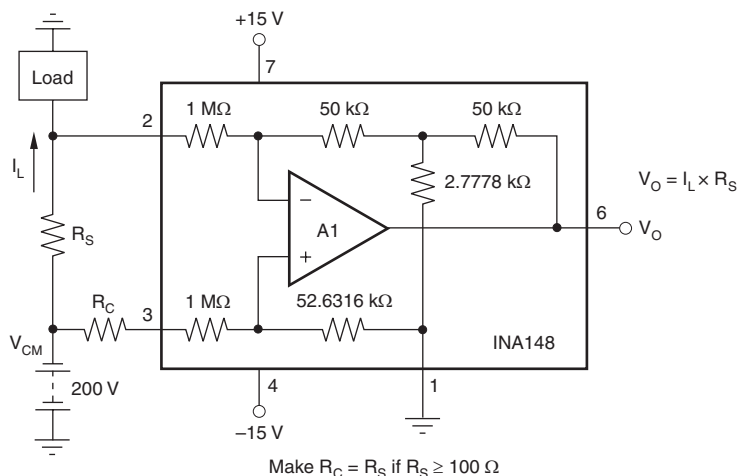


Figure 4. Shunt-Resistor Current Measurement Circuit

Unless the shunt resistor is less than approximately 100 Ω, an additional equal compensating resistor (R_C) is recommended to maintain input balance and high CMR.

查询"INA148-Q1"供应商

Source impedances (or shunts) greater than 5 k Ω are not recommended, even if they are "perfectly" compensated. This is because the internal resistor network is laser-trimmed for accurate voltage divider ratios, but not necessarily to absolute values. Input resistors are shown as 1 M Ω , however, this is only their nominal value.

In practice, the input resistors' absolute values may vary by as much as 30%. The two input resistors match to about 5%, so adding compensating resistors greater than 5 k Ω can cause a serious mismatch in the resulting resistor network voltage divider ratios, thus degrading CMR.

Attempts to extend the INA148 input voltage range by adding external resistors is not recommended for the reasons described in the previous paragraph. CMR suffers serious degradation unless the resistors are carefully trimmed for CMR and gain. This is an iterative adjustment and can be tedious and time consuming.

Typical Application Circuits

Figure 5 through Figure 9 show typical application circuits for the INA148.

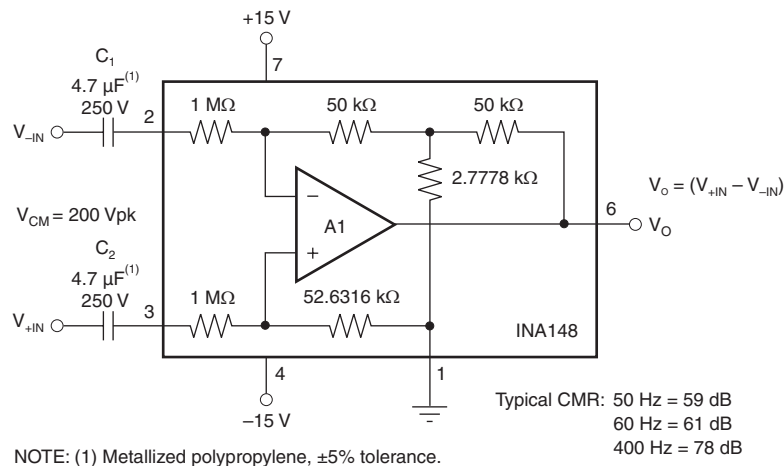


Figure 5. AC-Coupled Difference Amplifier

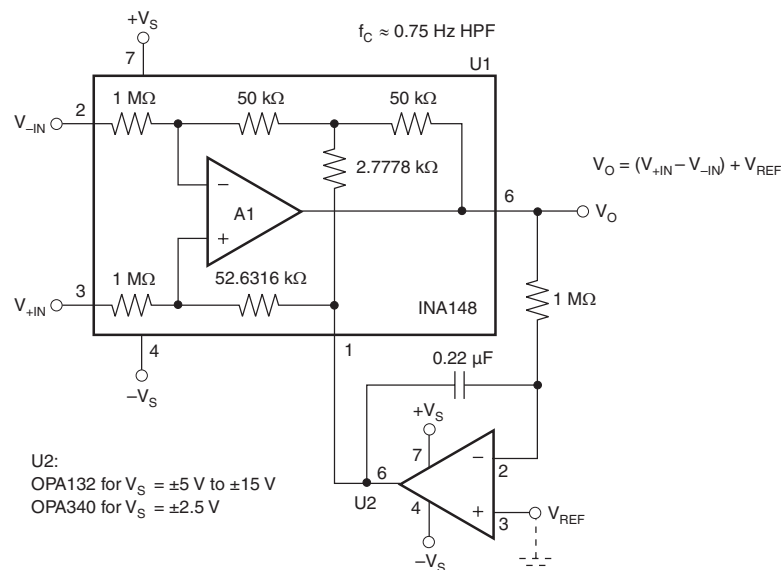


Figure 6. Quasi-AC-Coupled Differential Amplifier

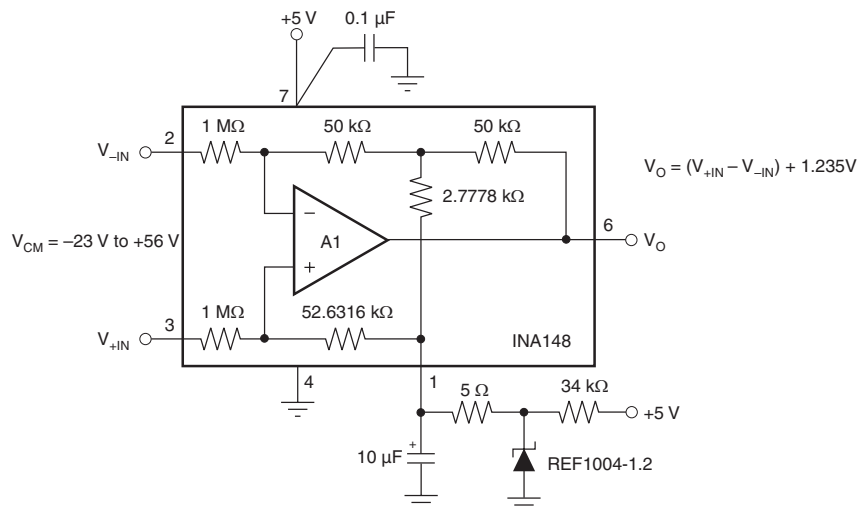


Figure 7. Single-Supply Differential Amplifier

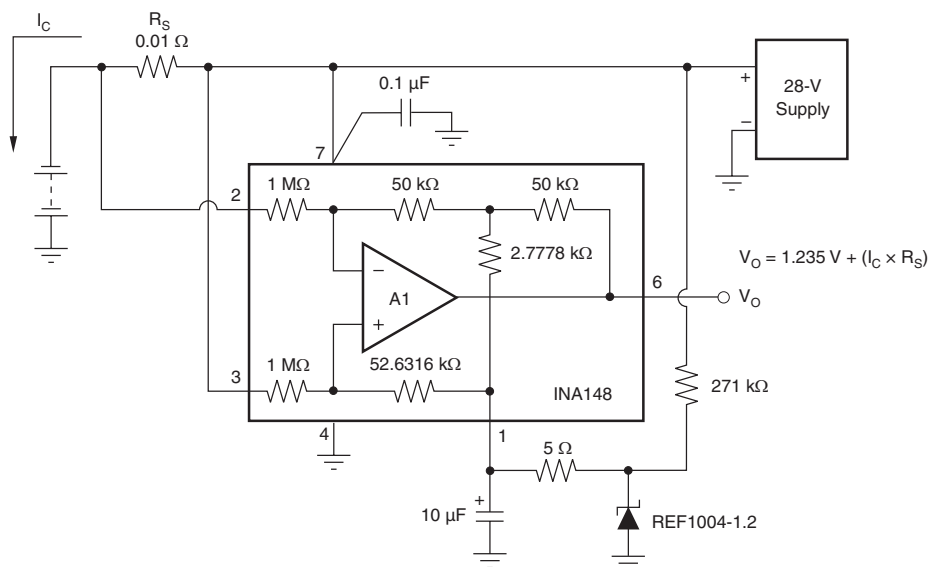


Figure 8. Battery Monitor Circuit

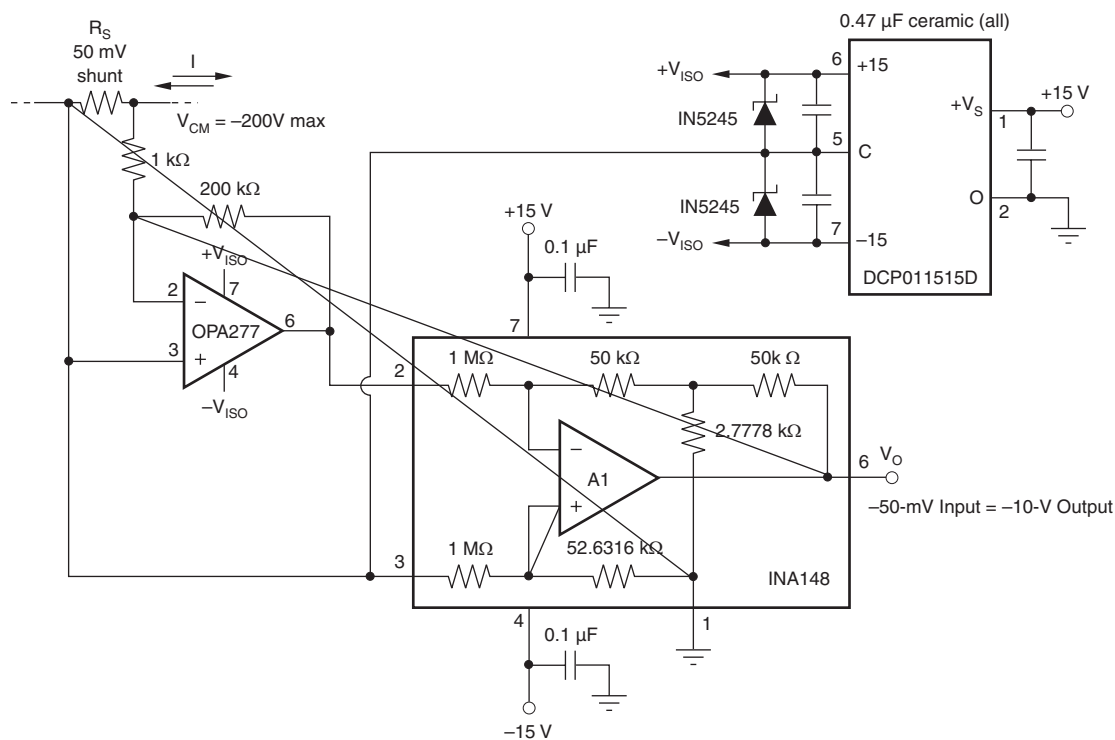


Figure 9. 50-mV Current-Shunt Amplifier with ± 200 -V Common-Mode Voltage Range



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PACKAG

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Pe |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|--------------|
| INA148QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-2600 |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all RoHS compliant products except that lead may not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in applications that require high temperature soldering processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach between the package and the carrier.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (RoHS). This does not include materials that are RoHS compliant but contain Br and/or Sb.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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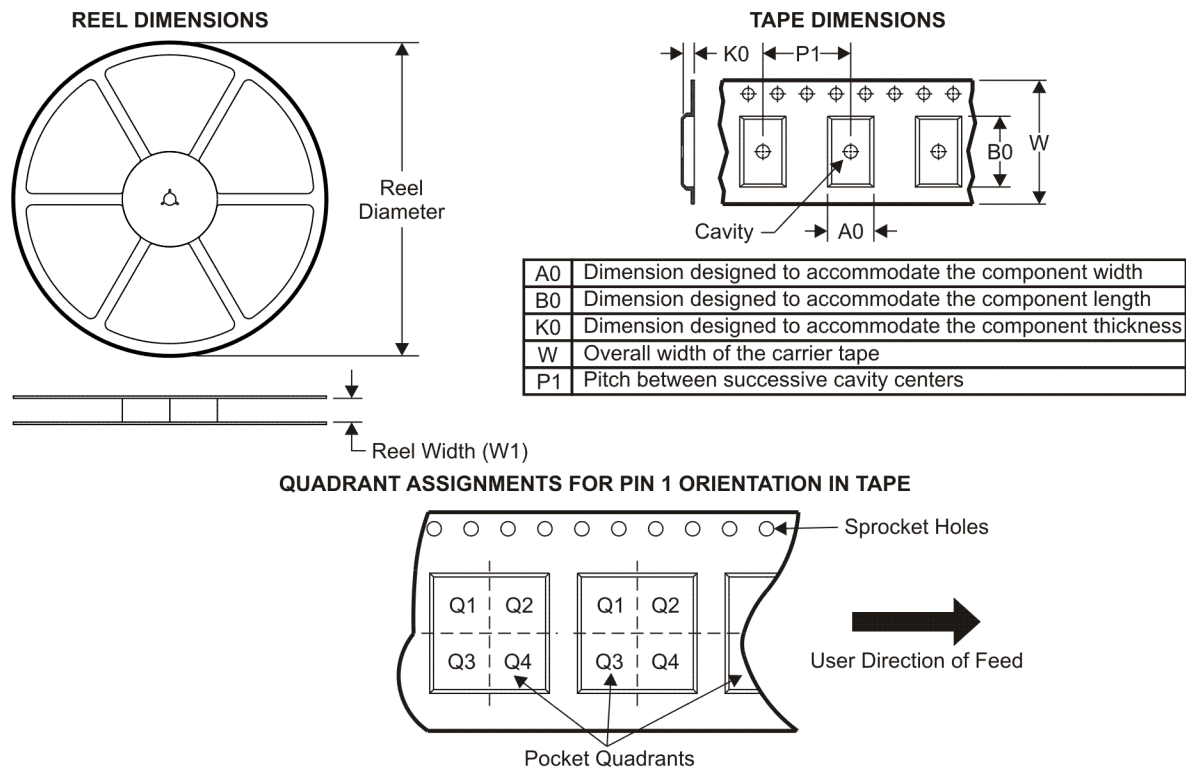
OTHER QUALIFIED VERSIONS OF INA148-Q1 :

- Catalog: [INA148](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA148QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

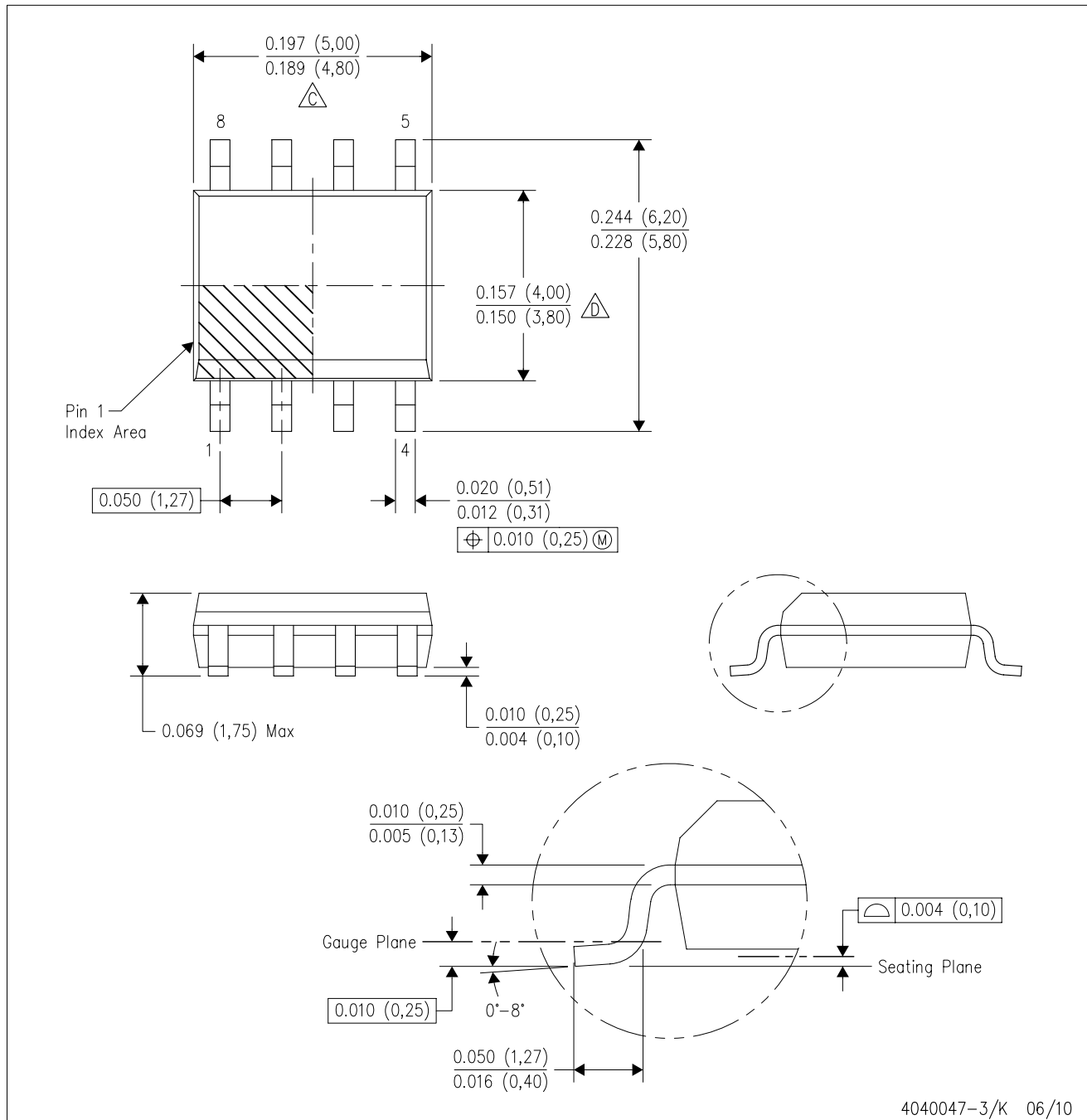


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA148QDRQ1 | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

D (R-PDSO-G8)

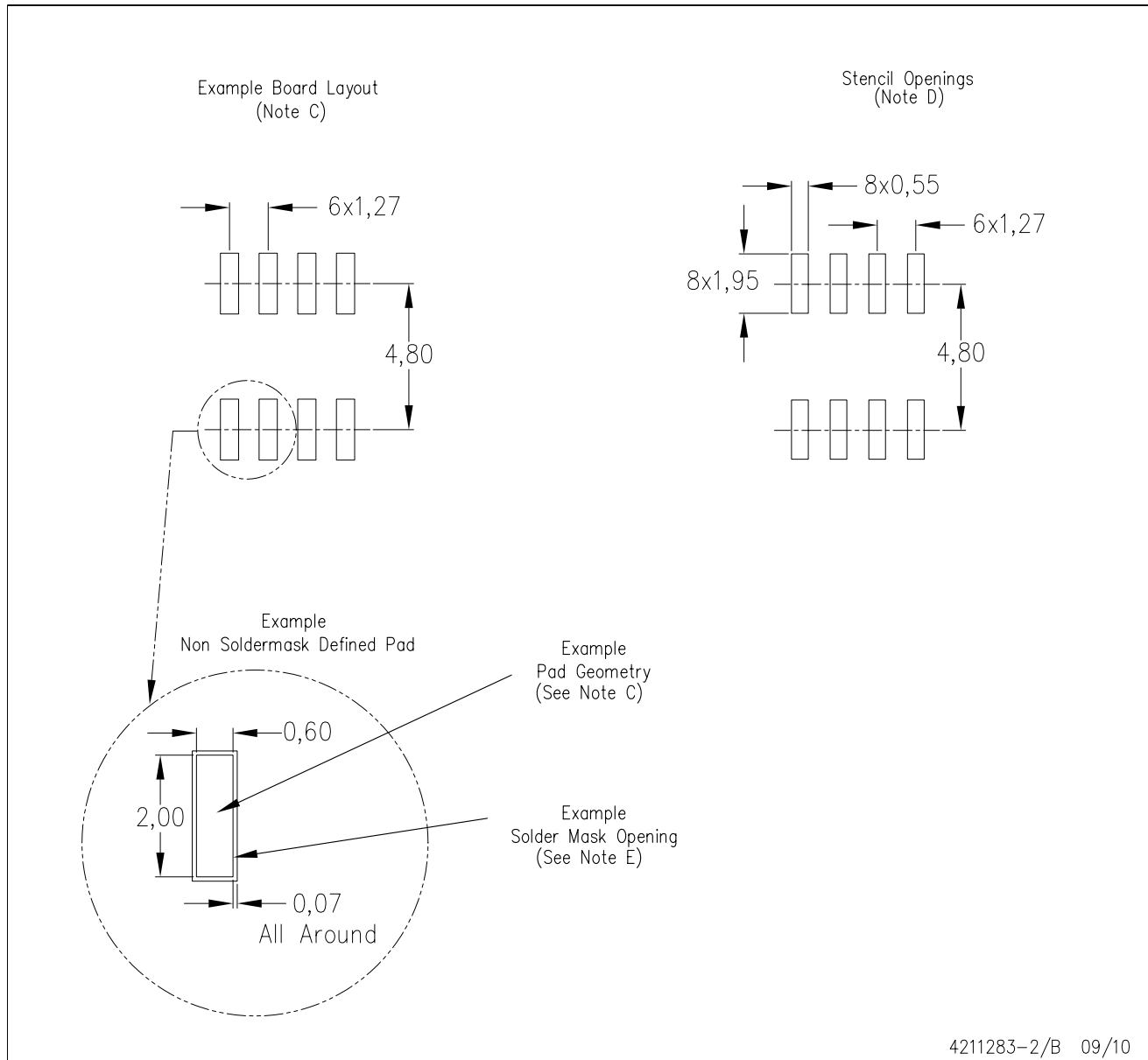
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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