

ADC1215S series

Single 12-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps with input buffer; CMOS or LVDS DDR digital outputs

Rev. 01 — 12 April 2010

Preliminary data sheet

1. General description

The ADC1215S is a single channel 12-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performances and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1215S is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, thanks to a separate digital output supply.

The ADC1215S supports the Low Voltage Differential Signalling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC.

The device also includes a SPI programmable full-scale to allow flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1215S is ideal for use in communications, imaging and medical applications - especially in high Intermediate Frequency (IF) applications thanks to the integrated input buffer. The input buffer ensures that the input impedance remains constant and low and the performance consistent over a wide frequency range.

2. Features and benefits

- SNR, 70 dBFS / SFDR, 86 dBc
- Sample rate up to 125 Msps
- 12-bit pipelined ADC core
- Clock input divider by 2 for less jitter contribution
- Integrated input buffer
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- Pin compatible with the ADC1415S series, the ADC1015S series and the ADC1115S125
- HVQFN40 package
- Input bandwidth, 600 MHz
- Power dissipation, 635 mW at 80 Msps, including analog input buffer
- SPI
- Duty cycle stabilizer
- Fast Out of Range (OTR) detection
- INL r 1.25 LSB, DNL r 0.25 LSB
- Offset binary, two's complement, gray code
- Power-down and Sleep modes



3. Applications

- Wireless and wired broadband communications
- Portable instrumentation
- Imaging systems
- Digital predistortion loop, power amplifier linearization
- Spectral analysis
- Ultrasound equipment
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	f _s (Msps)	Package		
		Name	Description	Version
ADC1215S125HN/C1	125	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 u 6 u 0.85 mm	SOT618-6
ADC1215S105HN/C1	105	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 u 6 u 0.85 mm	SOT618-6
ADC1215S080HN/C1	80	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 u 6 u 0.85 mm	SOT618-6
ADC1215S065HN/C1	65	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 u 6 u 0.85 mm	SOT618-6

5. Block diagram

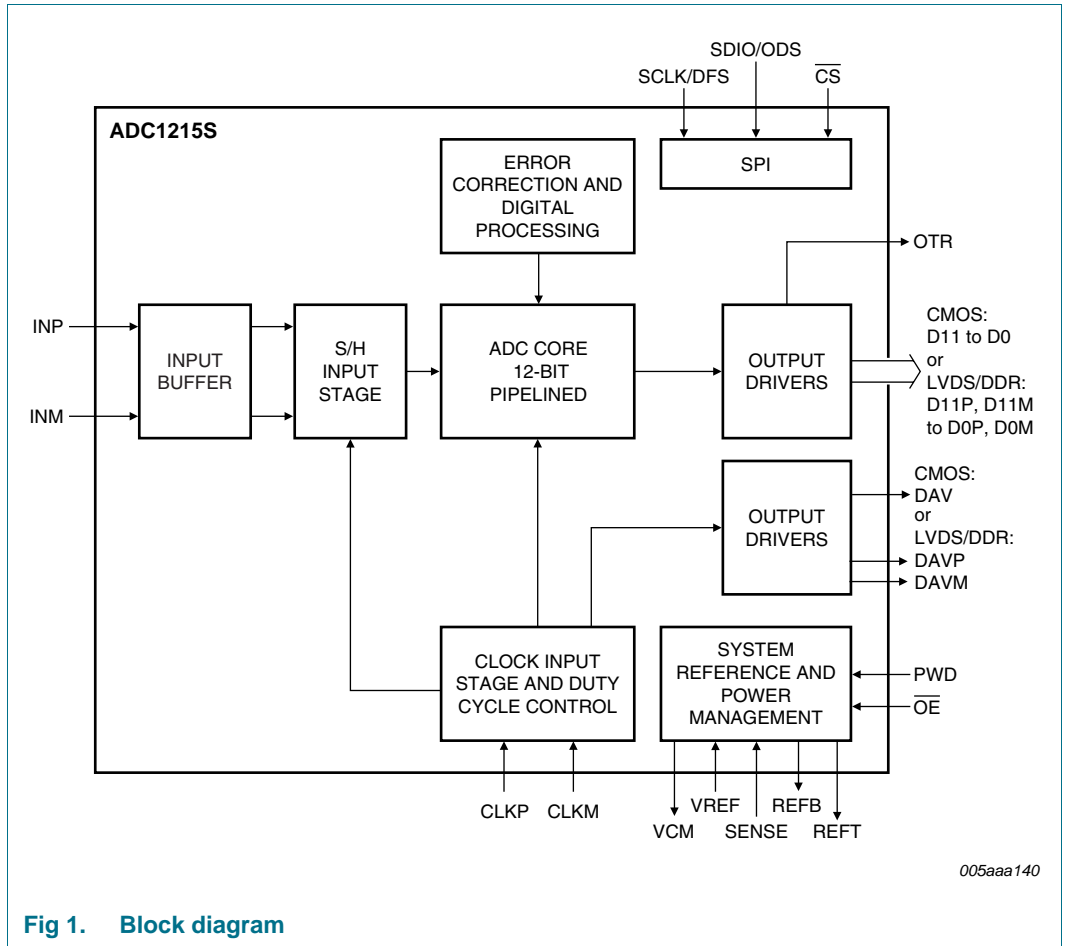


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

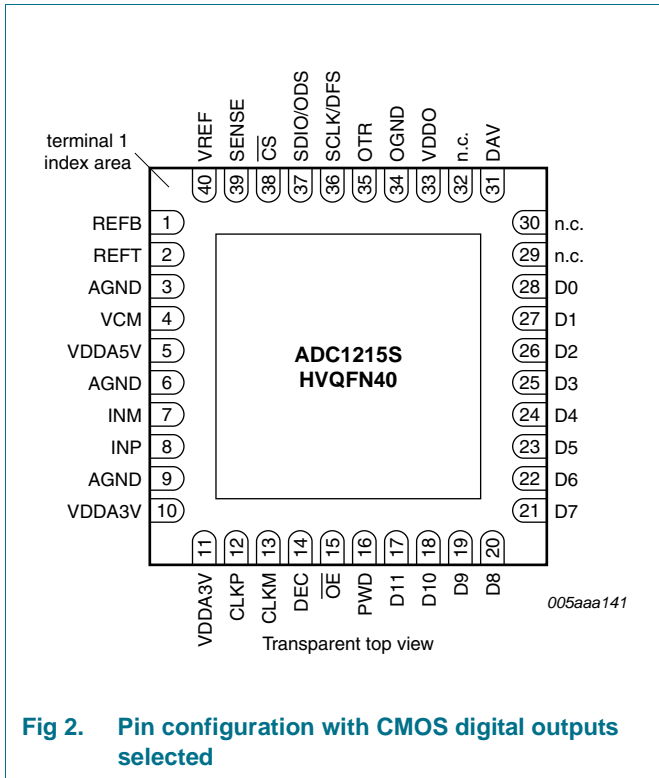


Fig 2. Pin configuration with CMOS digital outputs selected

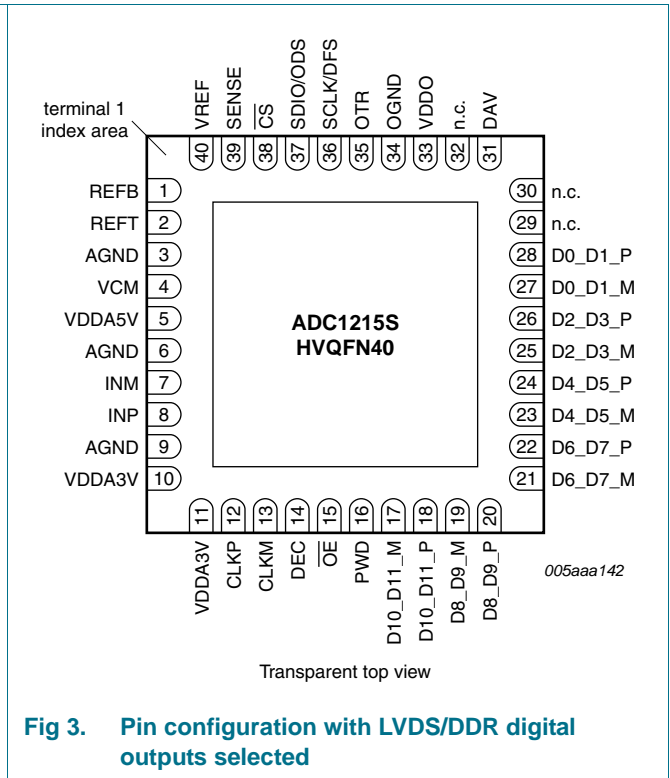


Fig 3. Pin configuration with LVDS/DDR digital outputs selected

6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type ^[1]	Description
REFB	1	O	bottom reference
REFT	2	O	top reference
AGND	3	G	analog ground
VCM	4	O	common-mode output voltage
VDDA5V	5	P	5 V analog power supply
AGND	6	G	analog ground
INM	7	I	complementary analog input
INP	8	I	analog input
AGND	9	G	analog ground
VDDA3V	10	P	3 V analog power supply
VDDA3V	11	P	3 V analog power supply
CLKP	12	I	clock input
CLKM	13	I	complementary clock input
DEC	14	O	regulator decoupling node
\overline{OE}	15	I	output enable, active LOW
PWD	16	I	power down, active HIGH

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type ^[1]	Description
D11	17	O	data output bit 11 (MSB)
D10	18	O	data output bit 10
D9	19	O	data output bit 9
D8	20	O	data output bit 8
D7	21	O	data output bit 7
D6	22	O	data output bit 6
D5	23	O	data output bit 5
D4	24	O	data output bit 4
D3	25	O	data output bit 3
D2	26	O	data output bit 2
D1	27	O	data output bit 1
D0	28	O	data output bit 0 (LSB)
n.c.	29	-	not connected
n.c.	30	-	not connected
DAV	31	O	data valid output clock
n.c.	32	-	not connected
VDDO	33	P	output power supply
OGND	34	G	output ground
OTR	35	O	out of range
SCLK/DFS	36	I	SPI clock / data format select
SDIO/ODS	37	I/O	SPI data IO / output data standard
$\overline{\text{CS}}$	38	I	SPI chip select
SENSE	39	I	reference programming pin
VREF	40	I/O	voltage reference input/output

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

Table 3. Pin description (LVDS/DDR) digital outputs)

Symbol	Pin ^[1]	Type ^[2]	Description
D10_D11_M	17	O	differential output data D10 and D11 multiplexed, complement
D10_D11_P	18	O	differential output data D10 and D11 multiplexed, true
D8_D9_M	19	O	differential output data D8 and D9 multiplexed, complement
D8_D9_P	20	O	differential output data D8 and D9 multiplexed, true
D6_D7_M	21	O	differential output data D6 and D7 multiplexed, complement
D6_D7_P	22	O	differential output data D6 and D7 multiplexed, true
D4_D5_M	23	O	differential output data D4 and D5 multiplexed, complement
D4_D5_P	24	O	differential output data D4 and D5 multiplexed, true
D2_D3_M	25	O	differential output data D2 and D3 multiplexed, complement
D2_D3_P	26	O	differential output data D2 and D3 multiplexed, true
D0_D1_M	27	O	differential output data D0 and D1 multiplexed, complement
D0_D1_P	28	O	differential output data D0 and D1 multiplexed, true
n.c.	29	-	not connected

Table 3. Pin description ...continued (LVDS/DDR) digital outputs

Symbol	Pin ^[1]	Type ^[2]	Description
n.c.	30	-	not connected
DAVM	31	O	data valid output clock, complement
DAVP	32	O	data valid output clock, true

[1] Pins 1 to 16 and pins 33 to 40 are the same for both CMOS and LVDS DDR outputs (see [Table 2](#))

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage	pins D11 to D0 or pins D11P to D0P and D11M to D0M	0.4	+3.9	V
$V_{DDA(3V)}$	analog supply voltage 3 V	on pin VDDA3V	0.5	+4.6	V
$V_{DDA(5V)}$	analog supply voltage 5 V	on pin VDDA5V	0.5	+6.0	V
V_{DDO}	output supply voltage		0.5	+4.6	V
V_{CC}	supply voltage difference	$V_{DDA(3V)}$ V_{DDO}	<tbd>	<tbd>	V
T_{stg}	storage temperature		55	+125	°C
T_{amb}	ambient temperature		40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] 30.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1] 13.3	K/W

[1] Value for 6 layers board in still air with a minimum of 25 thermal vias.

9. Static characteristics

Table 6. Static characteristics^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDA(5V)}$	analog supply voltage 5 V		4.75	5.0	5.25	V
$V_{DDA(3V)}$	analog supply voltage 3 V		2.85	3.0	3.4	V
V_{DDO}	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
$I_{DDA(5V)}$	analog supply current 5 V	$f_{clk} = 125$ Msps; $f_i = 70$ MHz	-	46	-	mA
$I_{DDA(3V)}$	analog supply current 3 V	$f_{clk} = 125$ Msps; $f_i = 70$ MHz	-	205	-	mA
I_{DDO}	output supply current	CMOS mode; $f_{clk} = 125$ Msps; $f_i = 70$ MHz	-	12	-	mA
		LVDS DDR mode: $f_{clk} = 125$ Msps; $f_i = 70$ MHz	-	39	-	mA
P	power dissipation	ADC1215S125; analog supply only	-	840	-	mW
		ADC1215S105; analog supply only	-	770	-	mW
		ADC1215S080; analog supply only	-	635	-	mW
		ADC1215S065; analog supply only	-	580	-	mW
		Power-down mode	-	2	-	mW
		Standby mode	-	40	-	mW
Clock inputs: pins CLKP and CLKM						
LVPECL						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	r 1.6	-	V
LVDS						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	r 0.70	-	V
SINE wave						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	r 0.8	r 3.0	-	V
LVC MOS						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA(3V)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA(3V)}$	-	-	V
Logic inputs: pins PWD and OE						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	$V_{DDA(3V)}$	V
I_{IL}	LOW-level input current		<tbid>	-	<tbid>	PA
I_{IH}	HIGH-level input current		10	-	+10	PA

Table 6. Static characteristics^[1] ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface: pins CS, SDIO/ODS, SCLK/DFS						
V _{IL}	LOW-level input voltage		0	-	0.3V _{DDA(3V)}	V
V _{IH}	HIGH-level input voltage		0.7V _{DDA(3V)}	-	V _{DDA(3V)}	V
I _{IL}	LOW-level input current		10	-	+10	PA
I _{IH}	HIGH-level input current		50	-	+50	PA
C _i	input capacitance		-	4	-	pF
Digital outputs, CMOS mode: pins D11 to D0, OTR, DAV						
Output levels, V _{DDO} = 3 V						
V _{OL}	LOW-level output voltage	I _{OL} = <tbid>	OGND	-	0.2V _{DDO}	V
V _{OH}	HIGH-level output voltage	I _{OH} = <tbid>	0.8V _{DDO}	-	V _{DDO}	V
I _{OL}	LOW-level output current	3-state; output level = 0 V	-	<tbid>	-	PA
I _{OH}	HIGH-level output current	3-state; output level = V _{DDA(3V)}	-	<tbid>	-	PA
C _O	output capacitance	high impedance; OE = HIGH	-	3	-	pF
Output levels, V _{DDO} = 1.8 V						
V _{OL}	LOW-level output voltage	I _{OL} = <tbid>	OGND	-	0.2V _{DDO}	V
V _{OH}	HIGH-level output voltage	I _{OH} = <tbid>	0.8V _{DDO}	-	V _{DDO}	V
Digital outputs, LVDS mode: pins D11P to D0P, D11M to D0M, DAVP and DAVM						
Output levels, V _{DDO} = 3 V only, R _{load} = 100 :						
V _{O(offset)}	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V
V _{O(dif)}	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
C _O	output capacitance		-	<tbid>	-	pF
Analog inputs: pins INP and INM						
I _I	input current		5	-	+5	PA
R _I	input resistance		-	550	-	:
C _I	input capacitance		-	1.3	-	pF
V _{I(cm)}	common-mode input voltage	V _{INP} = V _{INM}	0.9	1.5	2	V
B _i	input bandwidth		-	600	-	MHz
V _{I(dif)}	differential input voltage	peak-to-peak	1		2	V
Common mode output voltage: pin VCM						
V _{O(cm)}	common-mode output voltage		-	0.5V _{DDA(3V)}	-	V
I _{O(cm)}	common-mode output current		-	<tbid>	-	PA
I/O reference voltage: pin VREF						
V _{VREF}	voltage on pin VREF	output	-	0.5 to 1	-	V
		input	0.5	-	1	V

Table 6. Static characteristics^[1] ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy						
INL	integral non-linearity		1.25	r 0.25	+1.25	LSB
DNL	differential non-linearity	guaranteed no missing codes	0.25	r 0.12	+0.25	LSB
E_{offset}	offset error		-	r 2	-	mV
E_G	gain error		-	r 0.5	-	%FS
Supply						
PSRR	power supply rejection ratio	100 mV (p-p) on $V_{\text{DDA}(3V)}$	-	35	-	dBc

[1] Typical values measured at $V_{\text{DDA}(3V)} = 3\text{ V}$, $V_{\text{DDO}} = 1.8\text{ V}$, $V_{\text{DDA}(5V)} = 5\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ and $C_L = 5\text{ pF}$; minimum and maximum values are across the full temperature range $T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ at $V_{\text{DDA}(3V)} = 3\text{ V}$, $V_{\text{DDO}} = 1.8\text{ V}$, $V_{\text{DDA}(5V)} = 5\text{ V}$, $V_{\text{INP}} = V_{\text{INM}} = 1\text{ dBFS}$; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 7. Dynamic characteristics [1]

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog signal processing															
D _{2H}	second harmonic level	f _i = 3 MHz	-	87	-	-	87	-	-	86	-	-	88	-	dBc
		f _i = 30 MHz	-	86	-	-	86	-	-	86	-	-	87	-	dBc
D _{3H}		f _i = 70 MHz	-	85	-	-	85	-	-	84	-	-	85	-	dBc
		f _i = 170 MHz	-	82	-	-	82	-	-	81	-	-	83	-	dBc
	third harmonic level	f _i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f _i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
THD		f _i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f _i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc
	total harmonic distortion	f _i = 3 MHz	-	85	-	-	85	-	-	84	-	-	86	-	dBc
		f _i = 30 MHz	-	84	-	-	84	-	-	84	-	-	85	-	dBc
ENOB		f _i = 70 MHz	-	83	-	-	83	-	-	82	-	-	83	-	dBc
		f _i = 170 MHz	-	80	-	-	80	-	-	79	-	-	81	-	dBc
	effective number of bits	f _i = 3 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.3	-	bits
		f _i = 30 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.2	-	bits
SNR		f _i = 70 MHz	-	11.2	-	-	11.2	-	-	11.2	-	-	11.2	-	bits
		f _i = 170 MHz	-	11.1	-	-	11.1	-	-	11.1	-	-	11.1	-	bits
	signal-to-noise ratio	f _i = 3 MHz	-	70.0	-	-	69.9	-	-	69.8	-	-	69.6	-	dBFS
		f _i = 30 MHz	-	69.5	-	-	69.5	-	-	69.5	-	-	69.4	-	dBFS
SFDR		f _i = 70 MHz	-	69.2	-	-	69.2	-	-	69.1	-	-	69.0	-	dBFS
		f _i = 170 MHz	-	68.8	-	-	68.8	-	-	68.7	-	-	68.6	-	dBFS
	spurious-free dynamic range	f _i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f _i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
SFDR		f _i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f _i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc

Table 7. Dynamic characteristics [1] ... continued

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD	Intermodulation distortion	$f_i = 3 \text{ MHz}$	-	89	-	-	89	-	-	88	-	-	89	-	dBc
		$f_i = 30 \text{ MHz}$	-	88	-	-	88	-	-	88	-	-	88	-	dBc
		$f_i = 70 \text{ MHz}$	-	87	-	-	87	-	-	86	-	-	86	-	dBc
		$f_i = 170 \text{ MHz}$	-	84	-	-	85	-	-	83	-	-	84	-	dBc

[1] Typical values measured at $V_{DDA(3V)} = 3 \text{ V}$, $V_{DDO} = 1.8 \text{ V}$, $V_{DDA(5V)} = 5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $C_L = 5 \text{ pF}$; minimum and maximum values are across the full temperature range $T_{\text{amb}} = 40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$ at $V_{DDA(3V)} = 3 \text{ V}$, $V_{bDO} = 1.8 \text{ V}$, $V_{DDA(5V)} = 5 \text{ V}$; $V_{\text{INP}} = 1 \text{ dBFS}$; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

10.2 Clock and digital output timing

Table 8. Clock and digital output timing characteristics^[1]

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock timing input: pins CLKP and CLKM															
f_{clk}	clock frequency		20	-	65	60	-	80	75	-	105	100	-	125	MHz
$t_{lat(data)}$	data latency time		-	14	-	-	14	-	-	14	-	-	14	-	clocks cycle
G_{clk}	clock duty cycle	DCS_EN = 1	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = 0	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
t_{wake}	wake-up time		-	<tbd>	-	-	<tbd>	-	-	<tbd>	-	-	<tbd>	-	ns
CMOS mode timing output: pins D11 to D0 and DAV															
t_{PD}	propagation delay	DATA	-	3.9	-	-	3.9	-	-	3.9	-	-	3.9	-	ns
		DAV	-	4.2	-	-	4.2	-	-	4.2	-	-	4.2	-	ns
t_{su}	set-up time		-	7.7	-	-	6.5	-	-	4.7	-	-	4.3	-	ns
t_h	hold time		-	6.7	-	-	5.5	-	-	3.8	-	-	3.5	-	ns
t_r	rise time ^[2]	DATA	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
		DAV	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
t_f	fall time ^[2]	DATA	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns

Table 8. Clock and digital output timing characteristics^[1] ...continued

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LVDS DDR mode timing output: pins D11P to D0P, D11M to D0M, DAVP and DAVM															
t_{pD}	propagation delay	DATA DAV	-	3.9	-	-	3.9	-	-	3.9	-	-	3.9	-	ns
t_{su}	set-up time		-	5.1	-	-	3.5	-	-	2.1	-	-	1.4	-	ns
t_h	hold time		-	2.0	-	-	2.0	-	-	2.0	-	-	2.0	-	ns
t_r	rise time ^[3]	DATA DAV	50	100	200	50	100	200	50	100	200	50	100	200	ps
t_f	fall time ^[3]	DATA DAV	50	100	200	50	100	200	50	100	200	50	100	200	ps

[1] Typical values measured at $V_{DDA(3V)} = 3\text{ V}$, $V_{DDO} = 1.8\text{ V}$, $V_{DDA(5V)} = 5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$ and $C_L = 5\text{ pF}$; minimum and maximum values are across the full temperature range $T_{amb} = 40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ at $V_{DDA(3V)} = 3\text{ V}$, $V_{DDO} = 1.8\text{ V}$, $V_{DDA(5V)} = 5\text{ V}$, $V_{INP} = 1\text{ dBFS}$; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of V_{DDO} .

[3] Rise time measured from 50 mV to +50 mV; fall time measured from +50 mV to 50 mV.

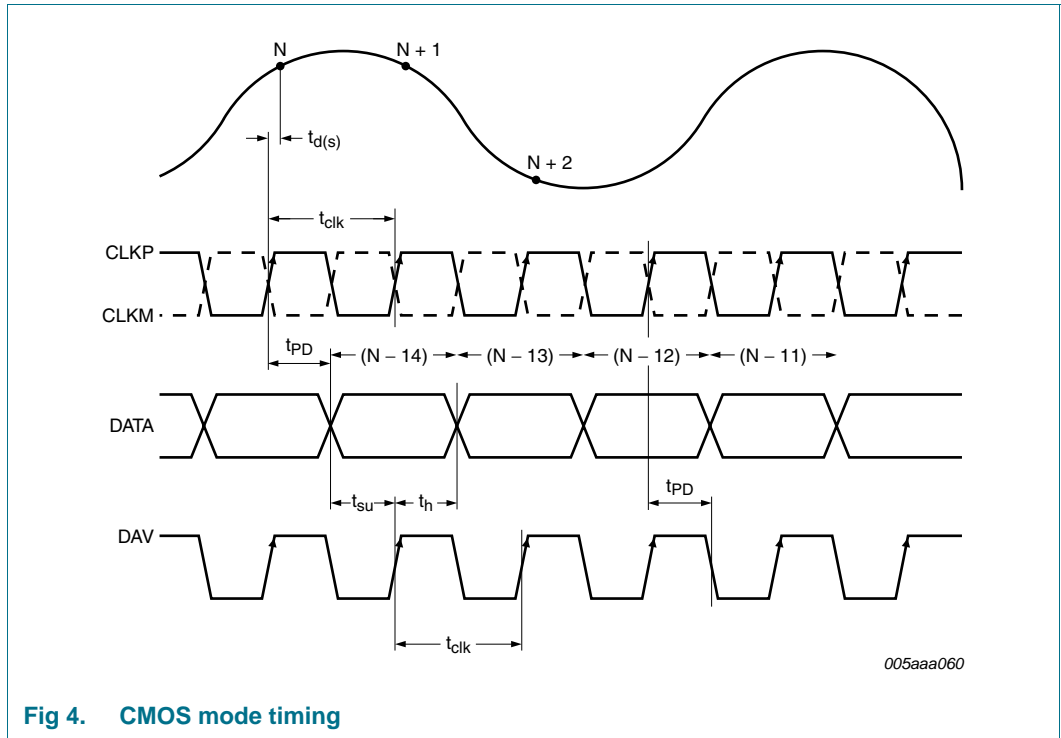


Fig 4. CMOS mode timing

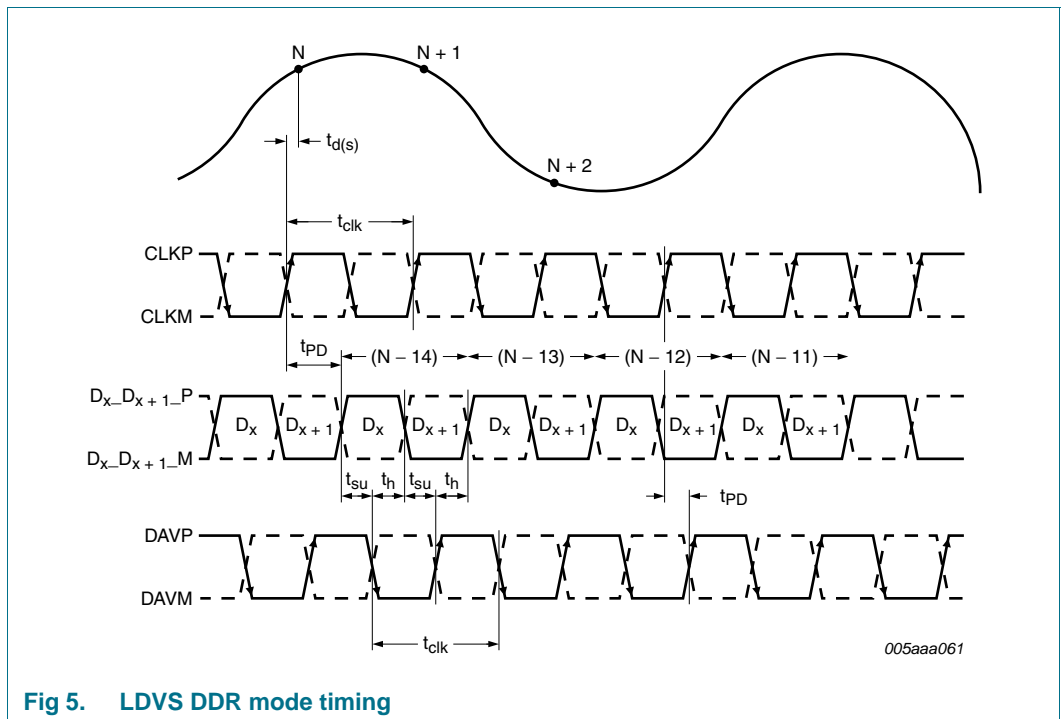


Fig 5. LVDS DDR mode timing

10.3 SPI timings

Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI timings						
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK pulse width HIGH		16	-	-	ns
$t_{w(SCLKL)}$	SCLK pulse width LOW		16	-	-	ns
t_{su}	set-up time	data to SCLKH	5	-	-	ns
		\overline{CS} to SCLKH	5	-	-	ns
t_h	hold time	data to SCLKH	2	-	-	ns
		\overline{CS} to SCLKH	2	-	-	ns
$f_{clk(max)}$	maximum clock frequency		-	-	25	MHz

[1] Typical values measured at $V_{DDA(3V)} = 3\text{ V}$, $V_{DDO} = 1.8\text{ V}$, $V_{DDA(5V)} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $C_L = 5\text{ pF}$; minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ at $V_{DDA(3V)} = 3\text{ V}$, $V_{DDO} = 1.8\text{ V}$, $V_{DDA(5V)} = 5\text{ V}$, $V_{INP} = V_{INM} = 1\text{ dBFS}$; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified

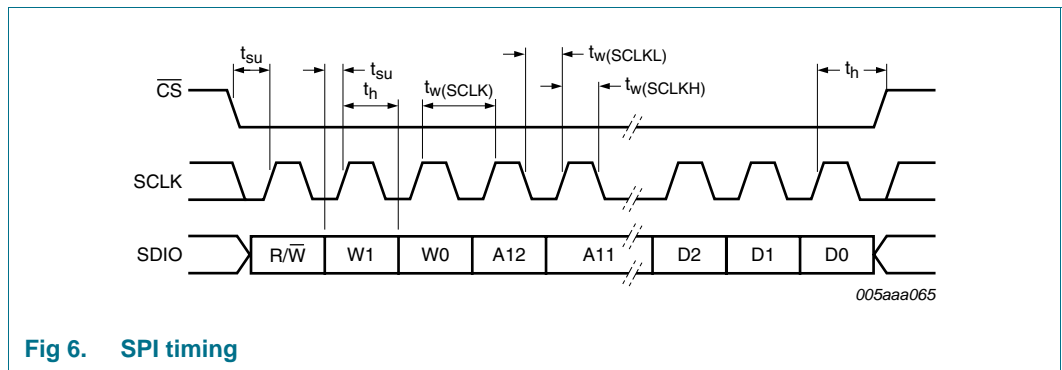


Fig 6. SPI timing

11. Application information

11.1 Device control

The ADC1215S can be controlled via the Serial Peripheral Interface (SPI control mode) or directly via the I/O pins (Pin control mode).

11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin \overline{CS} is held HIGH. In Pin control mode, the SPI pins SDIO, \overline{CS} and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin \overline{CS} LOW. Once SPI control mode has been enabled, the device will remain in this mode. The transition from Pin control mode to SPI control mode is illustrated in [Figure 7](#).

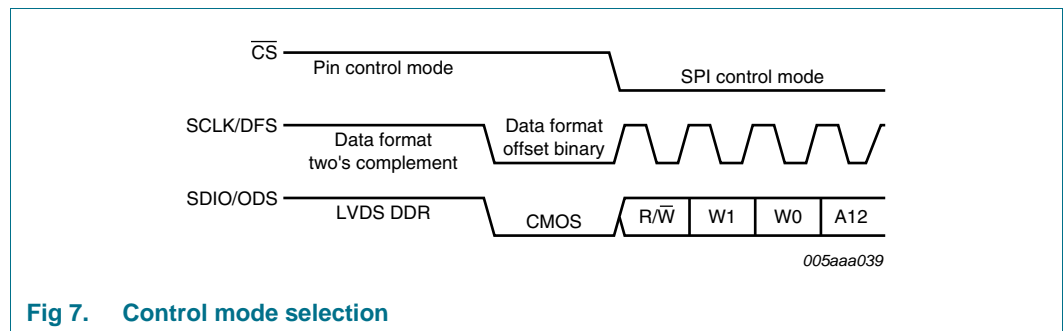


Fig 7. Control mode selection

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO as soon as a transition is triggered by a falling edge on \overline{CS} .

11.1.2 Operating mode selection

The active ADC1215S operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see [Figure 18](#)) or using pins PWD and \overline{OE} in Pin control mode, as described in [Table 10](#).

Table 10. Operating mode selection via pin PWD and \overline{OE}

Pin PWD	Pin \overline{OE}	Operating mode	Output high-Z
0	0	Power-up	no
0	1	Power-up	yes
1	0	Sleep	yes
1	1	Power-down	yes

11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see [Table 23](#)) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see [Table 23](#)) or using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1215S supports differential or single-ended input drive. Optimal performance is achieved using differential inputs. The ADC inputs are internally biased and need to be decoupled.

The full scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see [Section 11.3](#) and [Table 21](#) further details).

The equivalent circuit of the input buffer followed by the Sample and Hold (S/H) input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in [Figure 8](#).

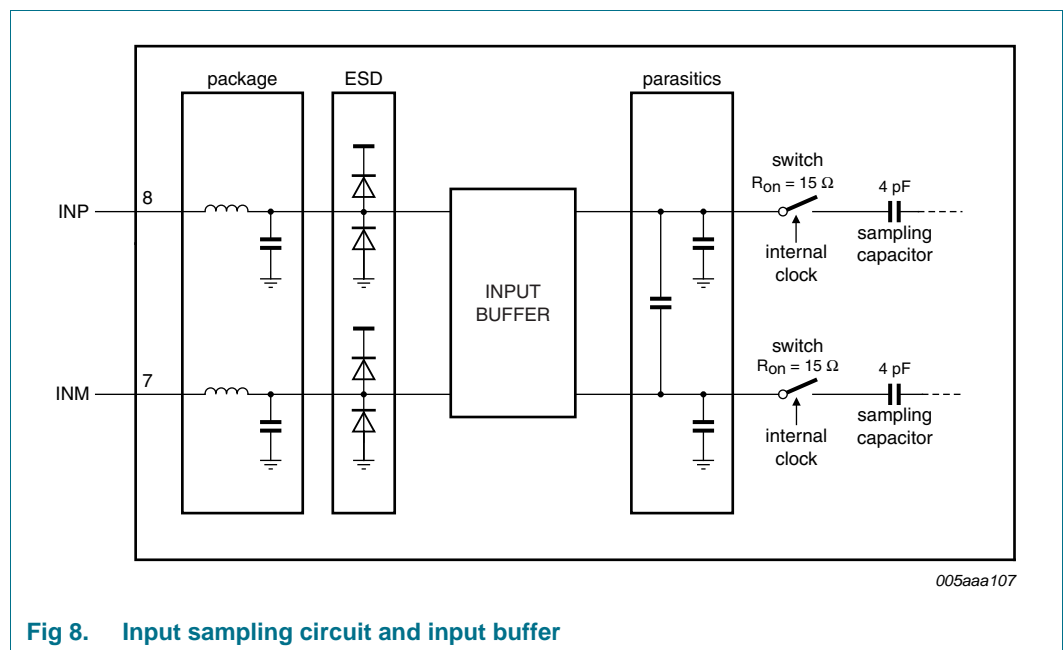


Fig 8. Input sampling circuit and input buffer

The integrated input buffer offers the following advantages:

- The kickback effect is avoided - the charge injection and glitches generated by the S/H input stage are isolated from the input circuitry. So there's no need for additional filtering.
- The input capacitance is very low and constant over a wide frequency range, which makes the ADC1215S easy to drive.

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.2.2 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in [Figure 9](#) would be suitable for a baseband application.

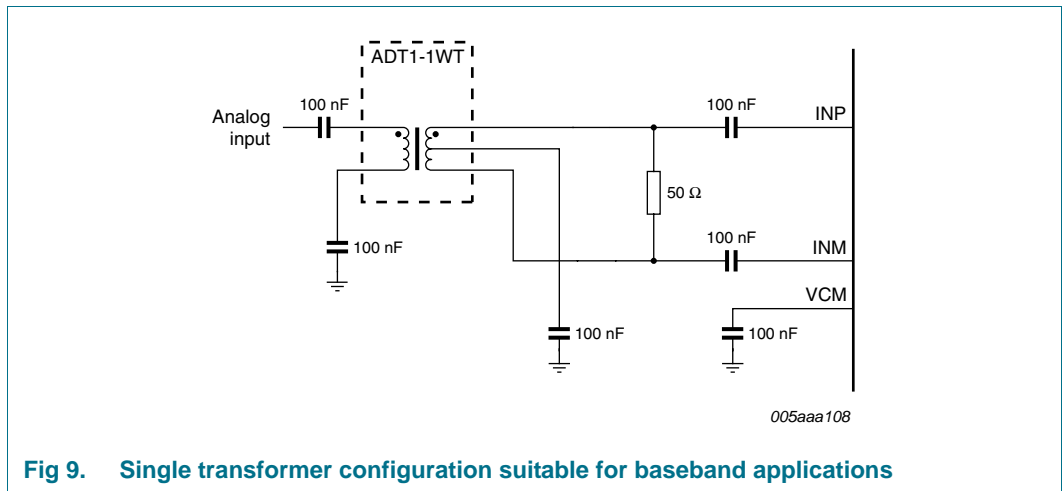


Fig 9. Single transformer configuration suitable for baseband applications

The configuration shown in [Figure 10](#) is recommended for high frequency applications. In both cases, the choice of transformer will be a compromise between cost and performance.

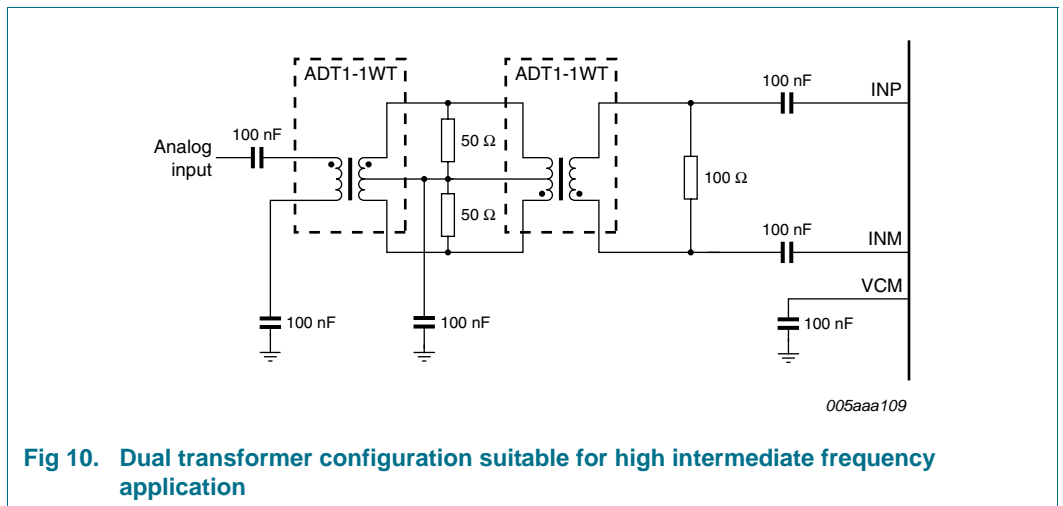


Fig 10. Dual transformer configuration suitable for high intermediate frequency application

11.3 System reference and power management

11.3.1 Internal/external references

The ADC1215S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and 6 dB via control bits INTREF[2:0] when bit INTREF_EN = 1; see Table 21). See Figure 12, Figure 13, Figure 14 and Figure 15. The equivalent reference circuit is shown in Figure 11. External reference is also possible by providing a voltage on pin VREF as described in Figure 14.

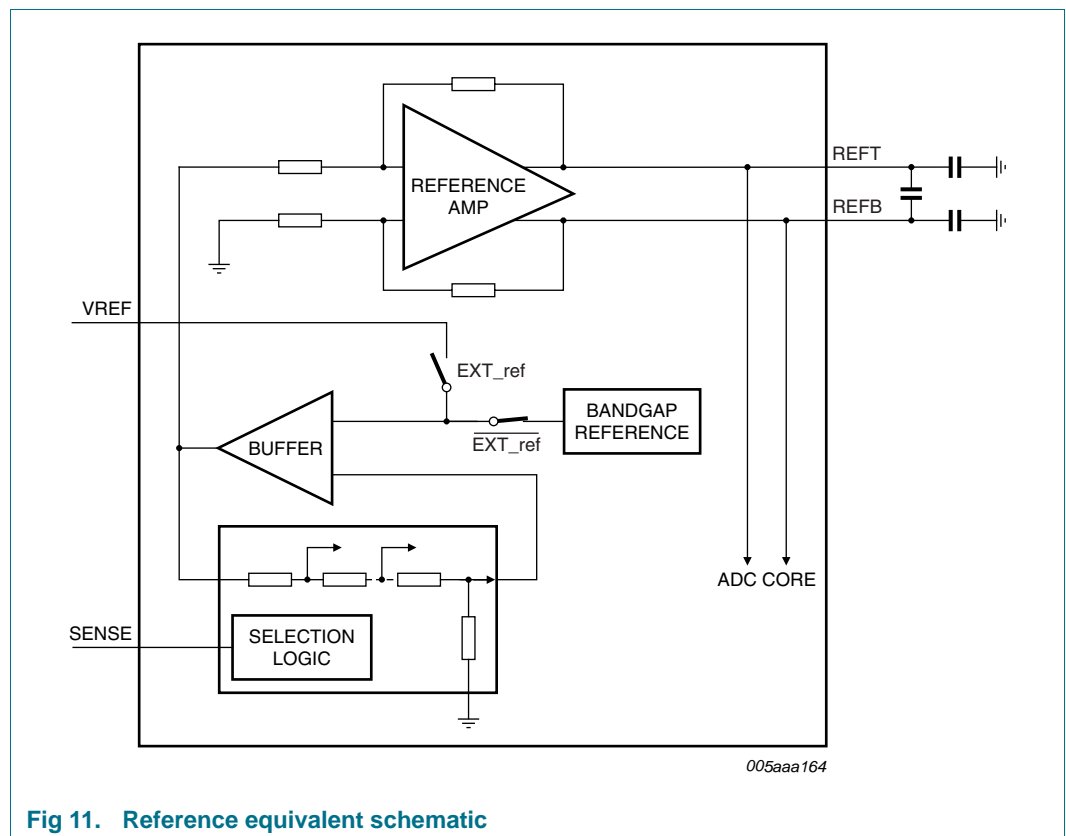


Fig 11. Reference equivalent schematic

If bit INTREF_EN is set to 0, the reference voltage will be determined either internally or externally as detailed in Table 11.

Table 11. Reference selection

Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	full scale (p-p)
internal (Figure 12)	0	AGND	330 pF capacitor to AGND	2 V
internal (Figure 13)	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
external (Figure 14)	0	V _{DDA(3V)}	external voltage between 0.5 V and 1 V ^[1]	1 V to 2 V
internal via SPI (Figure 15)	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

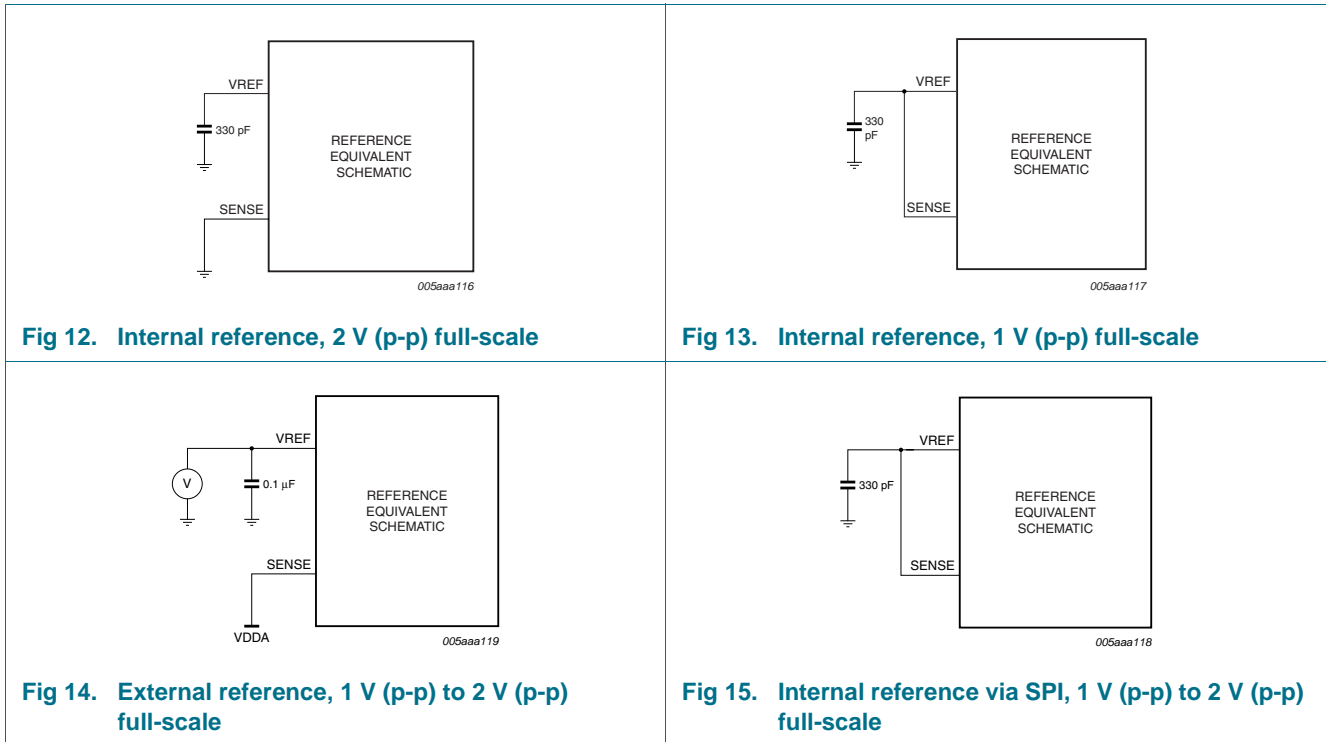


Figure 12 to Figure 15 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

11.3.2 Reference gain control

The reference gain is programmable between 0 dB to 6 dB in 1 dB steps via the SPI (see Table 21). The corresponding full-scale input voltage range varies between 2 V (p-p) and 1 V (p-p), as shown in Table 12:

Table 12. Reference SPI Gain Control

INTREF	Gain	full scale (p-p)
000	0 dB	2 V
001	1 dB	1.78 V
010	2 dB	1.59 V
011	3 dB	1.42 V
100	4 dB	1.26 V
101	5 dB	1.12 V
110	6 dB	1 V
111	reserved	x

11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 PF filter capacitor should be connected between pin VCM and ground.

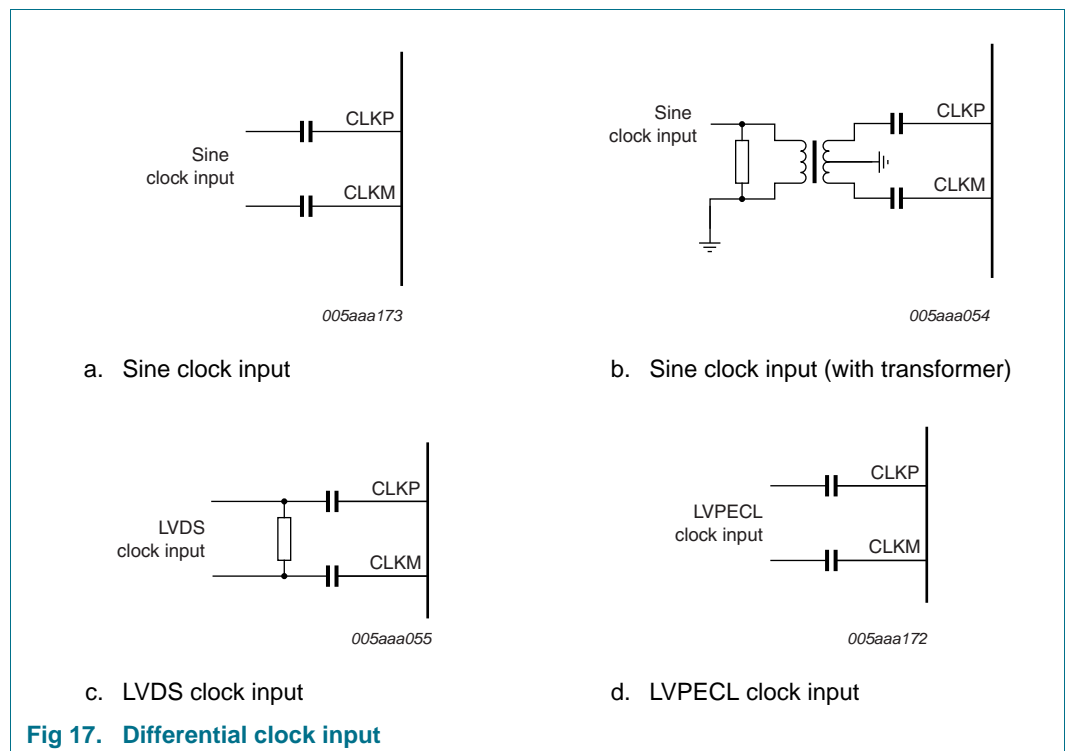
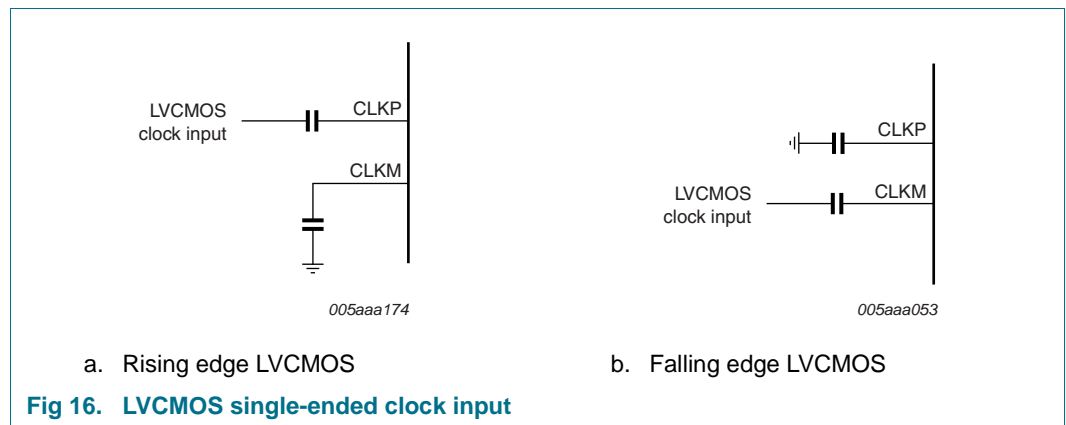
11.3.4 Biasing

The common-mode input voltage ($V_{I(cm)}$) on pins INP and INM is set internally. The input buffer bias current can be set to one of three levels (high, medium or low) via the SPI (see [Table 22](#)).

11.4 Clock input

11.4.1 Drive modes

The ADC1215S can be driven differentially (SINE, LVPECL or LVDS) with little or no degradation on dynamic performances. It can also be driven by a single-ended LVC MOS signal connected to pin CLKP (CLKM should be connected to ground via a capacitor) or CLKM (CLKP should be connected to ground via a capacitor).



11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in [Figure 18](#). The common-mode voltage of the differential input stage is set via internal 5 k Ω resistors.

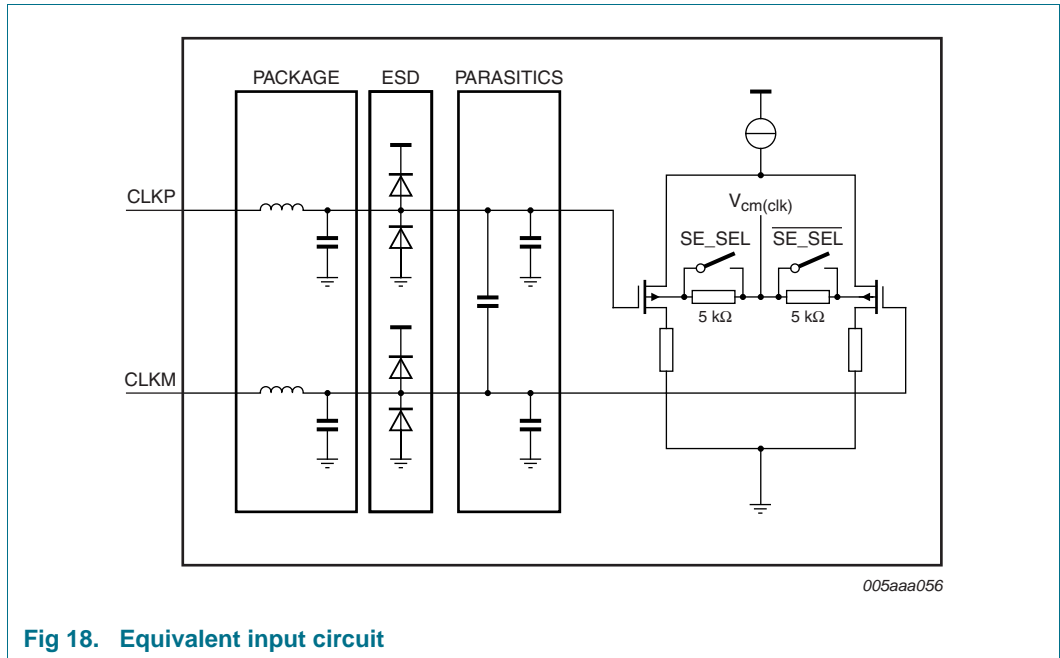


Fig 18. Equivalent input circuit

Single-ended or differential clock inputs can be selected via the SPI interface (see [Table 20](#)). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = 1; see [Table 20](#)), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = 0), the input clock signal should have a duty cycle of between 45% and 55%.

11.4.4 Clock input divider

The ADC1215S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = 1; see [Table 20](#)). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.5 Digital outputs

11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS/CMOS to 0 (see [Table 23](#)).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in [Figure 19](#). The buffer is powered by a separate OGND/V_{DDO} to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

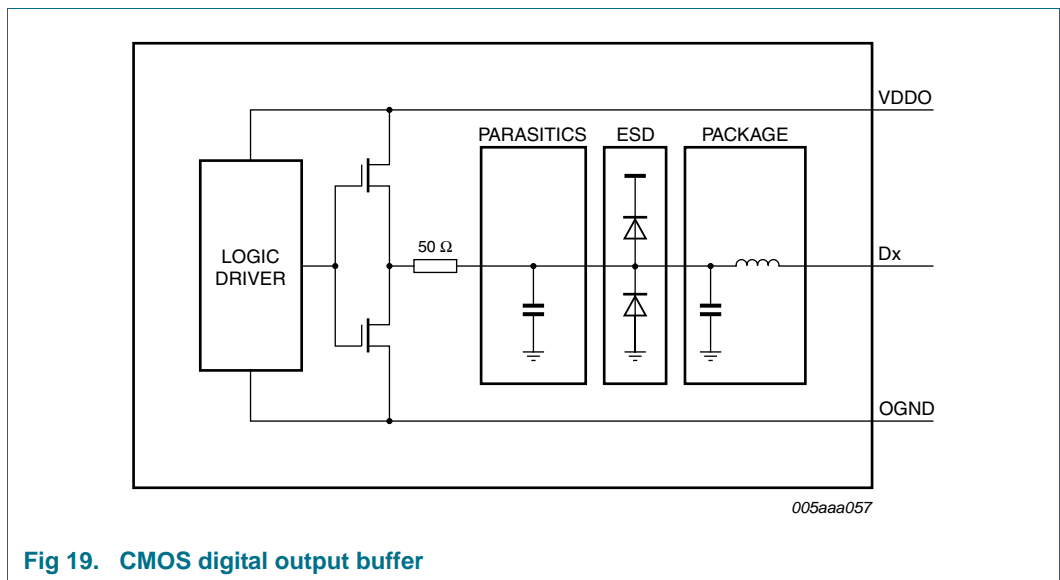


Fig 19. CMOS digital output buffer

The output resistance is 50 Ω and is the combination of the an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see [Table 30](#)):

11.5.2 Digital output buffers: LVDS DDR mode

The digital output buffers can be configured as LVDS DDR by setting bit LVDS/CMOS to 1 (see [Table 23](#)).

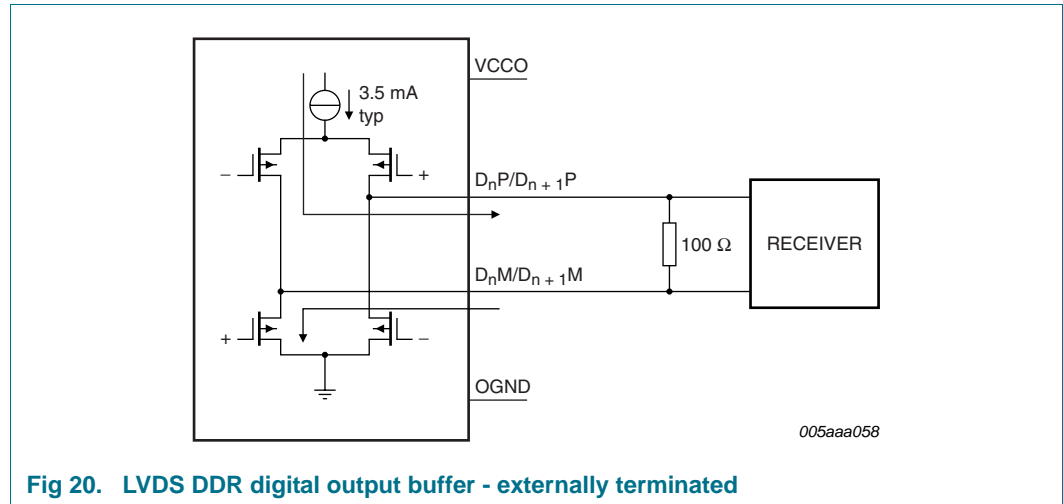


Fig 20. LVDS DDR digital output buffer - externally terminated

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side ([Figure 20](#)) or internally via SPI control bits LVDS_INT_TER[2:0] (see [Figure 21](#) and [Table 32](#)).

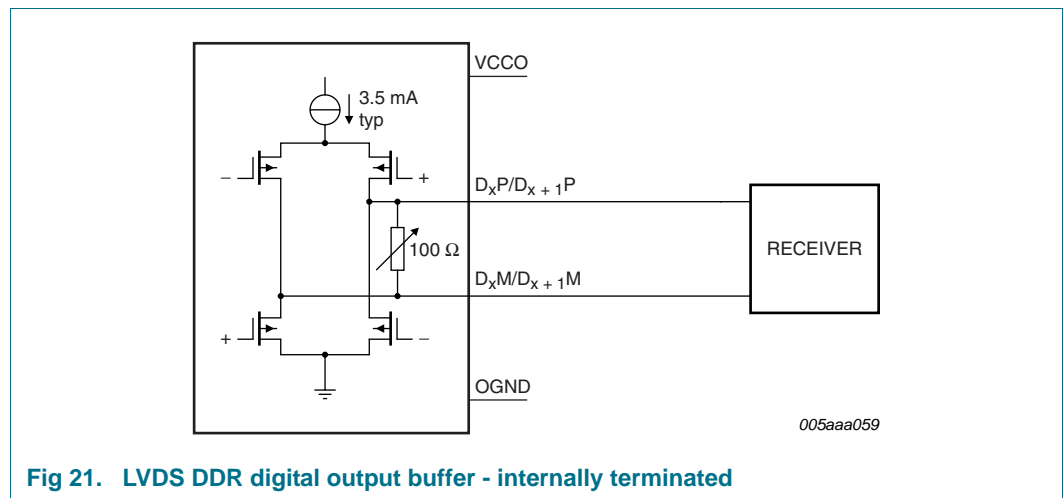


Fig 21. LVDS DDR digital output buffer - internally terminated

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see [Table 31](#)) in order to adjust the output logic voltage levels.

Table 13. LVDS DDR output register 2

LVDS_INT_TER[2:0]	Resistor value (Ω)
000	no internal termination
001	300
010	180
011	110
100	150

Table 13. LVDS DDR output register 2 ...continued

LVDS_INT_TER[2:0]	Resistor value (:)
101	100
110	81
111	60

11.5.3 Data valid (DAV) output clock

A data valid output clock signal (DAV) is provided that can be used to capture the data delivered by the ADC1215S. Detailed timing diagrams for CMOS and LVDS DDR modes are provided in [Figure 4](#) and [Figure 5](#) respectively.

11.5.4 Out-of-Range (OTR)

An out-of-range signal is provided on pin OTR. The latency of OTR is fourteen clock cycles. The OTR response can be speeded up by enabling Fast OTR (bit FASTOTR = 1; see [Table 29](#)). In this mode, the latency of OTR is reduced to only four clock cycles. The Fast OTR detection threshold (below full scale) can be programmed via bits FASTOTR_DET[2:0].

Table 14. Fast OTR register

FASTOTR_DET[2:0]	Detection level (dB)
000	20.56
001	16.12
010	11.02
011	7.82
100	5.49
101	3.66
110	2.14
111	0.86

11.5.5 Digital offset

By default, the ADC1215S delivers output code that corresponds to the analog input. However it is possible to add a digital offset to the output code via the SPI (bits DIG_OFFSET[5:0]; see [Table 25](#)).

11.5.6 Test patterns

For test purposes, the ADC1215S can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT_SEL[2:0]; see [Table 26](#)). A custom test pattern can be defined by the user (TESTPAT_USER; see [Table 27](#) and [Table 28](#)) and is selected when TESTPAT_SEL[2:0] = 101. The selected test pattern will be transmitted regardless of the analog input.

11.5.7 Output codes versus input voltage

Table 15. Output codes

V _{INP}	V _{INM}	Offset binary	Two's complement	OTR pin
< 1		0000 0000 0000	1000 0000 0000	1
1.0000000		0000 0000 0000	1000 0000 0000	0
0,9995117		0000 0000 0001	1000 0000 0001	0
0.9990234		0000 0000 0010	1000 0000 0010	0
0.9985352		0000 0000 0011	1000 0000 0011	0
0.9980469		0000 0000 0100	1000 0000 0100	0
....	0
0.0009766		0111 1111 1110	1111 1111 1110	0
0.0004883		0111 1111 1111	1111 1111 1111	0
0.0000000		1000 0000 0000	0000 0000 0000	0
+0.0004883		1000 0000 0001	0000 0000 0001	0
+0.0009766		1000 0000 0010	0000 0000 0010	0
....	0
+0.9980469		1111 1111 1011	0111 1111 1011	0
+0.9985352		1111 1111 1100	0111 1111 1100	0
+0.9990234		1111 1111 1101	0111 1111 1101	0
+0.9995117		1111 1111 1110	0111 1111 1110	0
+1.0000000		1111 1111 1111	0111 1111 1111	0
> +1		1111 1111 1111	0111 1111 1111	1

11.6 Serial Peripheral Interface (SPI)

11.6.1 Register description

The ADC1215S serial interface is a synchronous serial communications port that allows for easy interfacing with many commonly-used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin)

Pin SCLK is the serial clock input and \overline{CS} is the chip select pin.

Each read/write operation is initiated by a LOW level on CS. A minimum of three bytes will be transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see [Table 17](#)).

Table 16. Instruction bytes for the SPI

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/ \overline{W} [1]	W1[2]	W0[2]	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] Bit R/ \overline{W} indicates whether it is a read (1) or a write (0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred after the instruction byte (see [Table 17](#)).

Table 17. Number of data bytes to be transferred after the instruction bytes

W1	W0	Number of bytes transmitted
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes or more

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is increased to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. A falling edge on \overline{CS} in combination with a rising edge on SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but will always be a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on \overline{CS} indicates the end on data transmission.

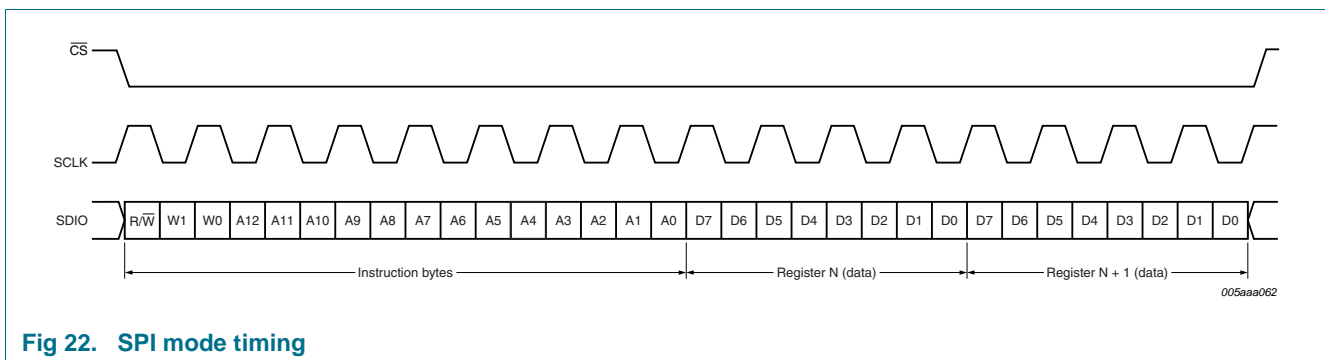


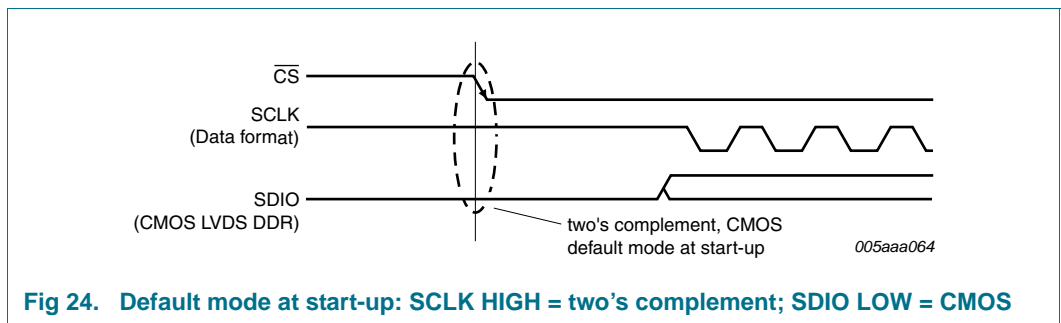
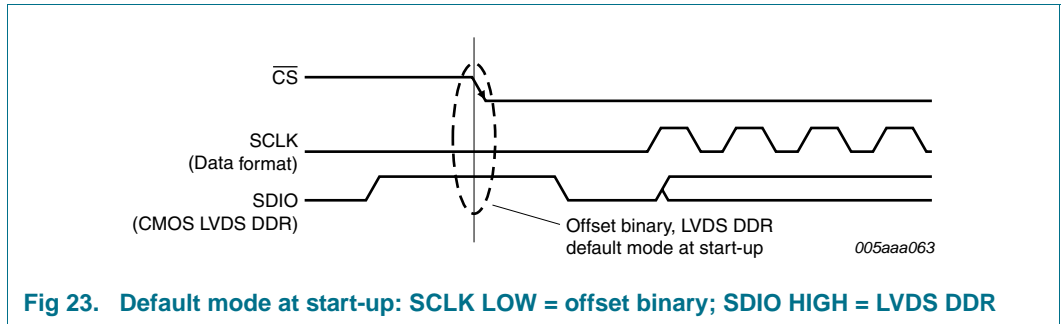
Fig 22. SPI mode timing

11.6.2 Default modes at start-up

During circuit initialization, it does not matter which output data standard has been selected. At power-up, the device enters Pin control mode.

A falling edge on \overline{CS} will trigger a transition to SPI control mode. When the ADC1215S enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see [Figure 23](#)). Once in SPI control mode, the output data standard can be changed via bit LVDS/CMOS in [Table 23](#).

When the ADC1215S enters SPI control mode, the output data format (two's complement or offset binary) is determined by the level on pin SCLK (gray code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA_FORMAT[1:0] in [Table 23](#).



11.6.3 Register allocation map

Table 18. Register allocation map

Addr Hex	Register name	R/W	Bit definition										Default Bin
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
0005	Reset and operating mode	R/W	SW_RST	RESERVED[2:0]	-	-	-	OP_MODE[1:0]	-	-	-	-	0000 0000
0006	Clock	R/W	-	SE_SEL	DIFF_SE	-	CLKDIV	DCS_EN	-	-	-	-	0000 0001
0008	Internal reference	R/W	-	-	INTREF_EN	-	INTREF[2:0]	-	-	-	-	-	0000 0000
0010	Input buffer	R/W	-	-	-	-	IB_IBIAS[1:0]	-	-	-	-	-	0000 0011
0011	Output data standard.	R/W	-	LVDS_CMO S	OUTBUF	OUTBUS_SWA P	DATA_FORMAT[1:0]	-	-	-	-	-	0000 0000
0012	Output clock	R/W	-	-	DAVINV	DAVPHASE[2:0]	-	-	-	-	-	-	0000 1110
0013	Offset	R/W	-	-	DIG_OFFSET[5:0]	-	-	-	-	-	-	-	0000 0000
0014	Test pattern 1	R/W	-	-	-	TESTPAT_SEL[2:0]	-	-	-	-	-	-	0000 0000
0015	Test pattern 2	R/W	-	-	TESTPAT_USER[11:4]	-	-	-	-	-	-	-	0000 0000
0016	Test pattern 3	R/W	-	TESTPAT_USER[5:0]	-	-	-	-	-	-	-	-	0000 0000
0017	Fast OTR	R/W	-	-	FASTOTR	FASTOTR_DET[2:0]	-	-	-	-	-	-	0000 0000
0020	CMOS output	R/W	-	-	DAV_DRV[1:0]	DATA_DRV[1:0]	-	-	-	-	-	-	0000 1110
0021	LVDS DDR O/P ₁	R/W	-	DAVI_x2_E N	DAVI[1:0]	DATAI_x2_EN	DATAI[1:0]	-	-	-	-	-	0000 0000
0022	LVDS DDR O/P ₂	R/W	-	-	BIT_BYTE_WIS E	LVDS_INT_TER[2:0]	-	-	-	-	-	-	0000 0000

Table 19. Reset and operating mode control register (address 0005h) bit description

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		reset digital section
			0	no reset
			1	performs a reset on SPI registers
6 to 4	RESERVED[2:0]		000	reserved
3 to 2	-		00	not used
1 to 0	OP_MODE[1:0]	R/W		operating mode
			00	normal (Power-up)
			01	Power-down
			10	Sleep
			11	normal (Power-up)

Table 20. Clock control register (address 0006h) bit description

Bit	Symbol	Access	Value	Description
7 to 5	-		000	not used
4	SE_SEL	R/W		single-ended clock input pin select
			0	CLKM
			1	CLKP
3	DIFF_SE	R/W		differential/single ended clock input select
			0	fully differential
			1	single-ended
2	-		0	not used
1	CLKDIV	R/W		clock input divide by 2
			0	disabled
			1	enabled
0	DCS_EN	R/W		duty cycle stabilizer
			0	disabled
			1	enabled

Table 21. Internal reference control register (address 0008h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	INTREF_EN	R/W		programmable internal reference enable
			0	disable
			1	active
2 to 0	INTREF[2:0]	R/W		programmable internal reference
			000	0 dB (FS = 2 V)
			001	1 dB (FS = 1.78 V)
			010	2 dB (FS = 1.59 V)
			011	3 dB (FS = 1.42 V)
			100	4 dB (FS = 1.26 V)
			101	5 dB (FS = 1.12 V)
			110	6 dB (FS = 1 V)
			111	reserved

Table 22. Input buffer control register (address 0010h) bit description

Bit	Symbol	Access	Value	Description
7 to 2	-		000000	not used
1 to 0	IB_IBIAS[1:0]	R/W		input buffer bias current
			00	not used
			01	medium
			10	low
			11	high

Table 23. Output data standard control register (address 0011h) bit description

Bit	Symbol	Access	Value	Description
7 to 5	-		000	not used
4	LVDS_CMOS	R/W		output data standard: LVDS DDR or CMOS
			0	CMOS
			1	LVDS DDR
3	OUTBUF	R/W		output buffers enable
			0	output enabled
			1	output disabled (high Z)
2	OUTBUS_SWAP	R/W		output bus swapping
			0	no swapping
			1	output bus is swapped (MSB becomes LSB and vice versa)
1 to 0	DATA_FORMAT[1:0]	R/W		output data format
			00	offset binary
			01	two's complement
			10	gray code
			11	offset binary

Table 24. Output clock register (address 0012h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	DAVINV	R/W		output clock data valid (DAV) polarity
			0	normal
			1	inverted
2 to 0	DAVPHASE[2:0]	R/W		DAV phase select
			000	output clock shifted (ahead) by 3 ns
			001	output clock shifted (ahead) by 2.5 ns
			010	output clock shifted (ahead) by 2 ns
			011	output clock shifted (ahead) by 1.5 ns
			100	output clock shifted (ahead) by 1 ns
			101	output clock shifted (ahead) by 0.5 ns
			110	default value as defined in timing section
			111	output clock shifted (delayed) by 0.5 ns

Table 25. Offset register (address 0013h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	-		00	not used
5 to 0	DIG_OFFSET[5:0]	R/W		digital offset adjustment
			011111	+31 LSB
		
			000000	0
		
			100000	32 LSB

Table 26. Test pattern register 1 (address 0014h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	-		00000	not used
2 to 0	TESTPAT_SEL[2:0]	R/W		digital test pattern select
			000	off
			001	mid scale
			010	FS
			011	+FS
			100	toggle '1111..1111'/'0000..0000'
			101	custom test pattern
			110	'1010..1010.'
			111	'010..1010'

Table 27. Test pattern register 2 (address 0015h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	TESTPAT_USER[11:4]	R/W	00000000	custom digital test pattern (bits 11 to 4)

Table 28. Test pattern register 3 (address 0016h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	TESTPAT_USER[3:0]	R/W	0000	custom digital test pattern (bits 3 to 0)
3 to 0	-		0000	not used

Table 29. Fast OTR register (address 0017h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	FASTOTR	R/W		fast Out-of-Range (OTR) detection
			0	disabled
			1	enabled
2 to 0	FASTOTR_DET[2:0]	R/W		set fast OTR detect level
			000	20.56 dB
			001	16.12 dB
			010	11.02 dB
			011	7.82 dB
			100	5.49 dB
			101	3.66 dB
			110	2.14 dB
			111	0.86 dB

Table 30. CMOS output register (address 0020h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3 to 2	DAV_DRV[1:0]	R/W		drive strength for DAV CMOS output buffer
			00	low
			01	medium
			10	high
			11	very high
1 to 0	DATA_DRV[1:0]	R/W		drive strength for DATA CMOS output buffer
			00	low
			01	medium
			10	high
			11	very high

Table 31. LVDS DDR output register 1 (address 0021h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	-		00	not used
5	DAVI_x2_EN	R/W		double LVDS current for DAV LVDS buffer
			0	disabled
			1	enabled
4 to 3	DAVI[1:0]	R/W		LVDS current for DAV LVDS buffer
			00	3.5 mA
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA
2	DATAI_x2_EN	R/W		double LVDS current for DATA LVDS buffer
			0	disabled
			1	enabled
1 to 0	DATAI[1:0]	R/W		LVDS current for DATA LVDS buffer
			00	3.5 mA
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA

Table 32. LVDS DDR output register 2 (address 0022h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	BIT/BYTE_WISE	R/W		DDR mode for LVDS output
			0	bit wise (even data bits output on DAV rising edge / odd data bits output on DAV falling edge)
			1	byte wise (MSB data bits output on DAV rising edge / LSB data bits output on DAV falling edge)
2 to 0	LVDS_INTTER[2:0]	R/W		internal termination for LVDS buffer (DAV and DATA)
			000	no internal termination
			001	300 :
			010	180 :
			011	110 :
			100	150 :
			101	100 :
			110	81 :
			111	60 :

12. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

SOT618-6

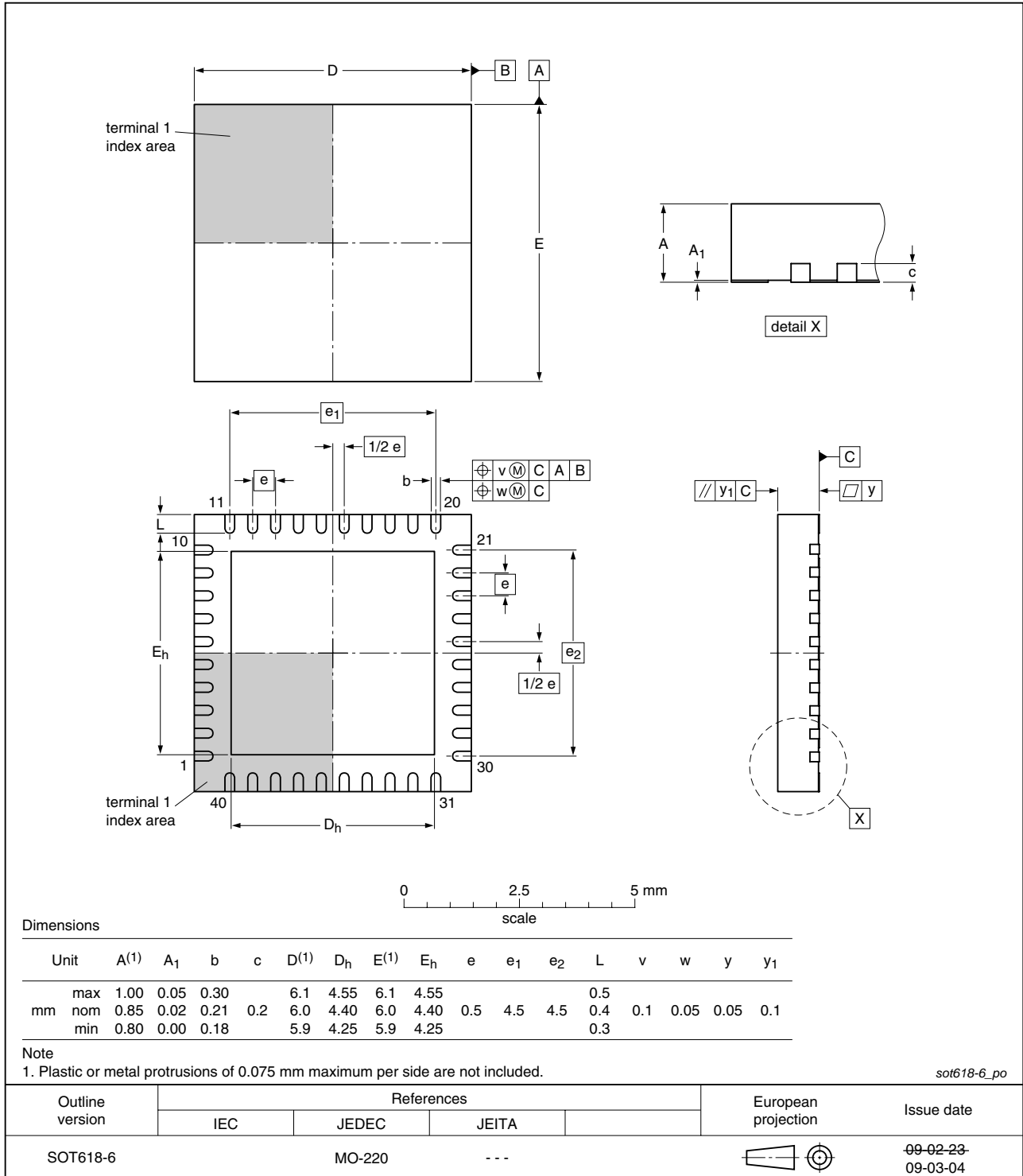


Fig 25. Package outline SOT618-6 (HVQFN40)

13. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1215S_SER_1	20100412	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

1	General description	1	12	Package outline	35
2	Features and benefits	1	13	Revision history	36
3	Applications	2	14	Legal information	37
4	Ordering information	2	14.1	Data sheet status	37
5	Block diagram	3	14.2	Definitions	37
6	Pinning information	4	14.3	Disclaimers	37
6.1	Pinning	4	14.4	Trademarks	38
6.2	Pin description	4	15	Contact information	38
7	Limiting values	6	16	Contents	39
8	Thermal characteristics	6			
9	Static characteristics	7			
10	Dynamic characteristics	10			
10.1	Dynamic characteristics	10			
10.2	Clock and digital output timing	12			
10.3	SPI timings	15			
11	Application information	16			
11.1	Device control	16			
11.1.1	SPI and Pin control modes	16			
11.1.2	Operating mode selection	16			
11.1.3	Selecting the output data standard	16			
11.1.4	Selecting the output data format	17			
11.2	Analog inputs	17			
11.2.1	Input stage	17			
11.2.2	Transformer	18			
11.3	System reference and power management	19			
11.3.1	Internal/external references	19			
11.3.2	Reference gain control	20			
11.3.3	Common-mode output voltage ($V_{O(cm)}$)	20			
11.3.4	Biasing	21			
11.4	Clock input	21			
11.4.1	Drive modes	21			
11.4.2	Equivalent input circuit	22			
11.4.3	Duty cycle stabilizer	22			
11.4.4	Clock input divider	22			
11.5	Digital outputs	23			
11.5.1	Digital output buffers: CMOS mode	23			
11.5.2	Digital output buffers: LVDS DDR mode	24			
11.5.3	Data valid (DAV) output clock	25			
11.5.4	Out-of-Range (OTR)	25			
11.5.5	Digital offset	25			
11.5.6	Test patterns	25			
11.5.7	Output codes versus input voltage	26			
11.6	Serial Peripheral Interface (SPI)	26			
11.6.1	Register description	26			
11.6.2	Default modes at start-up	27			
11.6.3	Register allocation map	29			

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