查询BUK6212-40C供应商

BUK6212-40C

N-channel TrenchMOS intermediate level FET

Rev. 2 — 21 September 2010 Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoids
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	[1]	-	-	50	A
P_{tot}	total power dissipation	see Figure 2		-	-	80	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12 A; T_{mb} = 25 °C; see Figure 11		-	9.5	11.2	mΩ

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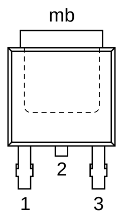
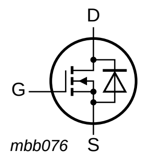
Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 50 A; $V_{sup} \leq$ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	55	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 13; see Figure 14	-	10.1	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT428 (DPAK)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6212-40C	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{GS}	gate-source voltage	Pulsed	[1]	-20	20	V
		DC	[2]	-16	16	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	[3]	-	50	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; see Figure 1		-	41	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3		-	233	A
P_{tot}	total power dissipation	see Figure 2		-	80	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C	[3]	-	50	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C		-	233	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 50$ A; $V_{sup} \leq 40$ V; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	55	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4][5][6]	-	-	J

[1] Accumulated pulse duration not to exceed 5 minutes.

[2] -16V accumulated duration not to exceed 168 hrs.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.

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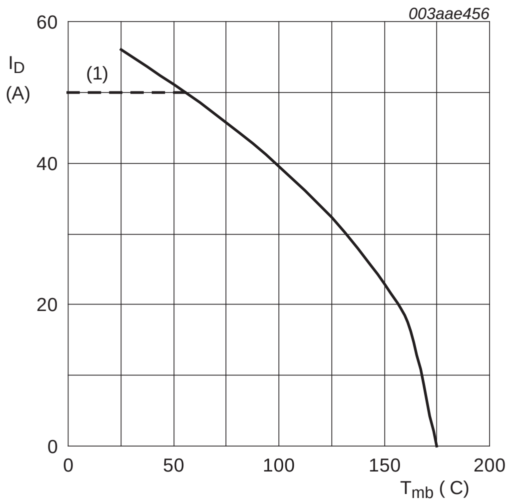
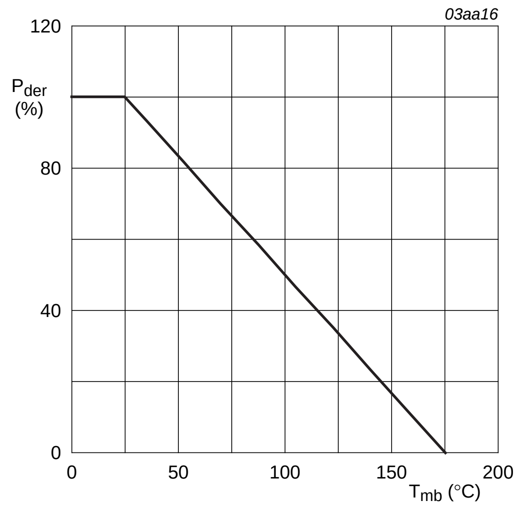


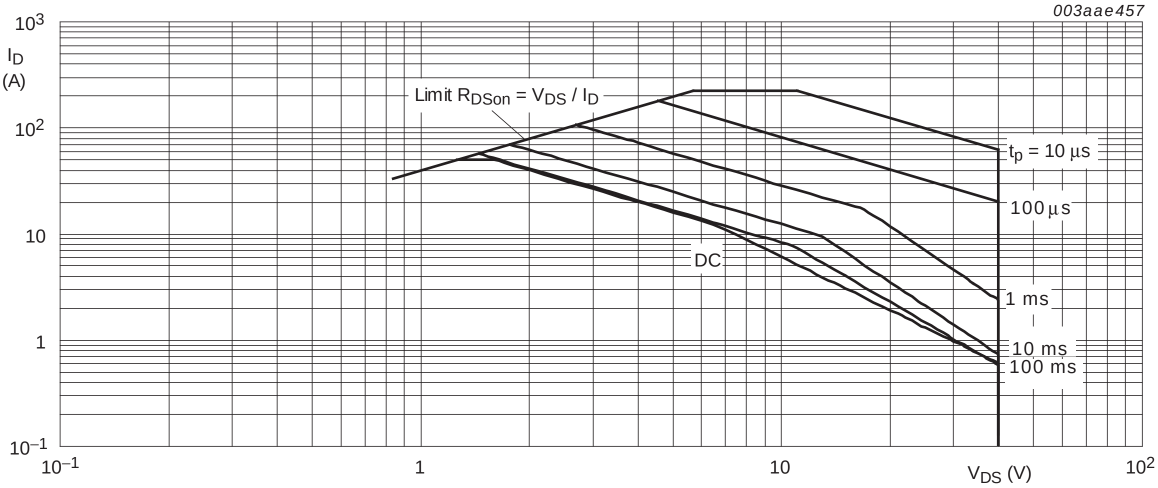
(1) Capped at 50 A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.87	K/W

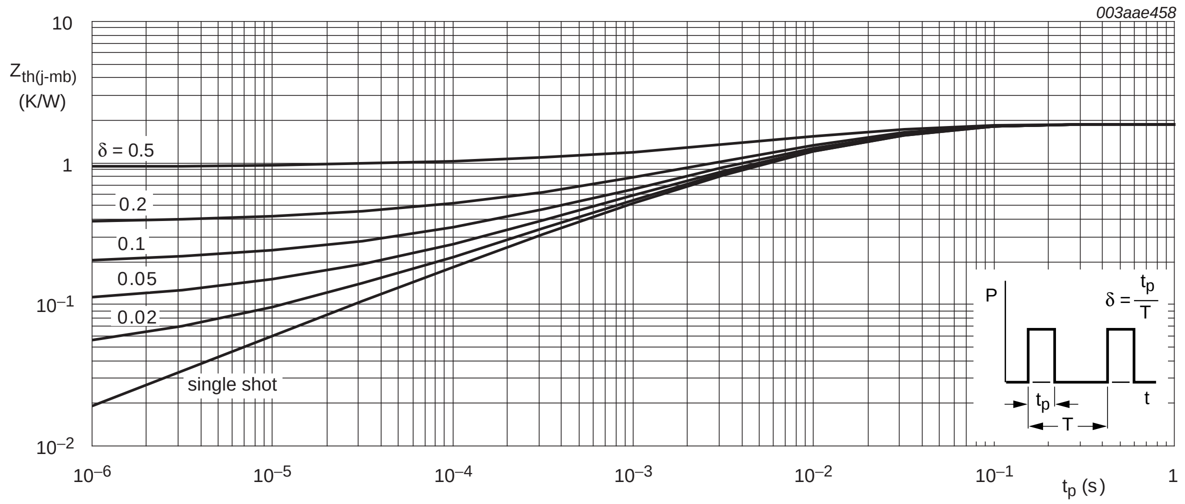

Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

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6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 9; see Figure 10	1.8	2.3	2.8	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 9; see Figure 10	-	-	3.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C	0.8	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 12 A; T_{mb} = 25 °C; see Figure 11	-	9.5	11.2	mΩ
		V_{GS} = 5 V; I_D = 12 A; T_j = 25 °C; see Figure 11	-	13	16.3	mΩ
		V_{GS} = 4.5 V; I_D = 12 A; T_{mb} = 25 °C; see Figure 11	-	15	20	mΩ
		V_{GS} = 10 V; I_D = 12 A; T_j = 175 °C; see Figure 12; see Figure 11	-	-	23.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 13; see Figure 14	-	33.9	-	nC
		I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; see Figure 13; see Figure 14	-	19.5	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 13; see Figure 14	-	5.4	-	nC
Q_{GD}	gate-drain charge		-	10.1	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1422	1900	pF
C_{oss}	output capacitance		-	205	250	pF
C_{rss}	reverse transfer capacitance		-	143	200	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω	-	9.7	-	ns
t_r	rise time		-	21	-	ns
$t_{d(off)}$	turn-off delay time		-	54	-	ns
t_f	fall time		-	32	-	ns
L_D	internal drain inductance	measured from source lead to source bond pad; ; T_j = 25 °C	-	3.5	-	nH
L_S	internal source inductance	T_j = 25 °C; measured from drain to centre of die;	-	2.5	-	nH

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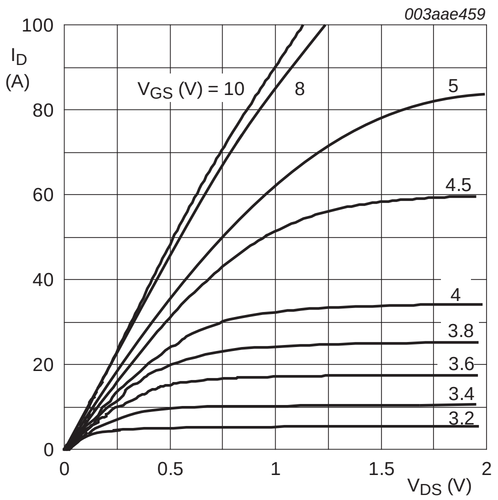
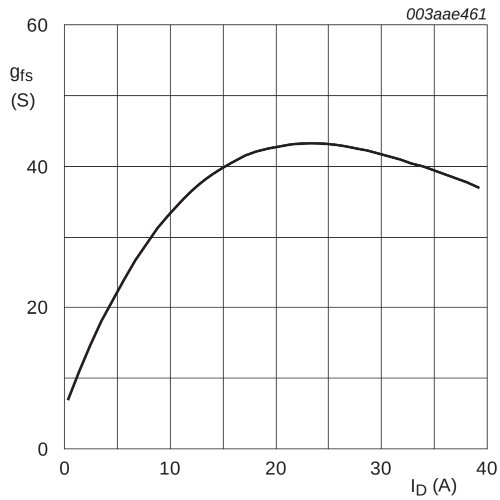
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	35.6	-	ns
Q_r	recovered charge		-	38	-	nC



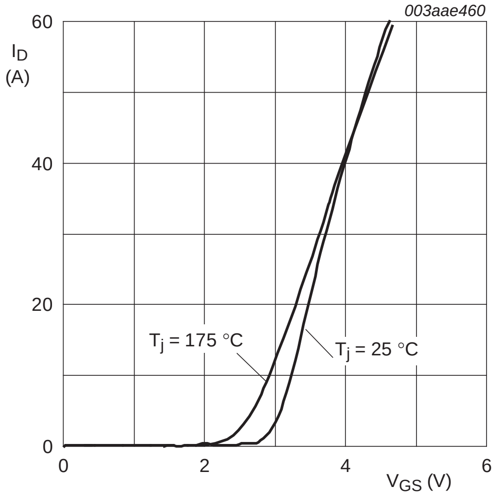
$T_j = 25\ °C;\ t_p = 300\ \mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



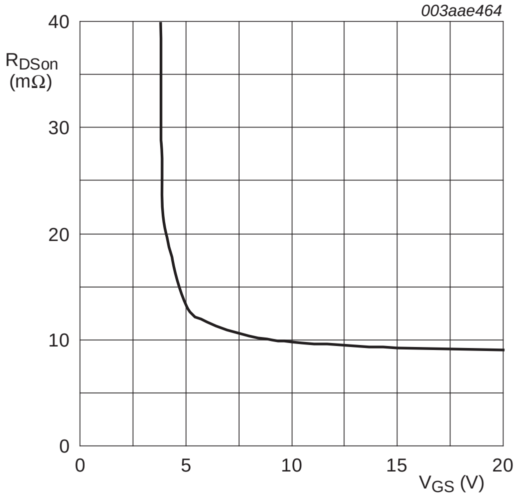
$T_j = 25\ °C;\ V_{DS} = 25\ V$

Fig 6. Forward transconductance as a function of drain current; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\ °C;\ I_D = 12\ A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

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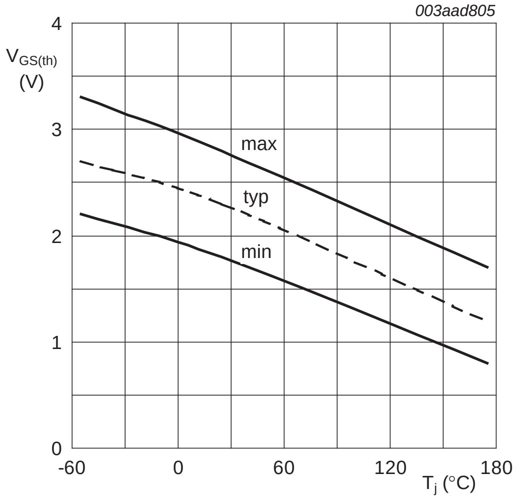
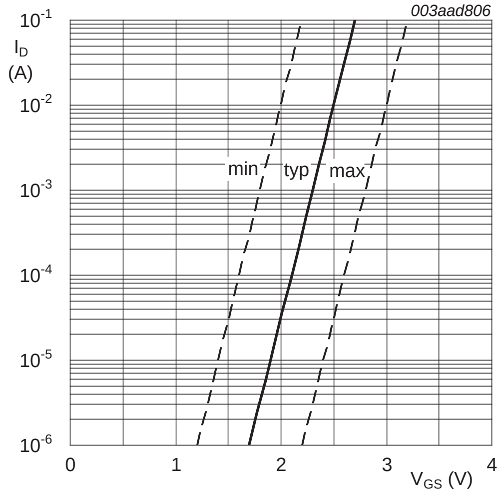


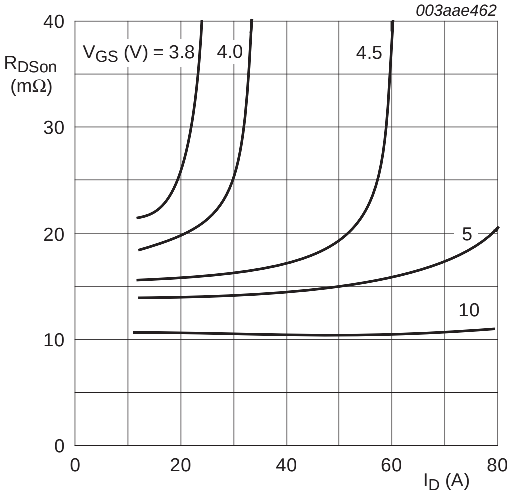
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



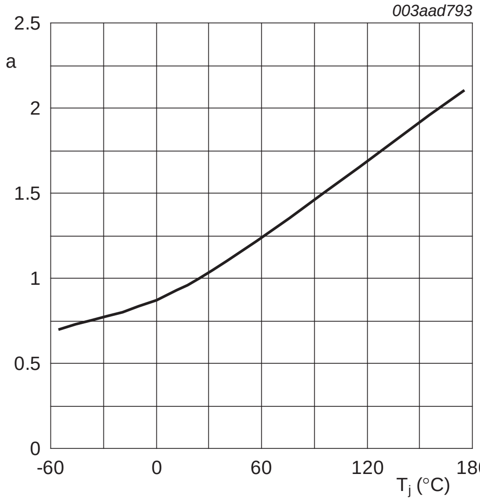
$$T_j = 25\,°C; V_{DS} = 5V$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$$T_j = 25\ °C;\ t_p = 300\ \mu s$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

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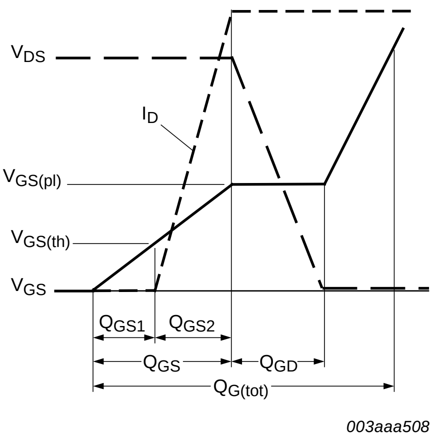
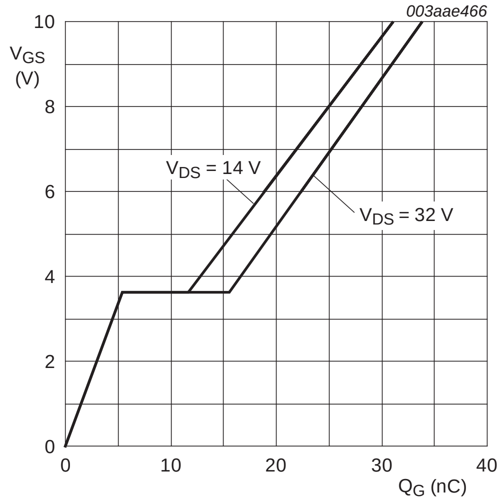
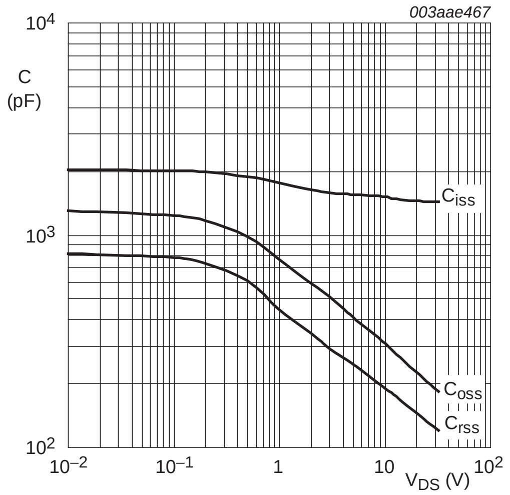


Fig 13. Gate charge waveform definitions



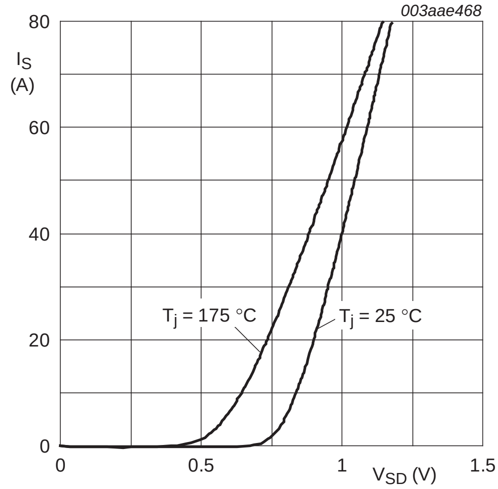
$T_j = 25\ °C;\ I_D = 25\ A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\ V;\ f = 1\ MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\ V$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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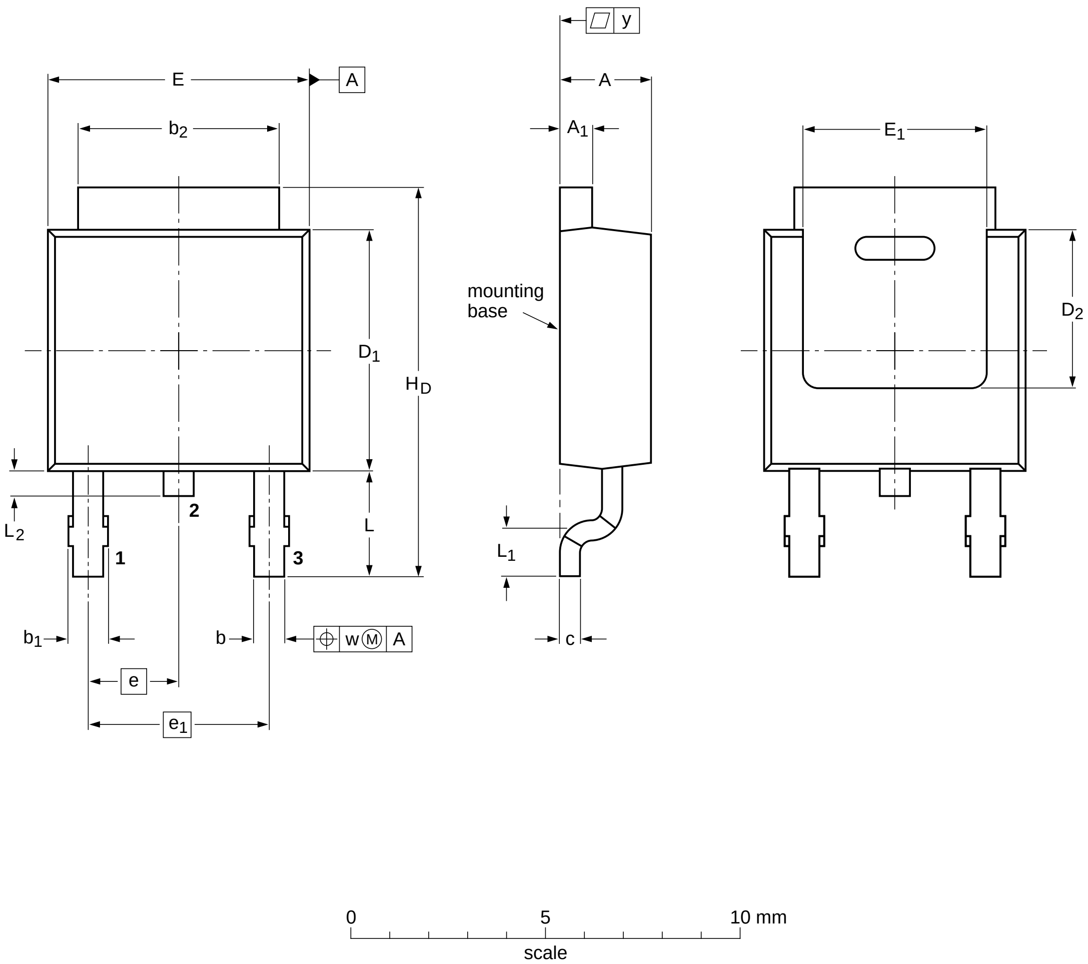
7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 17. Package outline SOT428 (DPAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6212-40C v.2	20100921	Product data sheet	-	BUK6212-40C v.1
Modifications:	• Status changed from Objective to Product. • Various changes to content.			
BUK6212-40C v.1	20100512	Objective data sheet	-	-

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9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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