

# BUK714R1-40BT

查询BUK714R1-40BT供应商

N-channel TrenchPLUS standard level FET

Rev. 02 — 10 February 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. The devices include TrenchPLUS diodes for temperature sensing. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Allows responsive temperature monitoring due to integrated temperature sensor
- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V loads
- Electrical Power Assisted Steering (EPAS)
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference

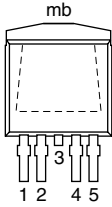
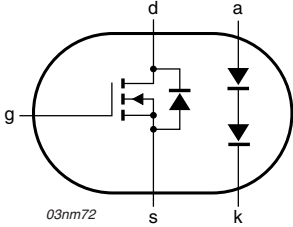
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a> ; see <a href="#">Figure 3</a>	[1]	-	75	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 2</a>	[1]	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	-	272	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 50\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	3.4	4.1	mΩ

[1] Continuous current is limited by package.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT426 (D2PAK)</b></p>	
2	A	anode		
3	D	drain		
4	K	cathode		
5	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK714R1-40BT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 5 leads (one lead cropped)	SOT426

## 4. Limiting values

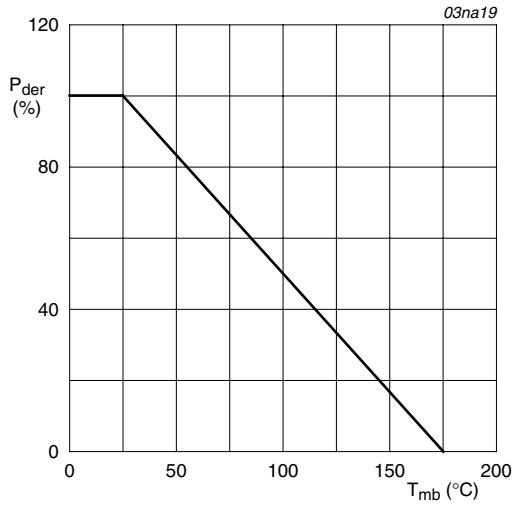
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> ; see <a href="#">Figure 3</a>	[1]	-	187	A
			[2]	-	75	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	[2]	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	748	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	272	W	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$ ;	[1]	-	187	A
			[2]	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	748	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	1.5	J	
<b>Electrostatic discharge</b>						
$V_{esd}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	4	kV	

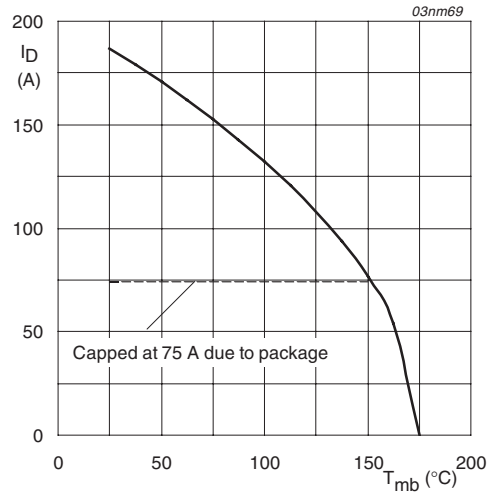
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



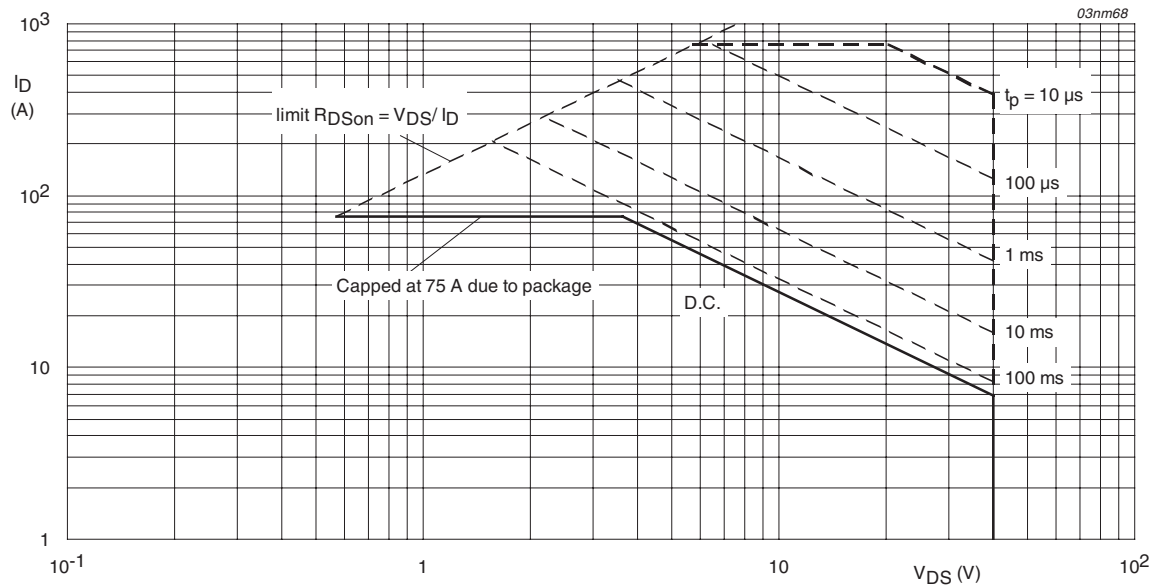
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**



$$V_{GS} \geq 10V$$

**Fig 2. Continuous drain current as a function of mounting base temperature**



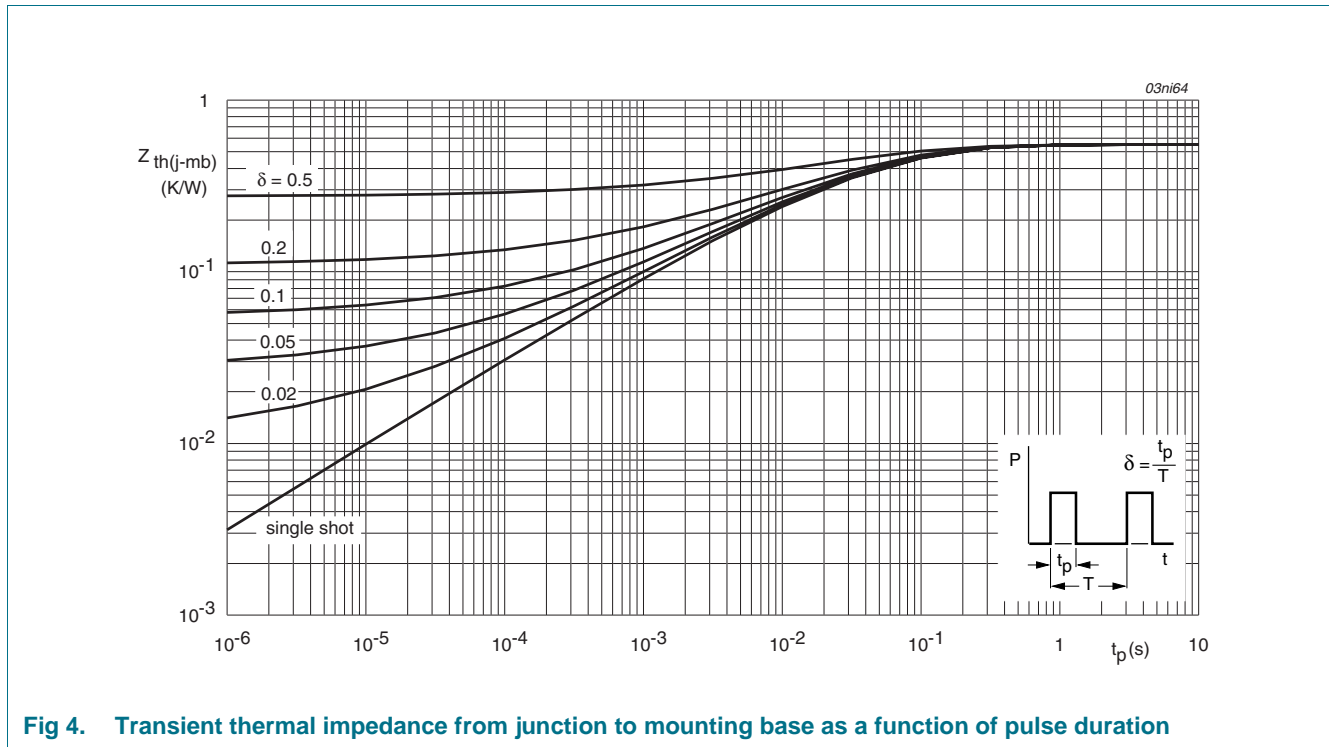
$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is single pulse}$$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	-	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.55	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 50 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	3.4	4.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 50 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	7.8	m $\Omega$
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 1 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	1.58	1.6	1.63	V
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 1 \text{ mA}; T_j > 55 \text{ }^\circ\text{C}; T_j < 175 \text{ }^\circ\text{C}$	-2.55	-2.83	-3.11	mV/K
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	83	-	nC
$Q_{GS}$	gate-source charge		-	18	-	nC
$Q_{GD}$	gate-drain charge		-	29	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	5106	6808	pF
$C_{oss}$	output capacitance		-	1389	1667	pF
$C_{rss}$	reverse transfer capacitance		-	527	721	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	38	-	ns
$t_r$	rise time		-	82	-	ns
$t_{d(off)}$	turn-off delay time		-	141	-	ns
$t_f$	fall time		-	90	-	ns
$L_D$	internal drain inductance	from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; lead length 6 mm; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 16</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = -10\text{ V}$ ;	-	70	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	55	-	nC

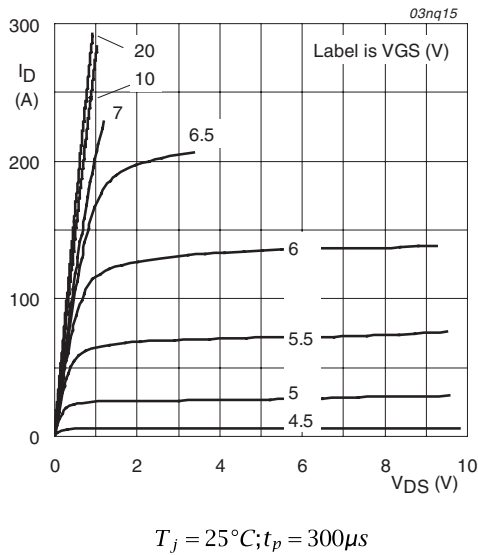


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

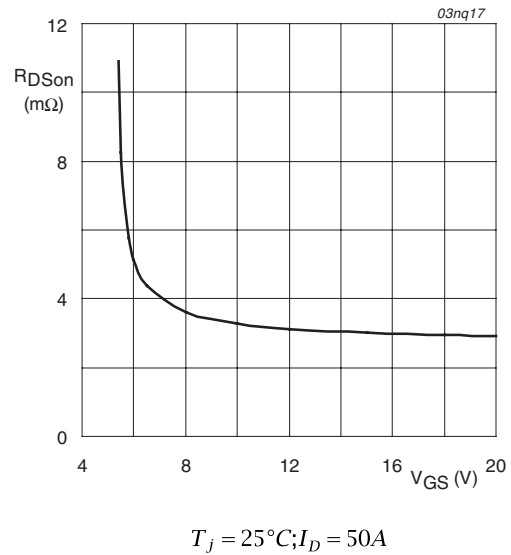


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

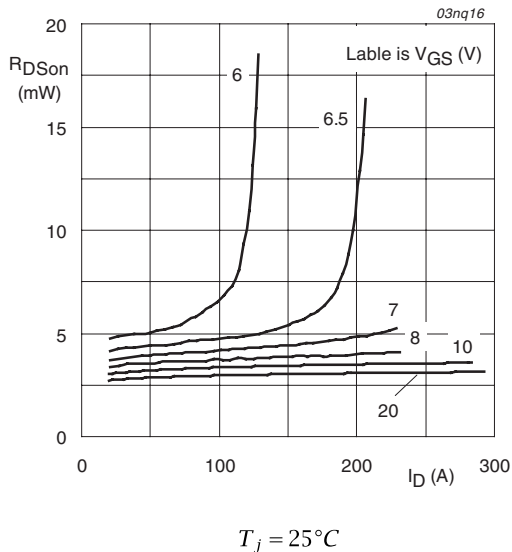


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

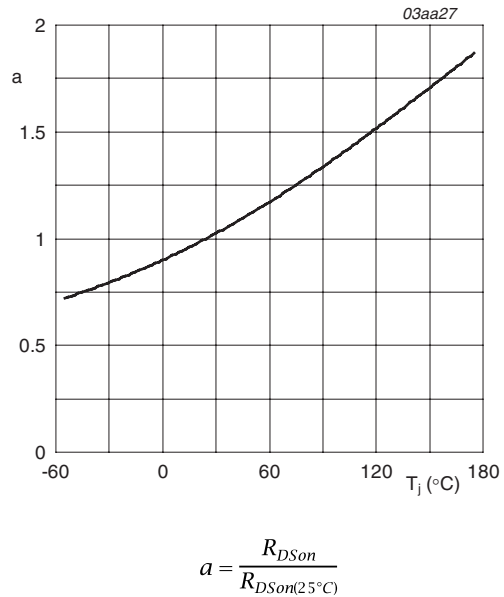
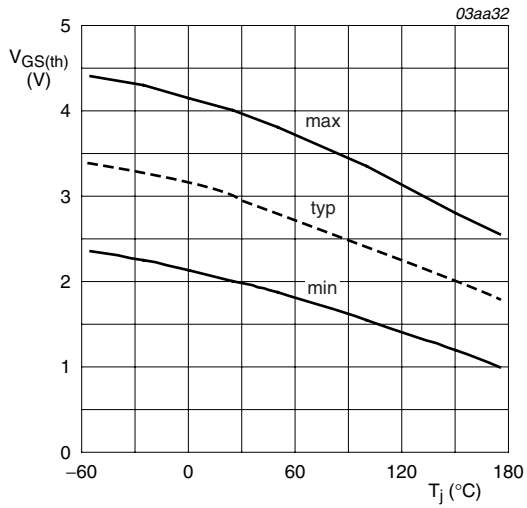
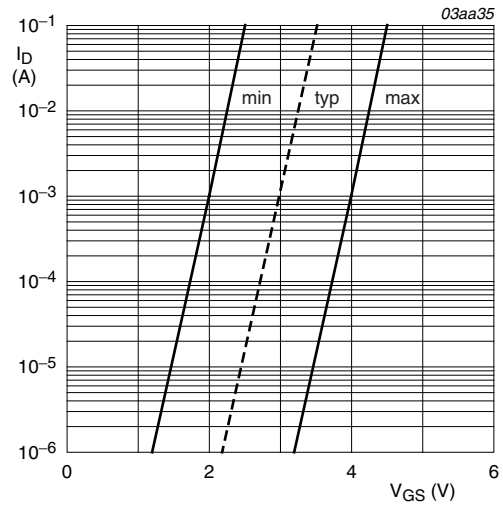


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



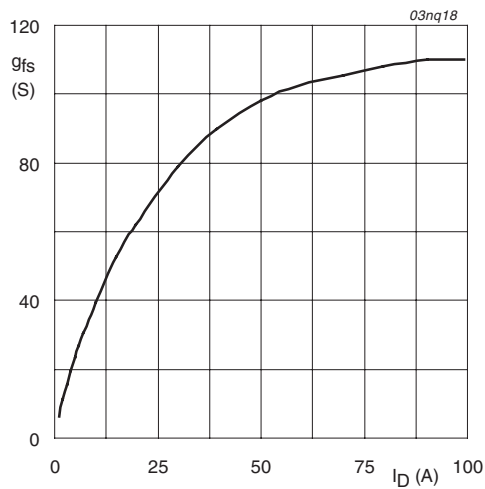
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



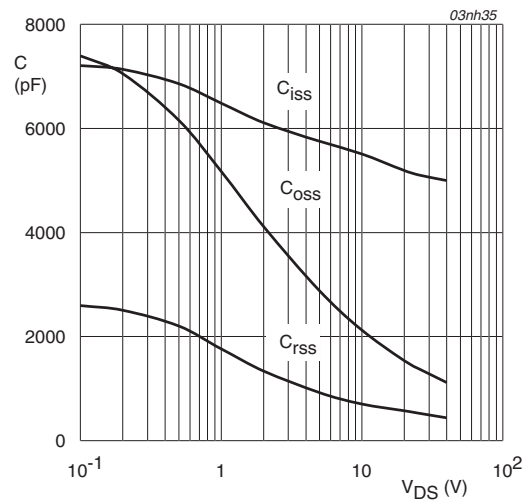
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

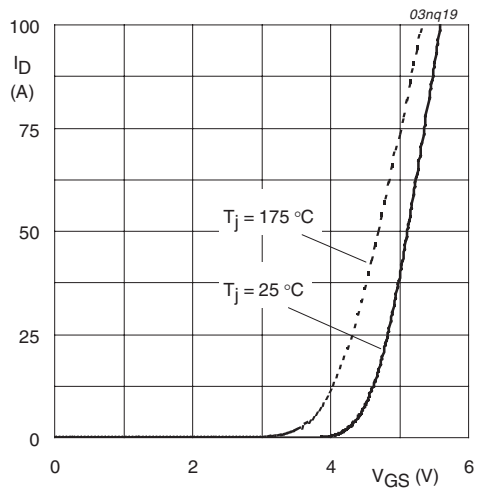
**Fig 11. Forward transconductance as a function of drain current; typical values**



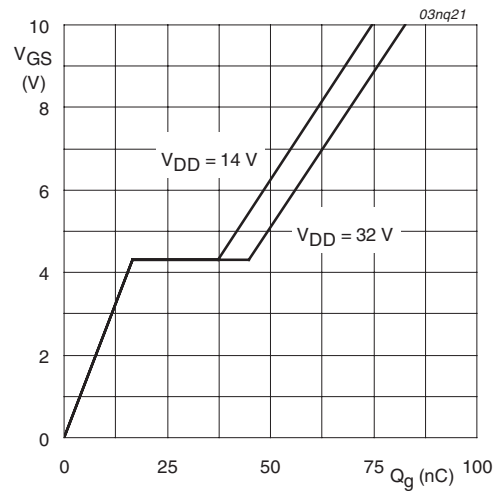
$V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

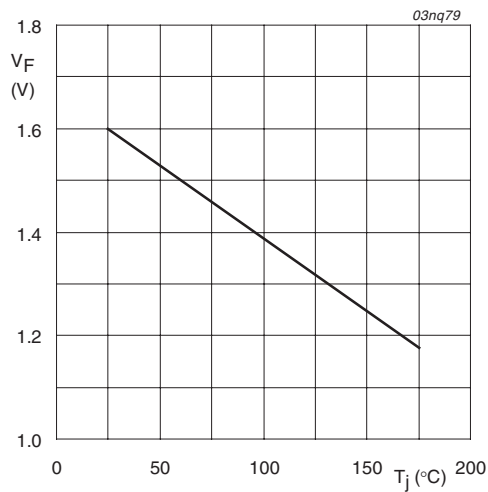




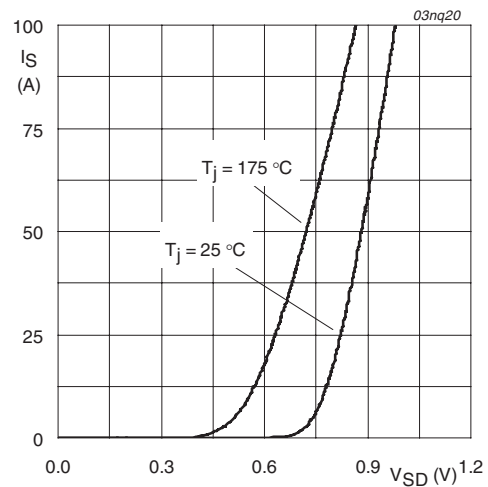
**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values**



**Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values**

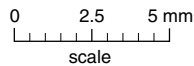
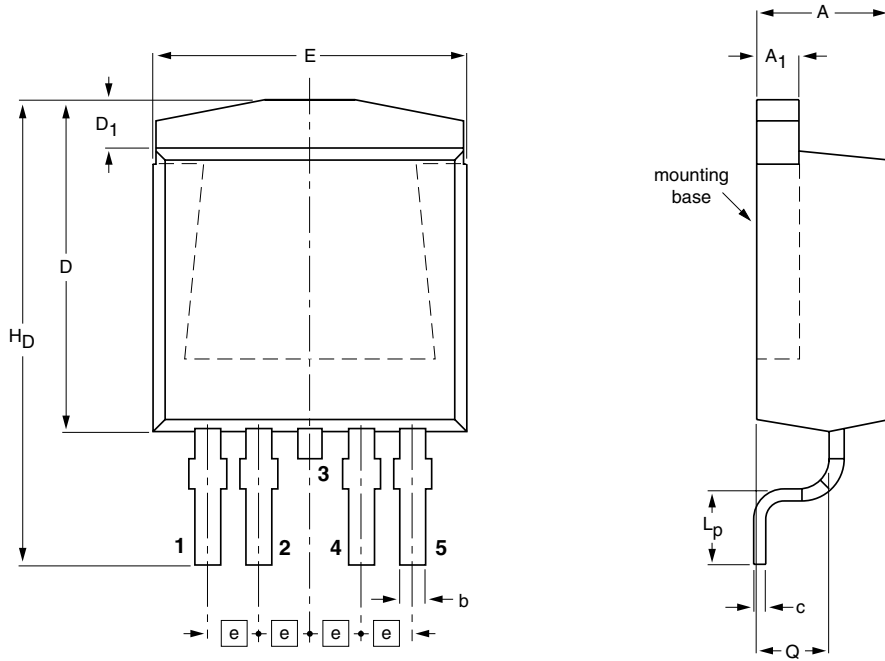


**Fig 16. Reverse diode current as a function of reverse diode voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 5 leads (one lead cropped)

SOT426



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.70	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT426						05-03-09 06-03-16

Fig 17. Package outline SOT426 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK714R1-40BT_2	20090210	Product data sheet	-	BUK71_794R1_40BT-01
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number BUK714R1-40BT separated from data sheet BUK71_794R1_40BT-01.</li></ul>		
BUK71_794R1_40BT-01 (9397 750 13954)	20041104	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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