BUK7L11-34ARC

N-channel TrenchPLUS standard level FET

Rev. 05 — 17 February 2009 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. The devices include internal gate resistors and TrenchPLUS diodes for clamping and ElectroStatic Discharge (ESD) protection. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Reduced component count due to integrated gate resistor

1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	[1] [2]	-	-	89	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	-	172	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 30 A; T_j = 25 °C; see Figure 14; see Figure 6		-	8	11	mΩ

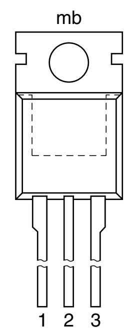
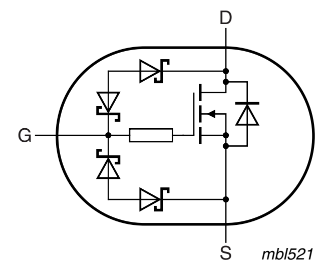
[1] Current is limited by power dissipation chip rating.

[2] Refer to document 9397 750 12572 for further information.

founded by Philips

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT78C (TO-220AB)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7L11-34ARC	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-leads	SOT78C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

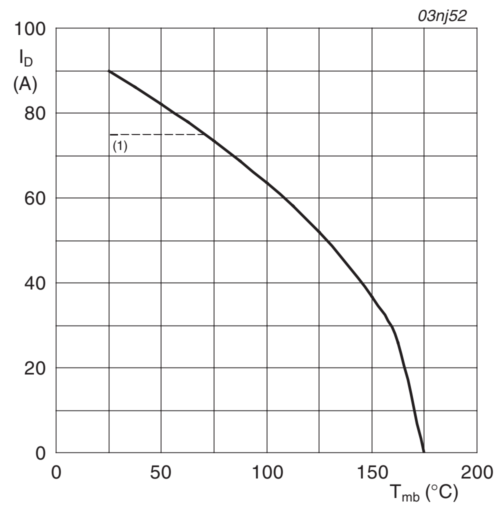
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	[1]	-	34	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	[1]	-	34	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	[2][3]	-	89	A
			[4]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 1		-	63	A
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \leq 10$ µs; pulsed; see Figure 3		-	358	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	172	W
$I_{DG(CL)}$	drain-gate clamping current	pulsed; t_p = 5 ms; δ = 0.01		-	50	mA
$I_{GS(CL)}$	gate-source clamping current			-	50	mA
		continuous		-	10	mA
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[2][3]	-	89	A
			[4]	-	75	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C		-	358	A
Avalanche ruggedness						
$E_{DS(CL)S}$	non-repetitive drain-source clamping energy	I_D = 60 A; $V_{DS} \leq 34$ V; V_{GS} = 10 V; R_{GS} = 50 Ω; unclamped; $T_{j(init)}$ = 25 °C		-	465	mJ
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage	HBM; C = 250 pF; R = 1.5 kΩ		-	6	kV
		HBM; C = 100 pF; R = 1.5 kΩ		-	8	kV

[1] Voltage is limited by clamping.

[2] Current is limited by power dissipation chip rating.

[3] Refer to document 9397 750 12572 for further information.

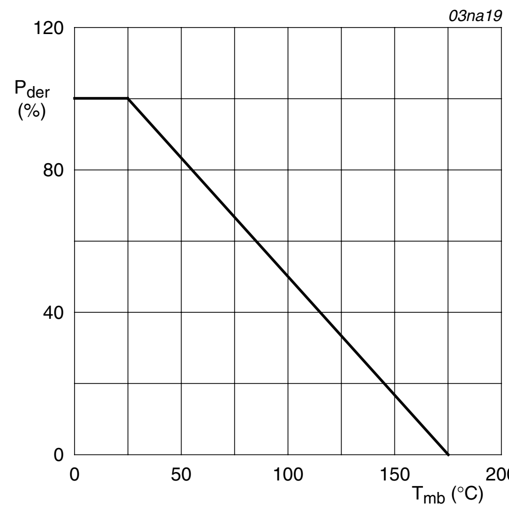
[4] Continuous current is limited by package.



$V_{GS} \geq 10V$

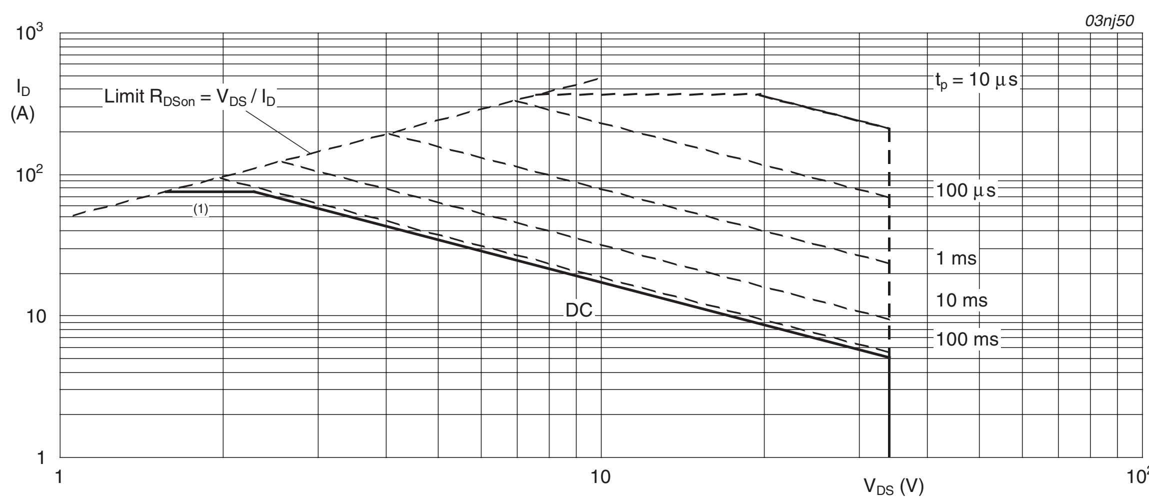
(1) Capped at 75 A due to package

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C; I_{DM}$ is single pulse

(1) Capped at 75 A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.55	0.87	K/W

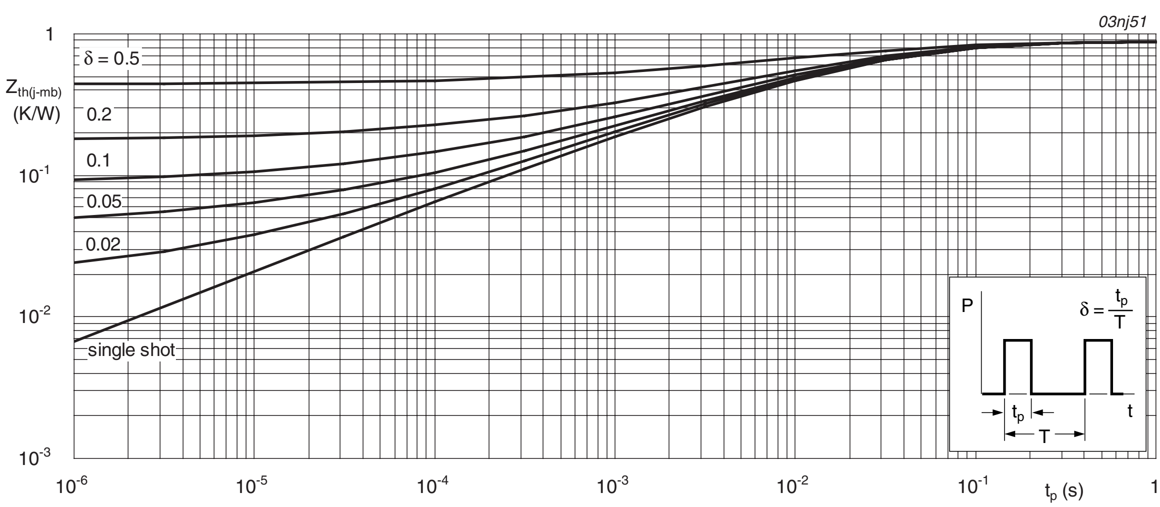


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

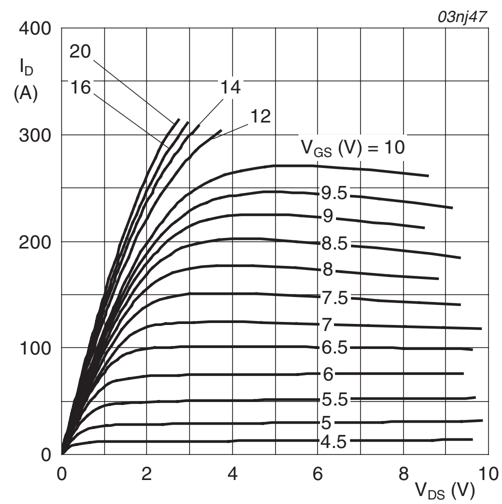
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DG}$	drain-gate (Zener diode) breakdown voltage	I_D = 1 mA; V_{GS} = 0 V; T_j = 25 °C	34	-	45	V
		I_D = 1 mA; V_{GS} = 0 V; T_j = -55 °C	34	-	45	V
$V_{DS(CL)}$	drain-source clamping voltage	$I_{GS(CL)}$ = -2 mA; I_D = 1 A; T_j = 25 °C; see Figure 12; see Figure 18	-	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 13; see Figure 7	2.2	3	3.8	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 13; see Figure 7	1.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 13; see Figure 7	1.2	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 13; see Figure 7	-	-	4.2	V
I_{DSS}	drain leakage current	V_{DS} = 16 V; V_{GS} = 0 V; T_j = 25 °C	-	0.1	2	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 150 °C	-	3	50	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 175 °C	-	18	250	µA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = 1 mA; V_{DS} = 0 V; T_j > -55 °C; T_j < 175 °C; see Figure 18; see Figure 19	20	22	-	V
		I_G = -1 mA; V_{DS} = 0 V; T_j > -55 °C; T_j < 175 °C; see Figure 18; see Figure 19	20	22	-	V
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C	-	5	1000	nA
		V_{DS} = 0 V; V_{GS} = -10 V; T_j = 25 °C	-	5	1000	nA
		V_{DS} = 0 V; V_{GS} = 10 V; T_j = 175 °C	-	-	50	µA
		V_{DS} = 0 V; V_{GS} = -10 V; T_j = 175 °C	-	-	50	µA
		V_{DS} = 0 V; V_{GS} = 16 V; T_j = 175 °C	-	-	150	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 30 A; T_j = 25 °C; see Figure 14; see Figure 6	-	8	11	mΩ
		V_{GS} = 10 V; I_D = 30 A; T_j = 175 °C; see Figure 14; see Figure 6	-	-	20.9	mΩ
		V_{GS} = 16 V; I_D = 30 A; T_j = 25 °C	-	7	9.7	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz; T_j = 25 °C	-	11	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 27 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 16	-	53	-	nC
Q_{GS}	gate-source charge		-	11	-	nC
Q_{GD}	gate-drain charge		-	20	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 17	-	1880	2506	pF
C_{oss}	output capacitance		-	640	768	pF
C_{rss}	reverse transfer capacitance		-	400	548	pF

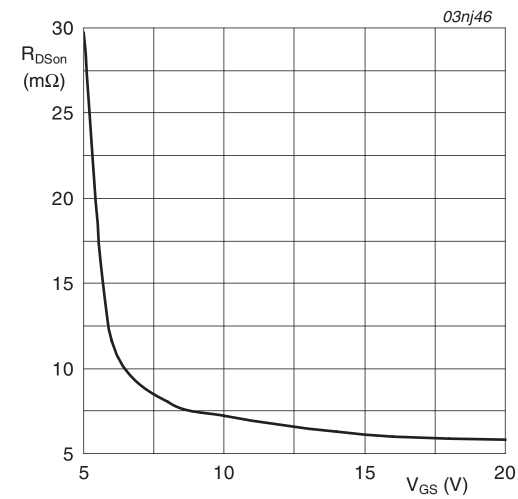
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	20	-	ns
t_r	rise time		-	92	-	ns
$t_{d(off)}$	turn-off delay time		-	127	-	ns
t_f	fall time		-	118	-	ns
L_D	internal drain inductance	measured from contact screw on mounting base to centre of die; T_j = 25 °C	-	3.5	-	nH
		measured from drain lead 6 mm from package to centre of die; T_j = 25 °C	-	4.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C	-	52	-	ns
Q_r	recovered charge		-	28	-	nC



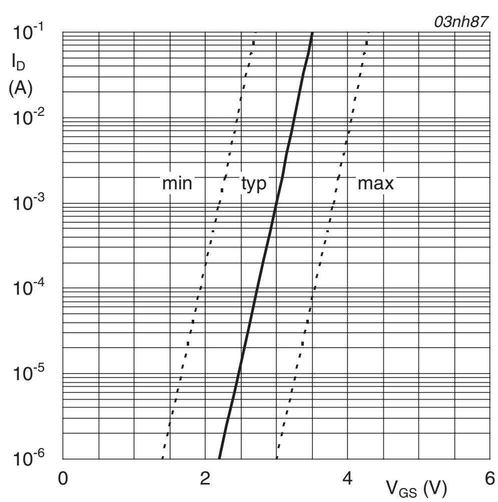
$T_j = 25°C; t_p = 300 \mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



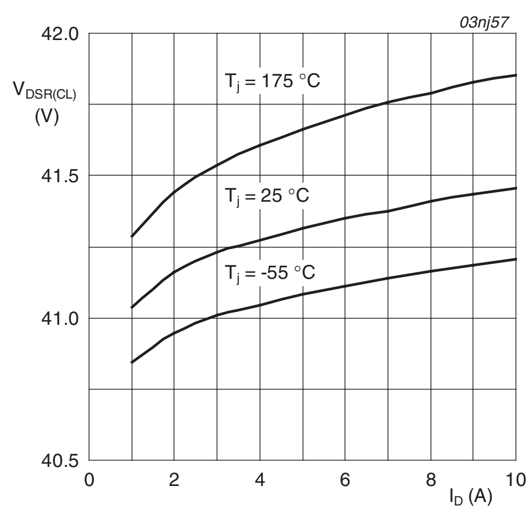
$T_j = 25°C; I_D = 30A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25°C; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$I_G = -2mA$

Fig 8. Drain-source clamping voltage as a function of drain current; typical values

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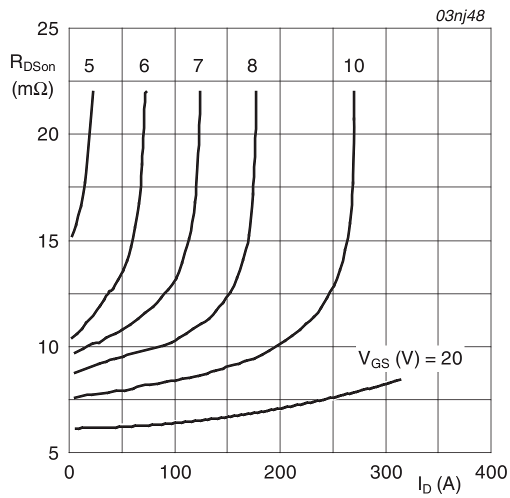
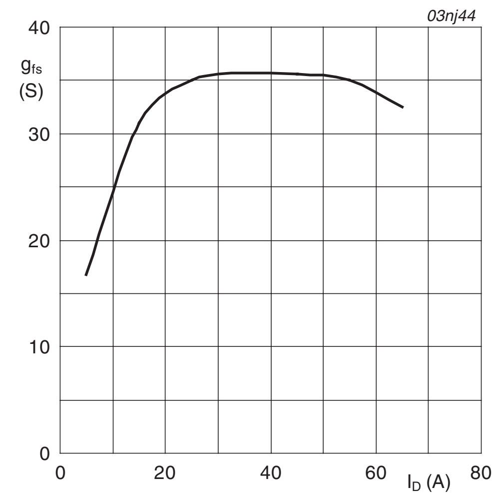


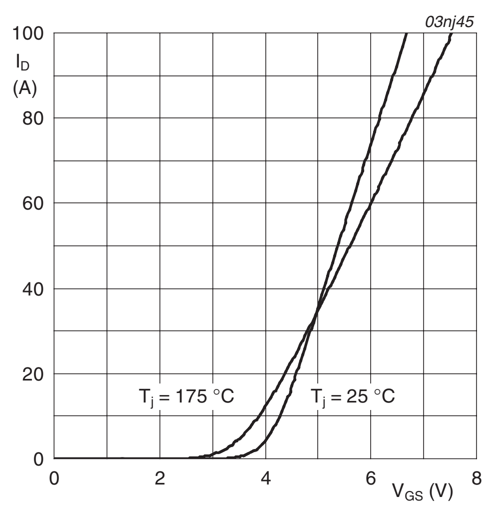
$T_j = 25°C; t_p = 300 µs$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



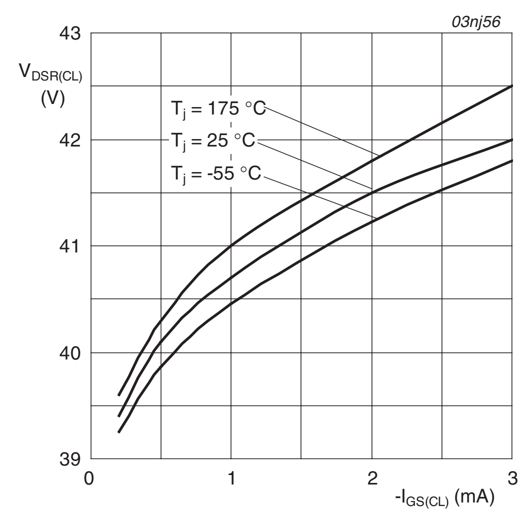
$T_j = 25°C; V_{DS} = 25 V$

Fig 10. Forward transconductance as a function of drain current; typical values



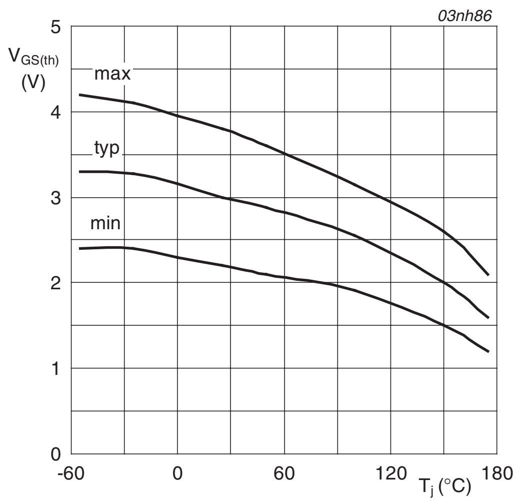
$V_{DS} = 25 V$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



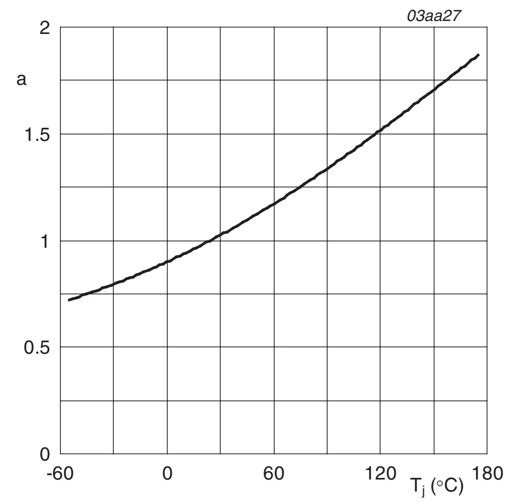
$I_D = 10 A$

Fig 12. Drain-source clamping voltage as a function of gate-source clamping current; typical values



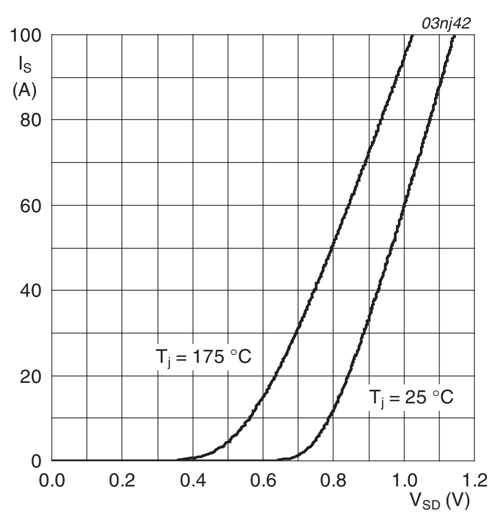
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 13. Gate-source threshold voltage as a function of junction temperature



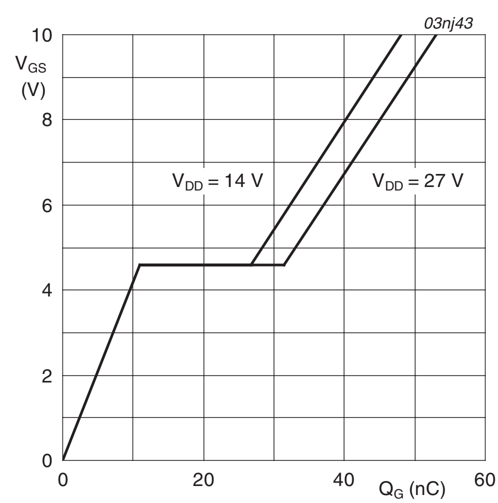
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 14. Normalized drain-source on-state resistance factor as a function of junction temperature



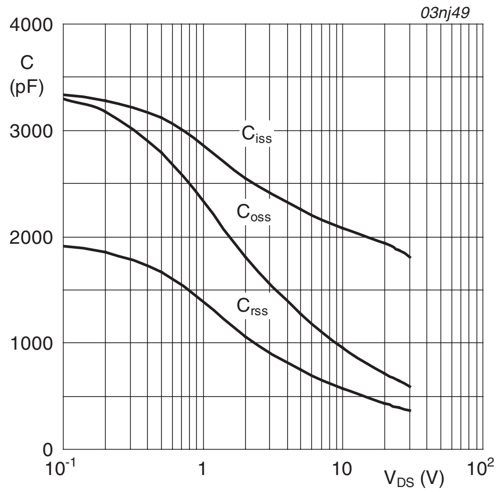
$V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values



$T_j = 25°C; I_D = 25A$

Fig 16. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

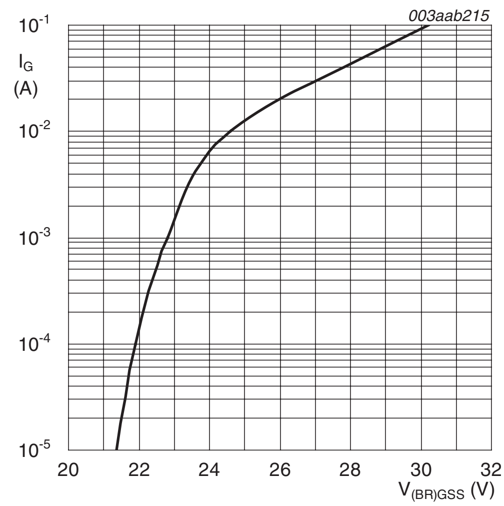
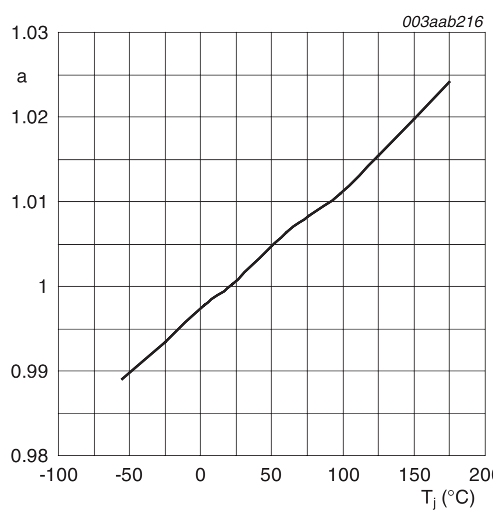


Fig 18. Source-gate clamping current as a function of source-gate clamping voltage; typical values

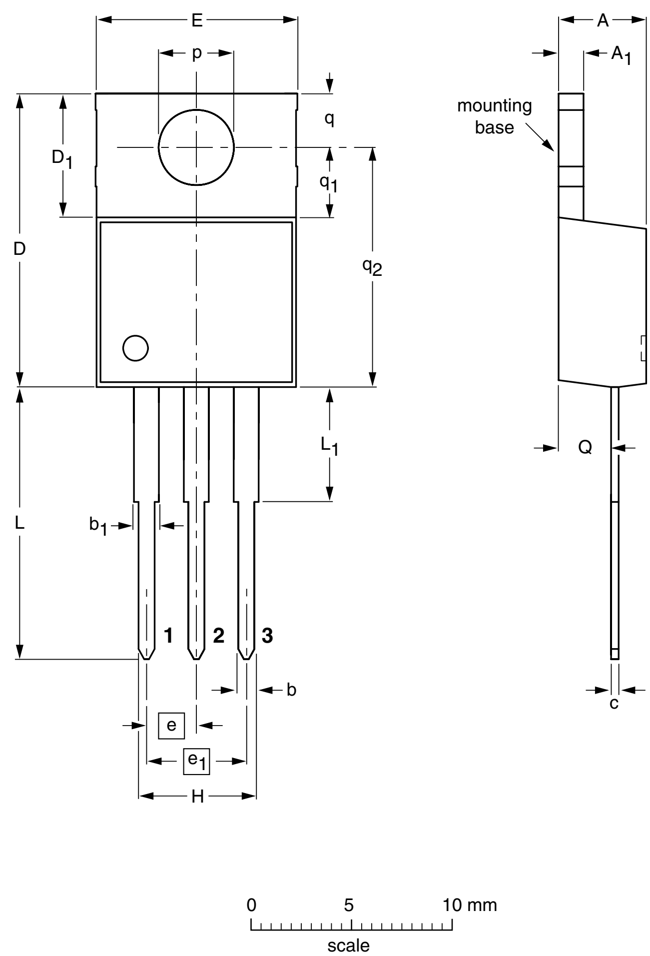


$$a = \frac{V_{(BR)GSS}}{V_{(BR)GSS(25°C)}}$$

Fig 19. Normalized source-gate clamping voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads **SOT78C**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	e_1	H	L	L_1	p	Q	q	q_1	q_2
mm	4.58 4.31	1.33 1.21	0.87 0.76	1.33 1.21	0.44 0.33	15.07 14.80	6.47 6.22	10.40 10.00	2.64 2.44	5.16 5.00	6.03 5.76	14.00 13.50	6.10 5.58	3.90 3.78	2.72 2.40	2.95 2.69	3.80 3.42	12.40 12.00

Notes

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78C		3-lead TO-220				~~01-12-11~~ 03-01-21

Fig 20. Package outline SOT78C (TO-220)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7L11-34ARC_5	20090217	Product data sheet	-	BUK7L11-34ARC_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUK7L11-34ARC_4	20051216	Product data sheet	-	BUK7L11_34ARC-03
BUK7L11_34ARC-03 (9397 750 12163)	20031203	Product data sheet	-	BUK7L11_34ARC-02
BUK7L11_34ARC-02 (9397 750 11472)	20030522	Product data sheet	-	BUK7L11_34ARC-01
BUK7L11_34ARC-01 (9397 750 11178)	20030423	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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