

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 185 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 185\text{ °C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	167	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$	-	4.4	5	mΩ
		$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	5.9	7	mΩ



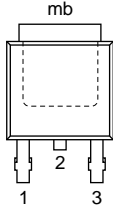
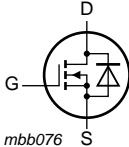
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; unclamped	-	-	329	mJ
Dynamic characteristics						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 24\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 11</a>	-	12	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

SOT428 (DPAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9207-30B	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

**Table 4. Limiting values**

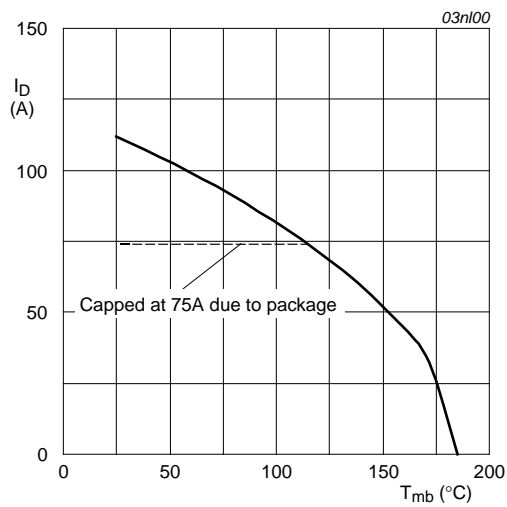
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 185 °C	-	-	30	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ	-	-	30	V
V <sub>GS</sub>	gate-source voltage		-15	-	15	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 1</a> ; <a href="#">[1]</a>	-	-	75	A
		see <a href="#">Figure 3</a> <a href="#">[2]</a>	-	-	112	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 1</a> <a href="#">[1]</a>	-	-	75	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed; see <a href="#">Figure 3</a>	-	-	449	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	167	W
T <sub>stg</sub>	storage temperature		-55	-	185	°C
T <sub>j</sub>	junction temperature		-55	-	185	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C <a href="#">[3]</a>	-	-	75	A
			<a href="#">[2]</a>	-	-	112
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C	-	-	449	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 75 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	-	329	mJ

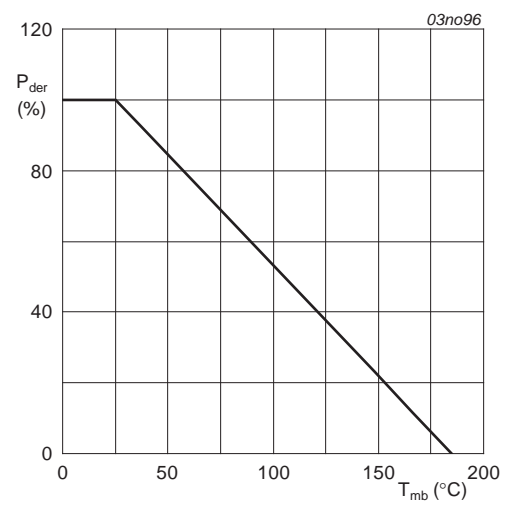
[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.

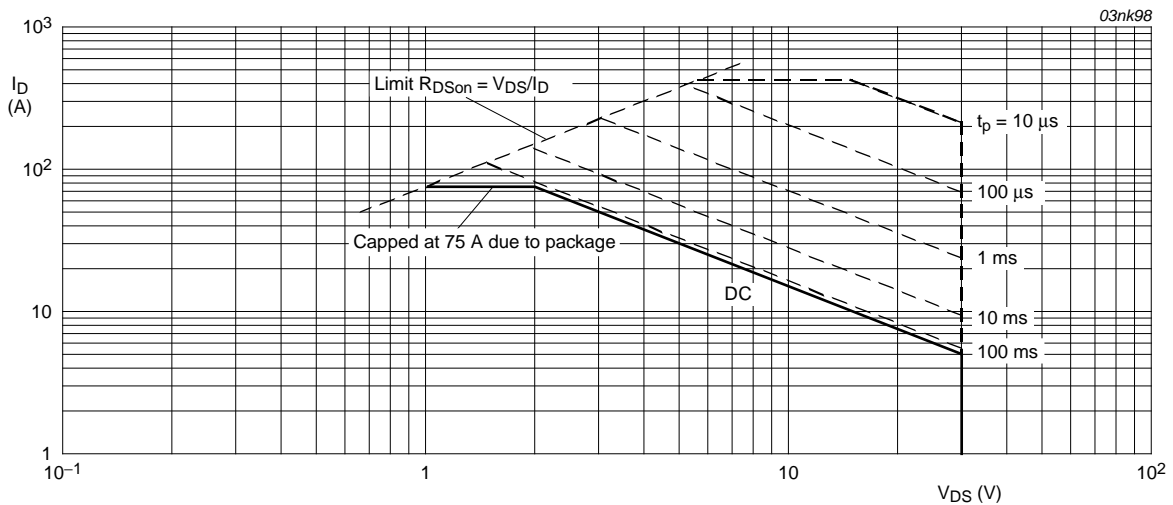


**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W

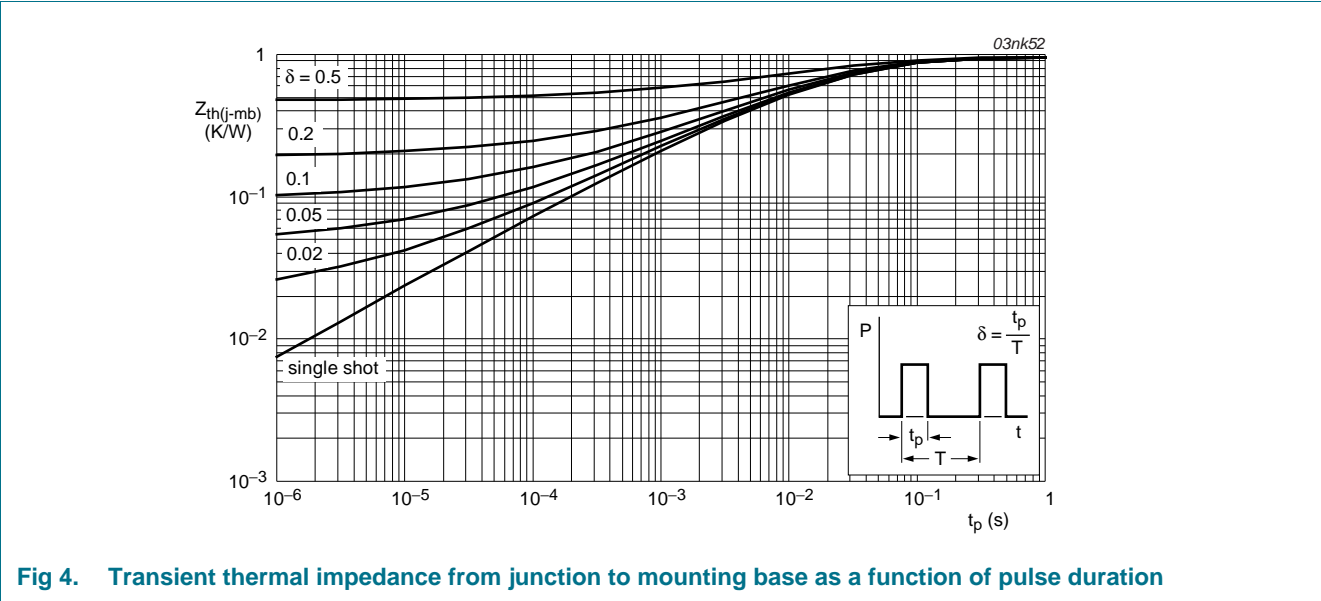


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	30	-	-	V
		I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 8</a>	-	-	2.3	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 8</a>	1.1	1.5	2	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 185 °C; see <a href="#">Figure 8</a>	0.4	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 185 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>DS</sub> = 0 V; V <sub>GS</sub> = -15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C	-	4.4	5	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C	-	-	7.7	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 185 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	-	13.3	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	5.9	7	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	31	-	nC
Q <sub>GS</sub>	gate-source charge		-	8	-	nC
Q <sub>GD</sub>	gate-drain charge		-	12	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	2573	3430	pF
C <sub>oss</sub>	output capacitance		-	635	762	pF
C <sub>rss</sub>	reverse transfer capacitance		-	268	367	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 25 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 10 Ω; T <sub>j</sub> = 25 °C	-	19	-	ns
t <sub>r</sub>	rise time		-	82	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	100	-	ns
t <sub>f</sub>	fall time		-	107	-	ns
L <sub>D</sub>	internal drain inductance	measured from drain to center of die ; T <sub>j</sub> = 25 °C	-	2.5	-	nH
L <sub>S</sub>	internal source inductance	measured from source lead to source bond pad ; T <sub>j</sub> = 25 °C	-	7.5	-	nH
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	55	-	ns
Q <sub>r</sub>	recovered charge		-	42	-	nC

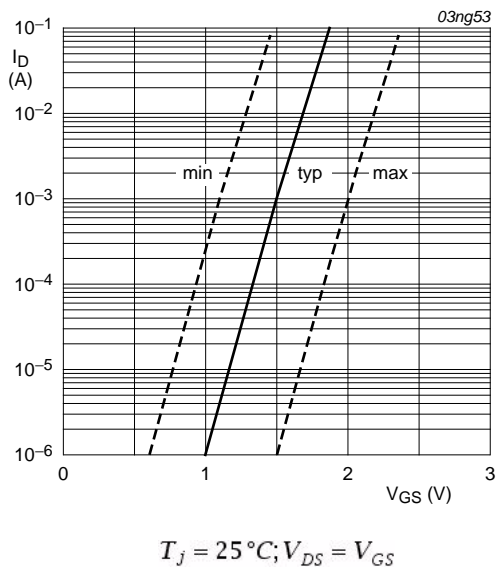


Fig 5. Sub-threshold drain current as a function of gate-source voltage

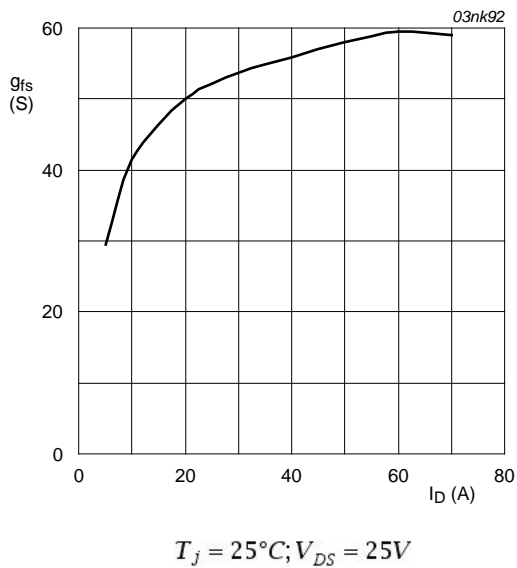


Fig 6. Forward transconductance as a function of drain current; typical values

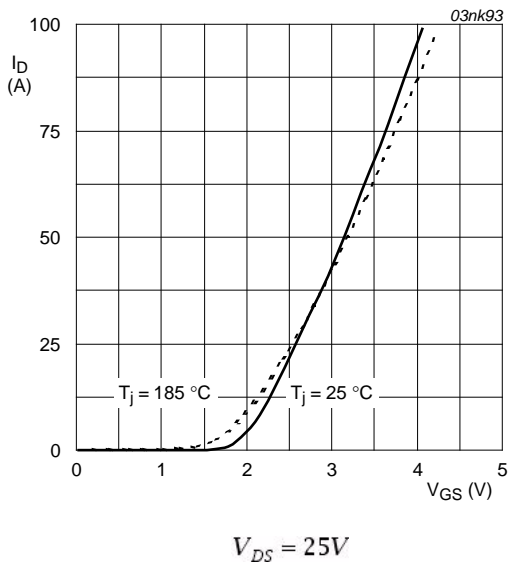


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

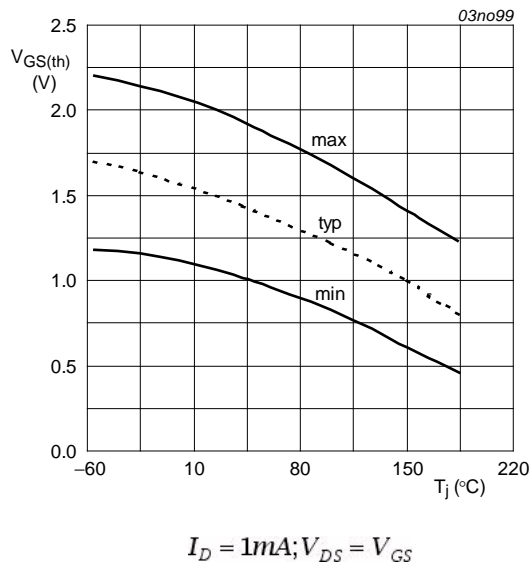
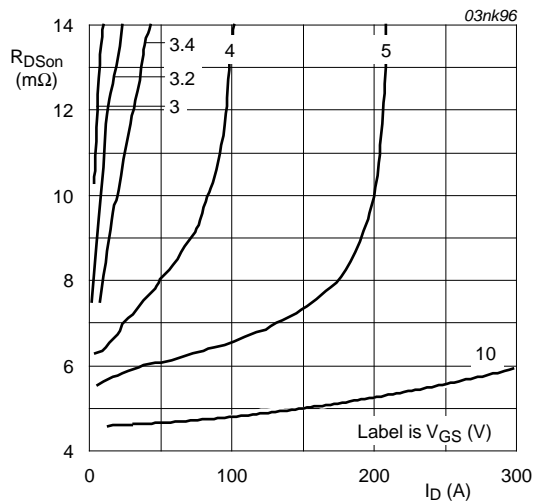
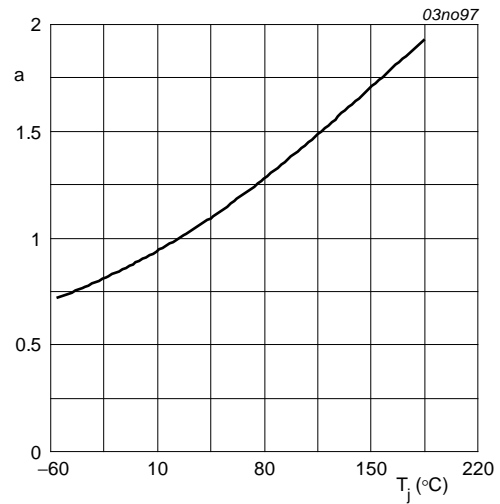


Fig 8. Gate-source threshold voltage as a function of junction temperature



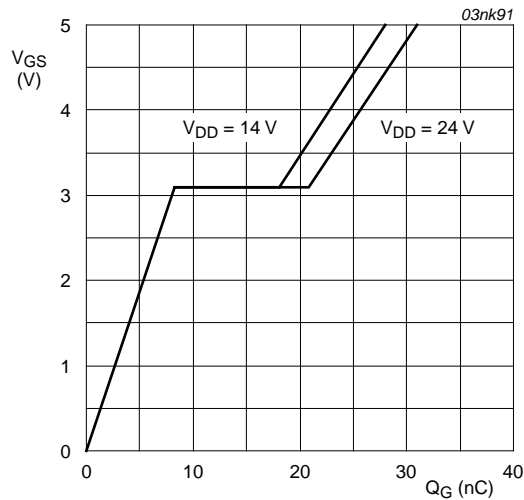
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



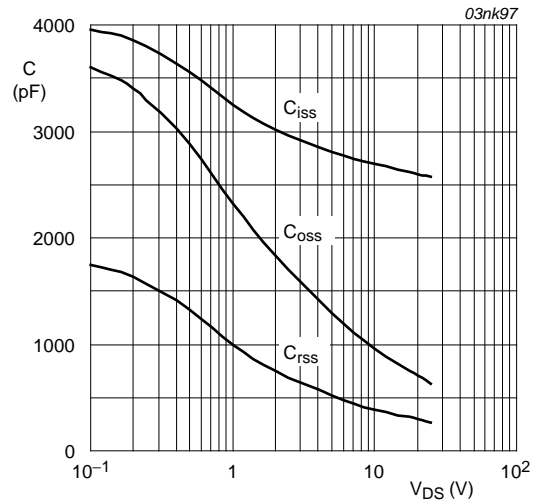
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

**Fig 11. Gate-source voltage as a function of turn-on gate charge; typical values**



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



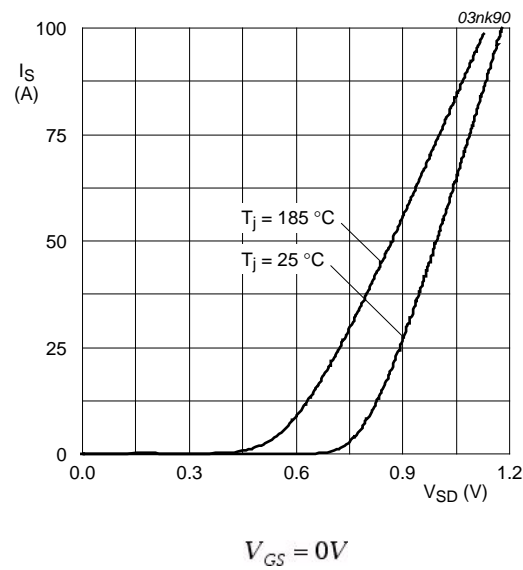


Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)
 SOT428

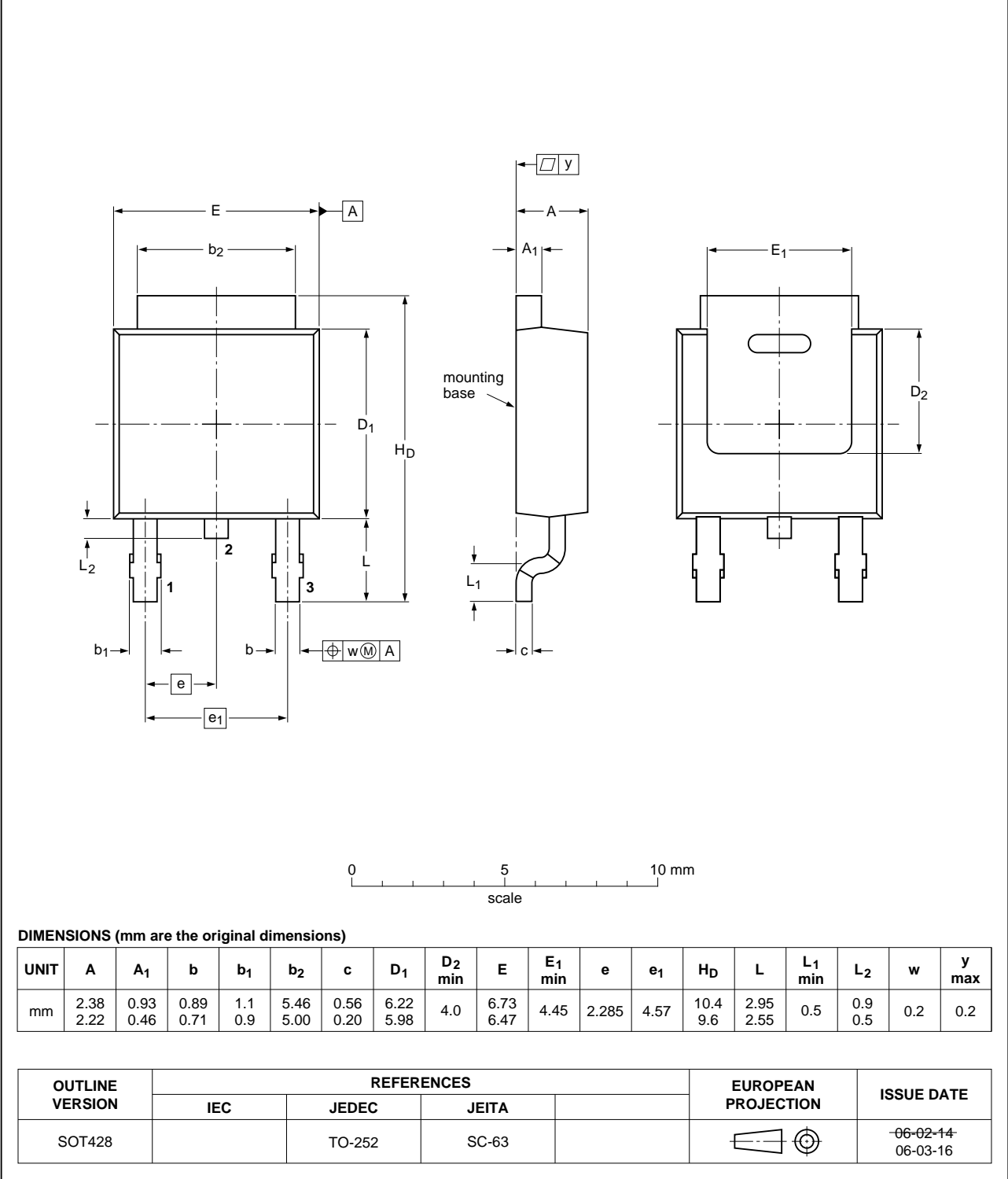


Fig 14. Package outline SOT428 (DPAK)

## 8. Revision history

**Table 7.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9207-30B v.3	20100616	Product data sheet	-	BUK9207-30B v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BUK9207-30B v.2 (9397 750 12233)	20031212	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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