LM1771 and LM3880 Based FPGA Power Supply Reference Design

National Semiconductor
Application Note 1677
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Introduction

The Xilinx Virtex™-5 FPGA is a family of advanced FPGAs that combine various platforms and speed grades enabling a high level of performance and flexibility[1-3]. This application note discusses the Virtex-5 FPGA power supply prerequisites in terms of the multiple voltage rail and current level requirements, output sequencing, and startup characteristics. Exemplarily, a power supply solution based on National Semiconductor LM1771 power supply controller and LM3880 sequencer is designed that combines high performance, power density and efficiency.

FPGA Power Supply Requirements

Nanoscale process technology used in the Virtex-5 FPGA enables the dynamic power dissipation (CV^2f) to be reduced by means of lower parasitic capacitances and lower core voltage rail[6], V_{CCINT}. Static power dissipation modes, via subthreshold and gate leakage[5,6], have been minimized by adding a third gate oxide thickness to the process. Fortunately, this is a net benefit in terms of the current levels demanded from the power supply solution.

The Virtex-5 generally requires at least three different voltage rails. The recommended core voltage is 1.0V ±5%. The I/O bank voltage supply, V_{CCO}, can vary from 1.14V to 3.45V depending on the I/O standard being implemented[2]. Thus, V_{CCO} voltage rails of 1.2V, 1.5V, 1.8V, 2.5V and 3.3V are feasible. Consequently, the overall power dissipation is application dependent and conditioned by ratios of static and dynamic power loss components. Additionally, Xilinx defines an auxiliary voltage, V_{CCAUX}, which is recommended to operate at 2.5V ±5% to supply FPGA clock rails related to the clock management tile blocks, e.g. the digital clock manager (DCM) resources[2].

The power-on sequence recommended by Xilinx is V_{CCINT}, V_{CCAUX}, and V_{CCO}. Although any monotonic power-on sequence is tolerated, use of the recommended sequence allows Xilinx to define the minimum inrush current required from the FPGA core, auxiliary and I/O supplies - denoted $I_{CCINTMIN}$, I_{AUXMIN}, and I_{CCOMIN}, respectively - to ensure correct power-on and configuration. It is possible that the power supplies must transiently handle larger currents during startup with relatively lower static and dynamic current levels during normal operation. The power-up ramp time specification - normally defined as the time from 10% to 90% of the nominal output voltage during startup - for all three voltage rails is 0.2 ms to 50.0 ms.

Note that the steady-state power supply demand can be derived pre-implementation by use of the Xilinx XPower Estimator (XPE) power estimation spreadsheet tool[4]. The junction temperature, frequency, device utilization and I/O types are included as parameters in this calculation so that designers can predict the power consumed by their system and design the power supply accordingly.

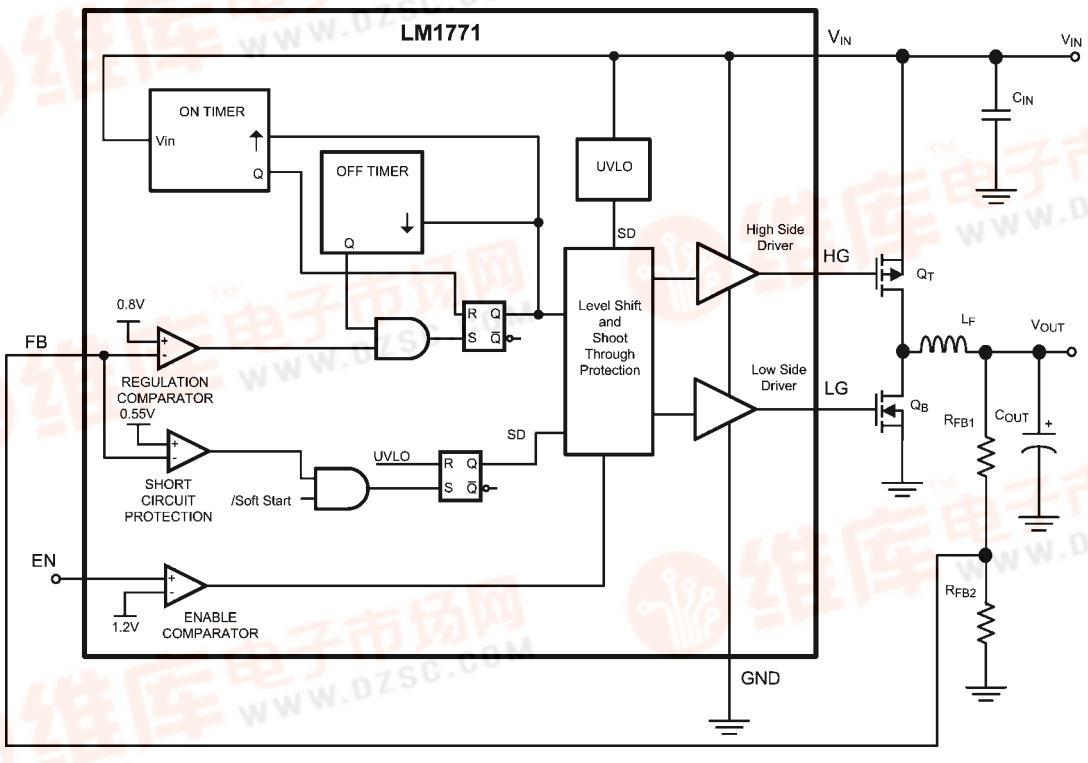


FIGURE 1. LM1771 DC-DC Buck Stage with COT Control Architecture

FPGA Power Supply Design Outline

The proposed FPGA power supply solution uses three National Semiconductor LM1771[9] PWM buck controllers with power-up and power-down of the individual voltage rails sequenced by a National Semiconductor LM3880[10] power sequencer.

The LM1771 block diagram with typical external connected components is presented in Figure 1. The LM1771 is an efficient buck converter switching controller available in MSOP-8 and LLP-6 packages and capable of converting an input voltage between 2.8V and 5.5V into a regulated output voltage as low as 0.8V. It drives an external high side PFET and low side NFET complementarily with duty cycle D and (1–D) respectively at switching frequency, f_s. A constant on-time (COT) control architecture is utilized which eliminates the need for an error amplifier and external compensation components. Thus, extremely fast transient load current response is possible. Additionally, the LM1771 features a precision enable pin to facilitate supply sequencing and/or flexibility in setting the operating input voltage range of the power supply.

Three LM1771 timing options - designated S, T and U in the part numbering specification - are available which translate to three possible switching frequency options for a given output voltage. For a given timing option, the switching frequency is largely independent of input voltage level as the controller input feed-forward feature varies high side switch on-time as a function of input voltage to maintain constant volt-seconds at the switch node.

By virtue of the small-sized package options, the LM1771 allows for a complete power supply design to occupy very little PCB real estate without sacrificing efficiency.

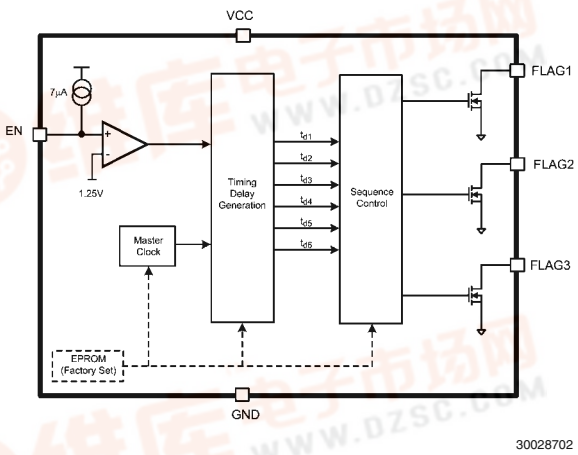


FIGURE 2. LM3880 Sequencer Block Diagram

The LM3880 sequencer block diagram is presented in Figure 2. It is available in a SOT23-6 package and it has three open-drain flag outputs which allow control of the three LM1771 enable pins. Upon enabling the LM3880, the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch conditions. Standard timing options of 10 ms, 30 ms, 60 ms and 120 ms are available. Further, the LM3880 is factory programmable to attain customized timing options combined with six possible power down sequences. The LM3880 operating supply voltage range, 2.7V to 5.5V, is compatible with that of the LM1771 controller.

FPGA Power Supply Implementation

The power train schematic based on the LM1771 controller and LM3880 sequencer is shown in Figure 3. The associated bill of materials is presented in Table 1.

The LM1771 based application board was designed with the input voltage nominally set at 5.0V, but can theoretically be varied over the entire operating range of the LM1771 (2.8V-5.5V). The entire power supply occupies less than 2.0" x 2.0" on a two layer FR4 PCB. For this design, the three buck regulator channels are capable of delivering maximum continuous load currents of 5A, 3A and 3A (I_{CCO}, I_{CCAUX}, and I_{CCINT}, respectively).

The I/O voltage is set at 3.3V, but can be easily varied by modifying one of the feedback resistors, RFB13 or RFB23. In the case of a buck converter to maintain regulation at 3.3V, the input voltage should not be allowed to fall below approximately 3.6V. The core and auxiliary rails are set at 1.0V and 2.5V, respectively, according to the FPGA specification.

The core, auxiliary and I/O regulators use the LM1771S (U1), LM1771T (U2) and LM1771U (U3) controllers which yield switching frequencies of 606 kHz, 758 kHz and 500 kHz, respectively. Each supply has its own input filter capacitor located as close as possible to the p-channel and n-channel buck and synchronous power FETs. Additionally, a small 0603 input bypass capacitor is placed local to each LM1771 IC.

The output filter capacitances on the core and I/O supplies are tantalum based and chosen to present the necessary ESR to maintain sufficient in-phase voltage ripple at the FB pin[9, 11, 12]. In the case of the I/O channel, feed-forward capacitor C_{F3} increases the magnitude of the FB ripple seen by its LM1771. This capacitor is not used in the core channel feedback circuit as it has minimal effect when the output voltage is close to the FB pin voltage. The output filter capacitance of the auxiliary voltage regulator is ceramic based to minimize the noise level of this rail. A current sense network comprising resistor R_{F1} and capacitor C_{F1} across filter inductor L_{F2} creates a triangular voltage waveform which is ac coupled by capacitor C_{F2} to the FB node[9]. A comprehensive discussion of the selection process for these components is available in National Semiconductor Application Note AN-1481.

This circuit can also be utilized in the core and I/O channels if tantalum capacitors are deemed unsuitable and/or low ESR ceramic capacitors are required either local to the regulator or downstream adjacent to the FPGA.

The filter inductors are designed for large current handling capability with low DC and AC effective resistance to maximize efficiency. The inductance value is conditioned to attain peak-to-peak ripple current of approximately 30% of the rated load current[13]. Further, the inductors chosen boast a relatively soft inductance-current saturation characteristic. This represents an ideal component characteristic when faced with short duration high current transient events in excess of the rated load current.

TSOP6 packages are used for the power FETs in the auxiliary rail supply while SO-8 FETs are implemented for the I/O channel regulator. The core voltage supply, given its low duty cycle operating point, has a high side TSOP6 FET, Q_{T1}, and a low side SO-8 FET, Q_{B1}. Note that by employing more thermally efficient packages and/or lower on-resistance switches, the possibility exists to increase maximum load current capability and thermal performance.

The LM3880 sequencer 30 ms timing option, designated -1AB, is recommended. External pull-up resistors are connected to each open-drain flag output.

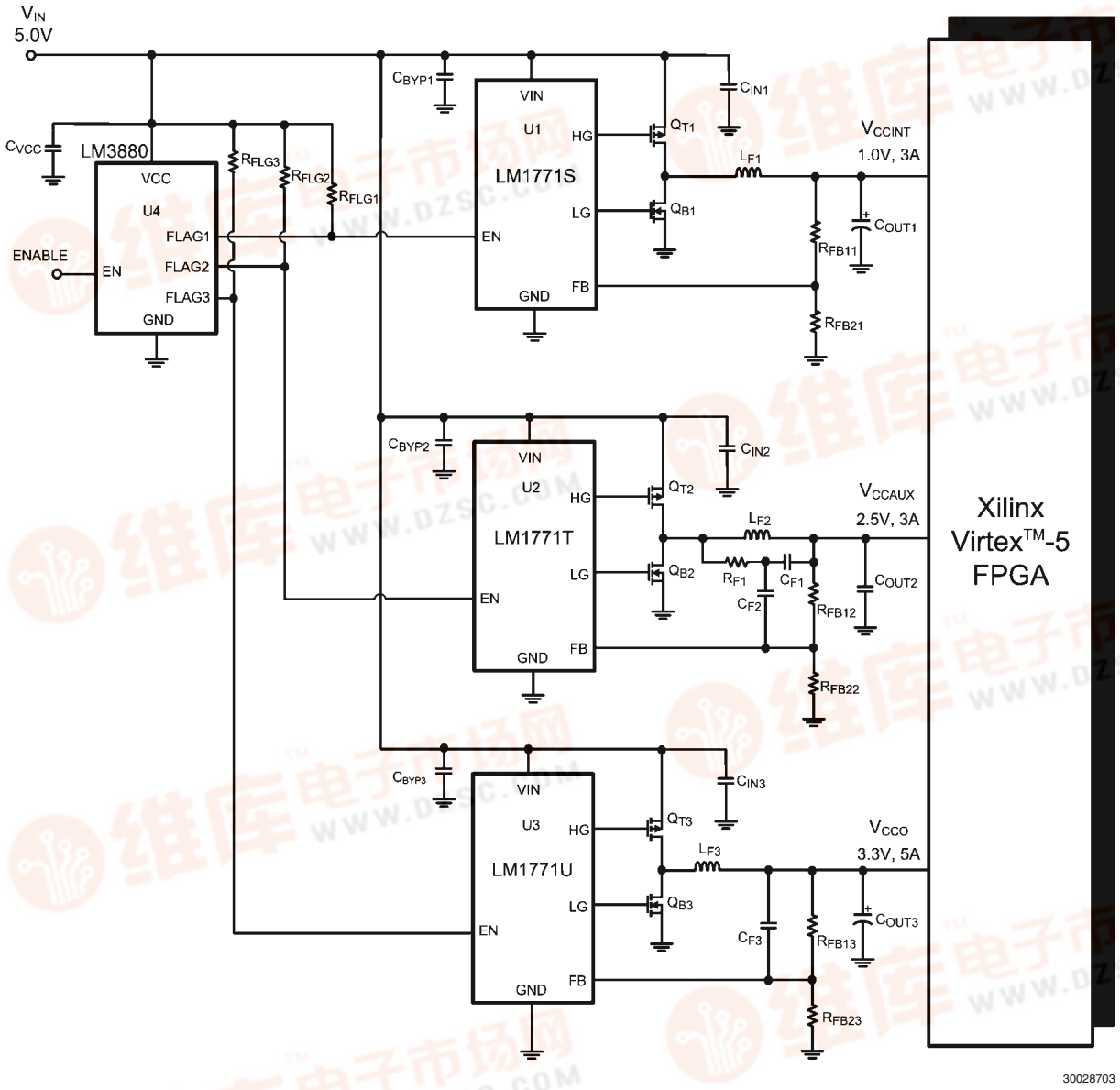


FIGURE 3. Virtex-5 FPGA Power Train Schematic

Virtex-5 LM1771 Based Power Supply Bill of Materials

Ref. Des.	Description	Part Number	Manufacturer
U1	LM1771S, 500 ns, PWM Controller	LM1771SMMX	National Semiconductor
U2	LM1771T, 1000 ns, PWM Controller	LM1771TMMX	National Semiconductor
U3	LM1771U, 2000 ns, PWM Controller	LM1771UMMX	National Semiconductor
U4	LM3880 Power Sequencer	LM3880MFX-1AB	National Semiconductor
Q_{T1}	High Side PFET, TSOP6	Si3867DV	Vishay Siliconix
Q_{B1}	Low Side NFET, SO-8	Si4394BDY	Vishay Siliconix
Q_{T2}	High Side PFET, TSOP6	Si3867DV	Vishay Siliconix
Q_{B2}	Low Side NFET, TSOP6	Si3460DV	Vishay Siliconix
Q_{T3}	High Side PFET, SO-8	Si9424BDY	Vishay Siliconix
Q_{B3}	Low Side NFET, SO-8	Si4394BDY	Vishay Siliconix
C_{IN1}	22 µF 6.3V X5R Ceramic Capacitor, 0805	C2012X5R0J226M	TDK
C_{IN2}	22 µF 6.3V X5R Ceramic Capacitor, 0805	C2012X5R0J226M	TDK
C_{IN3}	47 µF 6.3V X5R Ceramic Capacitor, 1206	C3216X5R0J476M	TDK
C_{BYP1}	1 µF 10V X5R Ceramic Capacitor, 0603	C1608X5R1A105M	TDK
C_{BYP2}	1 µF 10V X5R Ceramic Capacitor, 0603	C1608X5R1A105M	TDK
C_{BYP3}	1 µF 10V X5R Ceramic Capacitor, 0603	C1608X5R1A105M	TDK
C_{OUT1}	150 µF 6.3V Tantalum Capacitor, 50 mΩ, D-Case	TPSD157M006R0050	AVX
C_{OUT2}	100 µF 6.3V X5R Ceramic Capacitor, 1210	C3225X5R0J107M	TDK
C_{OUT3}	150 µF 6.3V Tantalum Capacitor, 50 mΩ, D-Case	TPSD157M006R0050	AVX
L_{F1}	2.2 µH Inductor, 6.86mm x 6.47mm x 3.0mm	IHLP2525CZER2R2M01	Vishay Dale
L_{F2}	2.2 µH Inductor, 6.86mm x 6.47mm x 3.0mm	IHLP2525CZER2R2M01	Vishay Dale
L_{F3}	2.2 µH Inductor, 11.5mm x 10.3mm x 4.0mm	IHLP4040DZER2R0M11	Vishay Dale
R_{FB11}	2.32 kΩ Resistor, 0603	CRCW06032321F	Vishay
R_{FB21}	10 kΩ Resistor, 0603	CRCW06031002F	Vishay
R_{FB12}	21 kΩ Resistor, 0603	CRCW06032102F	Vishay
R_{FB22}	10 kΩ Resistor, 0603	CRCW06031002F	Vishay
R_{FB13}	30.9kΩ Resistor, 0603	CRCW06033092F	Vishay
R_{FB23}	10 kΩ Resistor, 0603	CRCW06031002F	Vishay
C_{F1}	1 nF Capacitor, X7R, 0603	VJ0603102KXXA	Vishay
C_{F2}	22 nF Capacitor, X7R, 0603	VJ0603223KXXA	Vishay
C_{F3}	1 nF Capacitor, X7R, 0603	VJ0603102KXXA	Vishay
C_{VCC}	1 µF 10V Ceramic Capacitor, 0603	C1608X5R1A105M	TDK
R_{F1}	49.9 kΩ Resistor, 0603	CRCW06034992F	Vishay
R_{FLG1}	49.9 kΩ Resistor, 0603	CRCW06034992F	Vishay
R_{FLG2}	49.9 kΩ Resistor, 0603	CRCW06034992F	Vishay
R_{FLG3}	49.9 kΩ Resistor, 0603	CRCW06034992F	Vishay

FPGA Power Supply performance

The efficiency of the core, auxiliary and I/O buck regulator channels, operating independently at 5V input, as a function of current are shown in Figure 4, Figure 5 and Figure 6, respectively. Likewise, typical full load efficiencies are 80.6%, 89.1% and 93.2%. Global conversion efficiency with the three regulators operating at full load, including LM3880 related bias power, is 90.5%. This constitutes a total output power of 27W with 2.85W dissipation. When the LM3880 is disabled (EN pin less than 1.25V), the total quiescent current is approximately 1.5mA. Finally, Figure 7(a) and (b) demonstrate the sequenced monotonic power up and power down characteristics of each voltage rail as controlled by the LM3880. The time delays between enable transitioning and subsequent output voltages in regulation - defined as 90% V_{ENABLE} to 90% V_{CCINT}, or 90% V_{CCINT} to 90% V_{CCAUX}, etc. - are 30 ms.

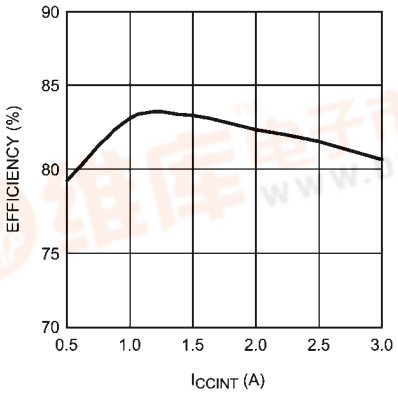


FIGURE 4. Core Channel Efficiency vs. Current, I_{CCINT}; V_{IN} = 5.0V

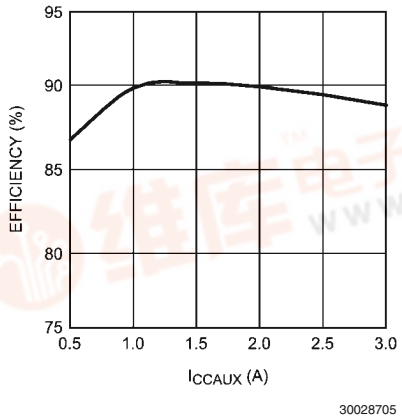


FIGURE 5. Auxiliary Channel Efficiency vs. Current, I_{CCAUX}; V_{IN} = 5.0V

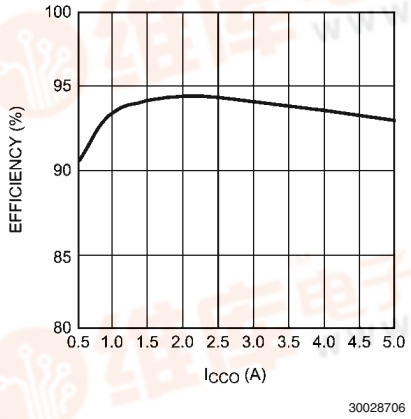
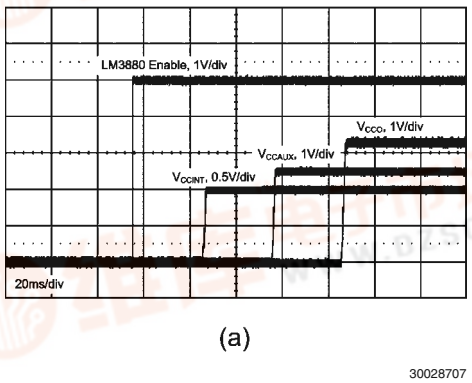


FIGURE 6. I/O Channel Efficiency vs. Current, I_{CCO}; V_{IN} = 5.0V



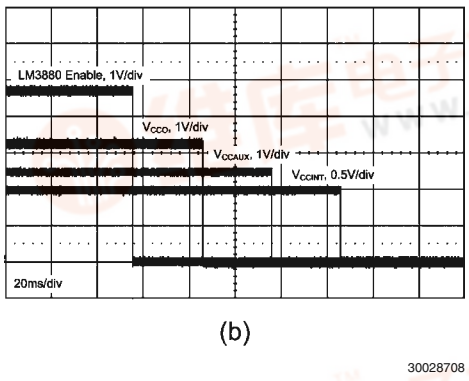


FIGURE 7. Sequenced Monotonic Startup / Shutdown Characteristic; V_{IN} = 5.0V

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Notes

Notes

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