LM2832X 6-Pin LLP Demo Board

National Semiconductor
Application Note 1552
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Introduction

The demo board included in this shipment converts 3V to 5.5V input to 1.8V output for 2A load current using the LM2832X 1.6 MHz DC-DC switching converter. This is a 4-layer board using the internal layers as a VIN plane and Ground plane.

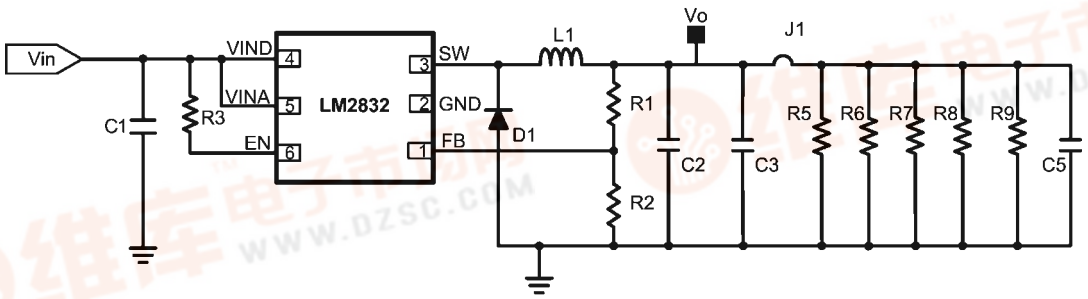
A bill of materials below describes the parts used on this demo board. A schematic and layout have also been included below along with measured performance characteristics. The above restrictions for the input voltage are valid only for the demo board as shipped with the demo board schematic below.

Operating Conditions

V_{IN} = 3V to 5.5V

V_O = 1.8V

I_O = 2A



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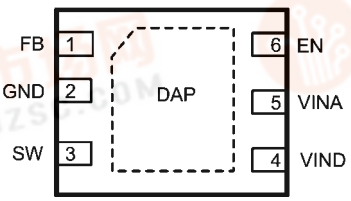
LM2832X 6-Pin LLP Demo Board Schematic

Pin-Out



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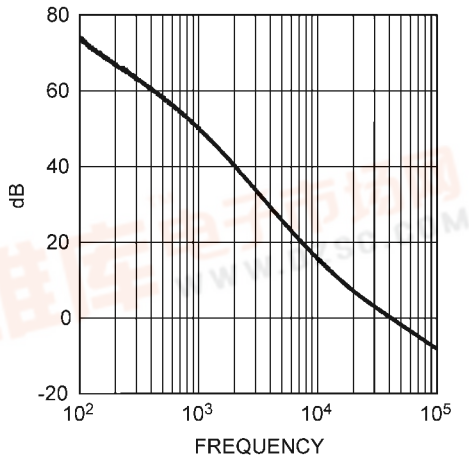
Pin Description 6-Pin LLP

Pin	Name	Function
1	FB	Feedback pin. Connect to external resistor divider to set output voltage.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	SW	Output switch. Connect to the inductor and catch diode.
4	VIND	Power Input supply.
5	VINA	Control circuitry supply voltage. Connect VINA to VIND on PC board.
6	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VINA + 0.3V.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

LM2832 Gain/Phase 5V to 1.8V @ 1A



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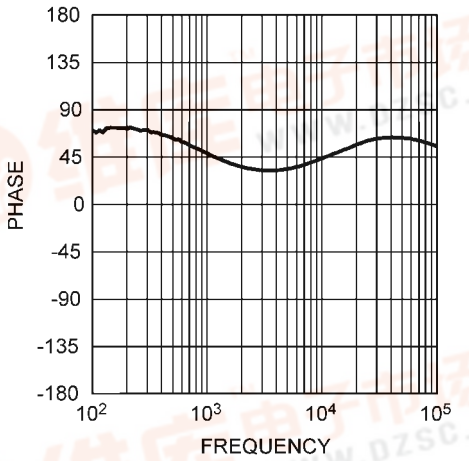

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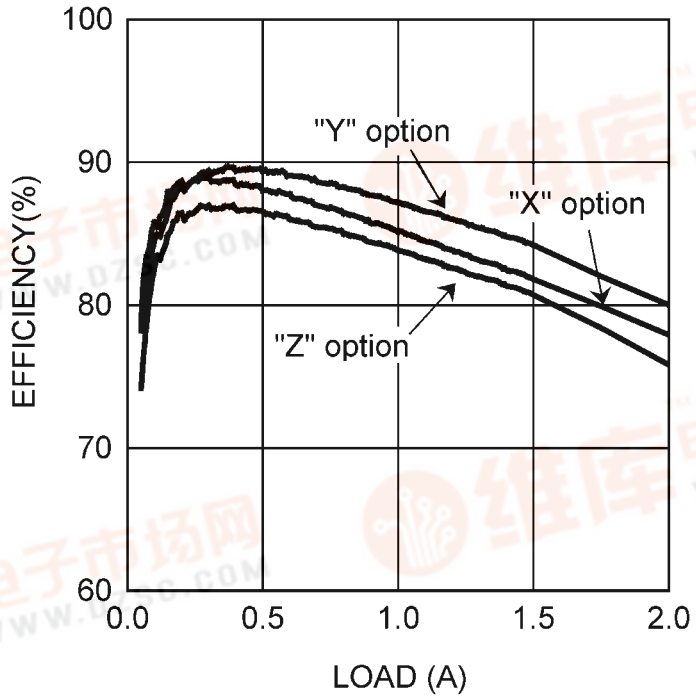
LM2832 Efficiency: Vin = 3.3V, Vo = 1.8V



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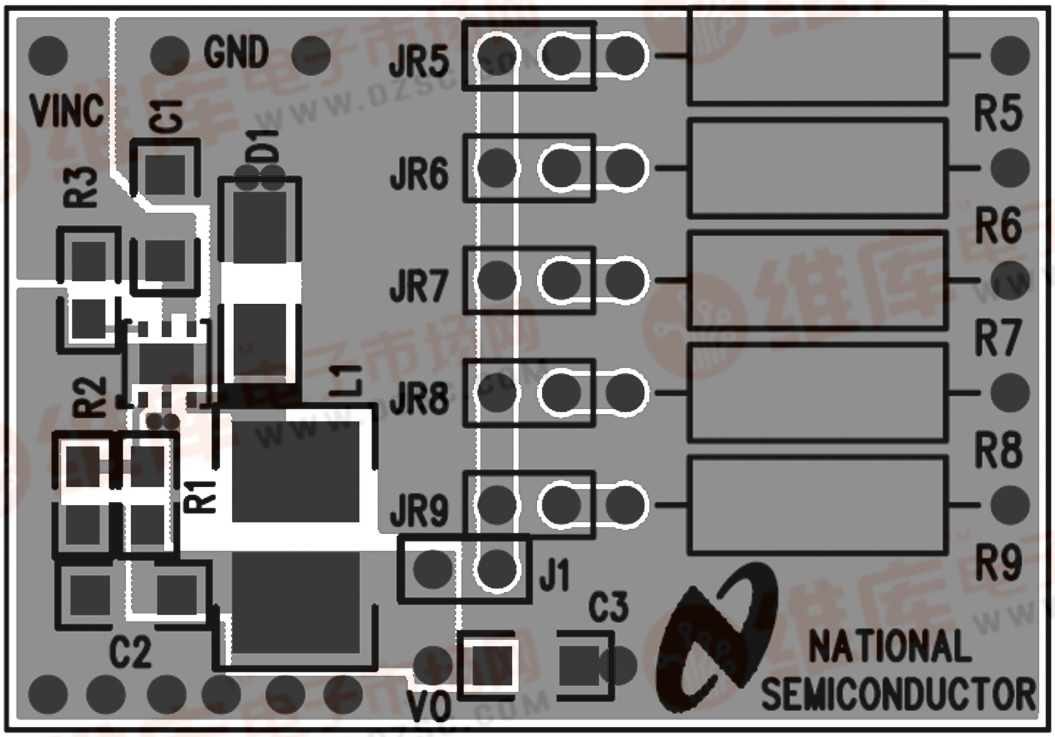
Bill Of Materials LM2832X-Version

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	NSC	LM2832X
C1, Input Cap	22 µF, 6.3V, X5R	TDK	C3216X5ROJ226M
C2 Output Cap	22 µF, 6.3V, X5R	TDK	C3216X5ROJ226M
C3 Output Cap	22 µF, 6.3V, X5R	TDK	C3216X5ROJ226M
D1, Catch Diode	0.3V_f Schottky 1.5A, 30V_R	TOSHIBA	CRS08
L1	3.3 µH, 3.5A	CoilCraft	MSS7341-332NL
R1	20.0 kΩ, 1%	Vishay	CRCW08052002F
R2	10.0 kΩ, 1%	Vishay	CRCW08051002F
R3	20.0 kΩ, 1%	Vishay	CRCW08052002F
J1	No Load		
R5 – R9	No Load		

Layout



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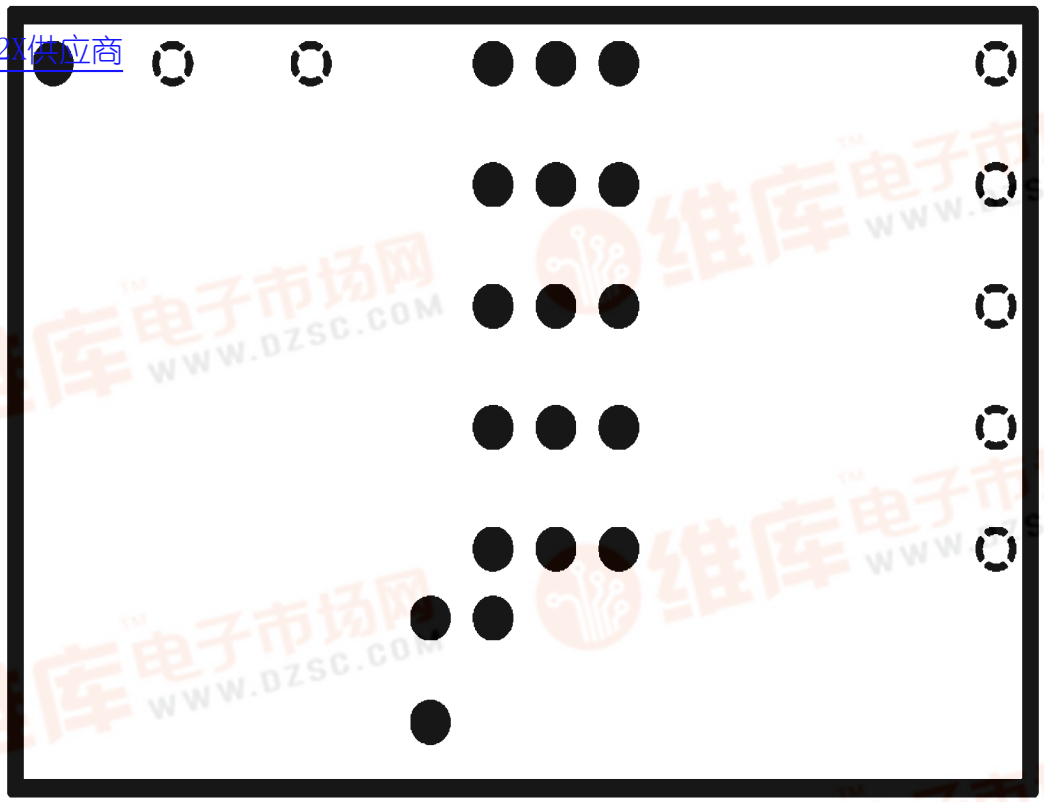
Top Layer



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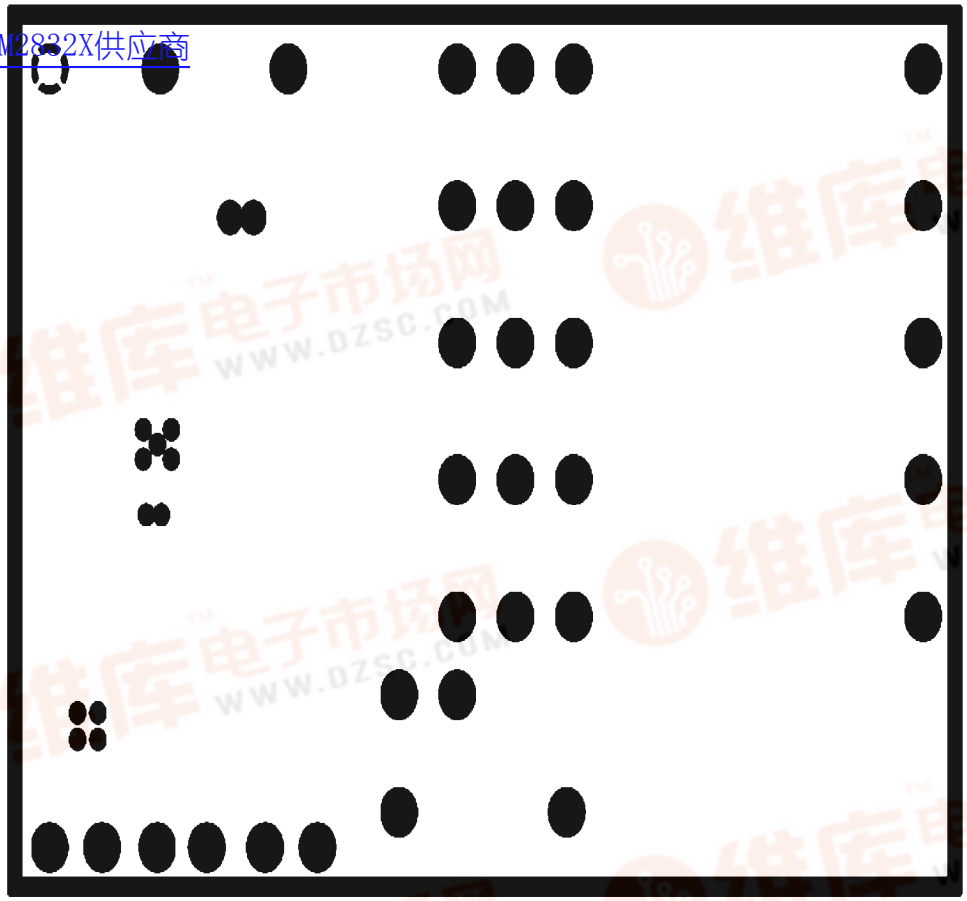
Internal Plane 1 (GND)



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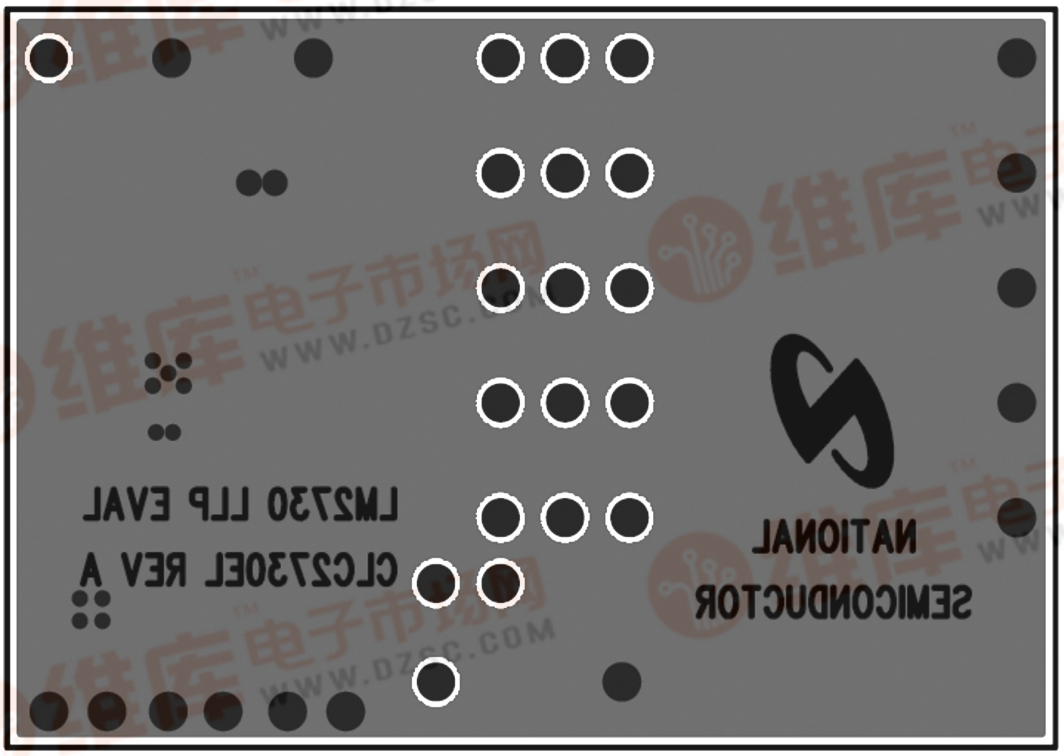
Internal Plane 2 (V_{IN})



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Bottom Layer

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