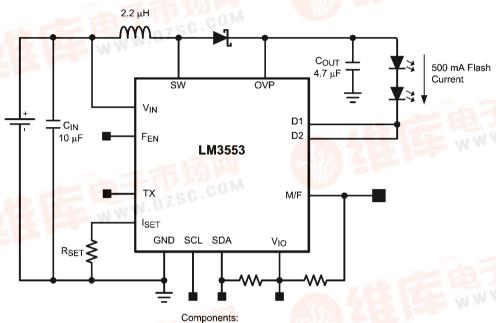
# LM3553 1.2A Dual Flash LED Driver System with I2C Compatible Interface

National Semiconductor Application Note 1780 March 12, 2008



# **Typical Application Drawing**



L = Toko FDSE0312-2R2M

CIN = Murata GRM188R60J106ME47D

COUT = Murata GRM21BR61E475KA12L

LEDs = Lumileds LXCL – PWF3

Or equivalent

30049620

# **Bill of Materials**

Component Symbol	Value	Package	Man <mark>ufacturer</mark>	Part #
LM3553	二曲子	SDF12A LLP12	National	LM3553SDX
LM3553 Evaluation Board	-WWA	1.02-	National	551600092-001 RevA
LED1,LED2	White LED		Philips Lumiled	LXCL-PWF3
CIN	10μF, 6.3V	0603	Murata	GRM188R60J106ME47D
COUT	4.7µF, 25V	0805	Murata	GRM21BR61E475KA12L
L1	2.2µH	3mm x 3mm x 1.2mm	Toko	FDSE0312-2R2M
RSET	33kΩ	0402	Vis <mark>hay Dale</mark>	CRCW040233K0FKED
D1	1.5A, 30V	- TD MOOM	ROHM	RB070M-30
RSDA, RSCL, RFEN, RMF, RTX	10kΩ	0402	Vishay Dale	CRCW040210K0JNED

AN-1780

## Schematic 查询LM3553供应商 LXCL-PWF3 LXCL-PWF3 ISET ISET MF DI D2 ISET FEN SDA $10 \text{ k}\Omega$ VIN VIN VIO VIO. R3 RSET DAPGND XX RMF swł SW SCL -Isa 10 kΩ CRCW040233K0FKED OVP ΤX RTX 2 4 6 8 10 12 14 16 3 5 7 9 11 13 15 SDA 1234567 SDA OIV

**LM3553 Evaluation Board Layout** 

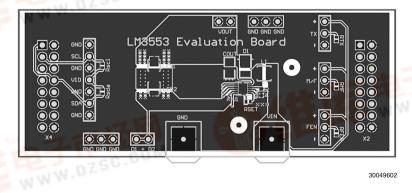
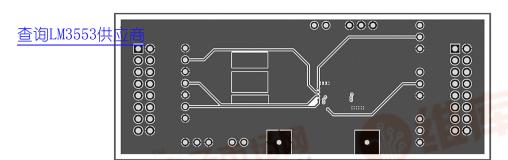


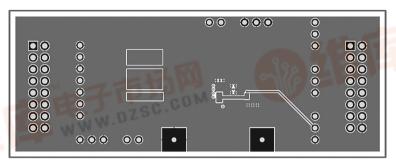
FIGURE 1. Top Layer

找一PDF 维库一下



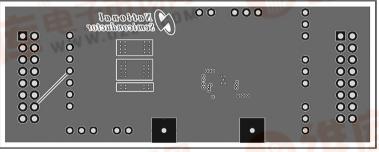
30049604

FIGURE 2. Mid-Layer 1



30049605

FIGURE 3. Mid-Layer 2



30049603

FIGURE 4. Bottom Layer (unmirrored)

# **Board Operation**

# BASIC CONNECTIONS

To operate the LM3553 1.2A Dual Flash LED Driver System with I2C Compatible Interface, connect a supply voltage (2.7V-5.5V) between board connectors VIN and GND and attach an I2C interface using one of the methods described in the EXTERNAL CONTROL INTERFACE SECTION of this document.

Default Jumper Connections:

- M/F: Connected to "-". To enable the LM3553 evaluation board, connect the M/F header to the '+' using the provided jumper. This will place the LM3553 evaluation board into normal operation mode and out of Hardware Reset
- TX: Connected to "-". By default, this setting will allow the full-scale flash to occur. Moving the TX jumper to the "+"

- position during a flash will force the LM3553 in a lower current TX mode. This TX mode level is equal to the level stored in the Torch Control Register.
- FEN: Connected to "-". By default, this setting will not allow an externally controlled flash even to occur. Moving the FEN jumper to the "+" position will start a flash event. The flash event will remain active until the FEN pin is driven back to the "-" position or the internal timeout time lapses, which ever occurs first.

With the default jumper connections made, the board will be ready to operate once an input voltage and an I2C interface generator (external or USB docking board) are connected. NOTE: For the evaluation board to work properly, the OVP bit in the Multi-Function/Options Register must be set to a 1 (18.9V OVP). If this bit is not enabled, the part



# **EXTERNAL CONTROL INTERFACE CONNECTION**

The LM3553 Evaluation Board provides two ways to connect an I<sup>2</sup>C compatible interface to the LM3553 IC. The first method to connect the interface is through a set of connectors on the bottom of the evaluation board that allow the board to plug into National's USB interface board directly. The second method of interface connection is through a header strip located on the left hand side of the evaluation board. There are pins available to connect VIO (contoller reference voltage), SCL (Interface Clock Line), and SDA (Interface Data Line) each separated by a ground pin. The evaluation board has two external pull-ups that connect both SCL and SDA to VIO to compliment the open drain inputs found on the LM3553. The OPERATION DESCRIPTION section of this application note describes the internal registers and I<sup>2</sup>C compatible interface in greater detail.

#### **OPERATION DESCRIPTION**

#### I<sup>2</sup>C Compatible Interface

#### **DATA VALIDITY**

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

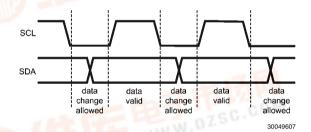


FIGURE 5. Data Validity Diagram

A pull-up resistor between VIO and SDA must be greater than [  $(VIO-V_{OL})$  / 3.7mA] to meet the  $V_{OL}$  requirement on SDA. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

#### START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I<sup>2</sup>C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP conditions. The I<sup>2</sup>C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

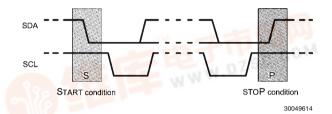


FIGURE 6. Start and Stop Conditions

#### TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3553 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3553 generates an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3553 address is 53h. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

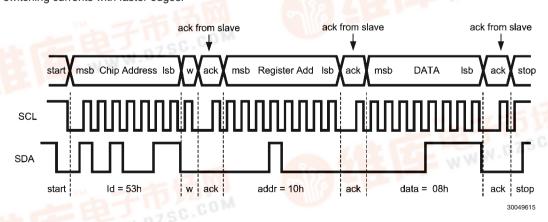


FIGURE 7. Write Cycle

w = write (SDA = "0")

ack = acknowledge (SDA pulled down by the slave)

id = chip address, 53h for LM3553

技 作 MEE — N

#### I2C COMPATIBLE CHIP ADDRESS

The characters for BM \$553 唐 1010011, or 53hex.

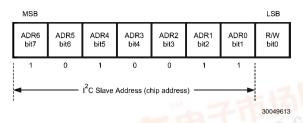


FIGURE 8.

#### **INTERNAL REGISTERS OF LM3553**

Register	Internal Hex Address	Power On Value
General Purpose Register	0x10	0001 1000
Multi-Function Pin Control Register	0x20	1110 0000
Current Step Time Register	0x50	1111 1100
Torch Current Control Register	0xA0	1000 0000
Flash Current Control Register	0xB0	1000 0000
Flash Duration Control Register	0xC0	1111 0000

### **General Purpose Register**

MSB		General Purpose Control Register Address: 0x10 LSB							
0	0	VFB	1	1	VM	EN1	EN0		
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		

30049608

# FIGURE 9.

EN0-EN1: Set Flash LED mode

Indicator Mode sets  $I_{LED} = 20$ mA. In this mode, D1 is enabled and D2 is disabled.

VM: Enables Voltage Mode. Current sinks D1 and D2 are turned off and the LM3553 will operate in a regulated voltage boost mode. Setting the VM bit to a '1' does not override the EN0 and EN1 bits stored in the general purpose register. The default setting is '0'. If the LM3553 is in Voltage Mode and an indicator, torch or flash command is issued, the LM3553 will turn on the D1 and D2 current sources and begin regulating the output voltage to a value equal to VFB (350mV or 450mV) + VLED.

VM	EN1	EN0	Function
0	0	0	Shutdown
0	0	1	Indicator Mode
0	1	0	Torch Mode
0	1	1	Flash Mode
1	0	0	Voltage Mode
01∖}}	0	1	Indicator Mode
1	1	0	Torch Mode
1	1	1	Flash Mode

**VFB**: Selects the regulation voltage for the LM3553. Setting this VFB bit to a '0' sets the regulation voltage to 450mV while setting the VFB bit to a '1' sets the regulation voltage to 350mV. Setting the VFB bit to a '1' during torch mode and/or lower current flash modes ( $I_{\rm LED}$  < 1A) will help improve the LED efficiency of the LM3553.

#### M/F Pin Control Register

MSB	Multi-Function Pin Control/Options Register Address: 0x20 LSB							
1	1	1	OCL	OVP	DATA	MODE	RESET	
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	

30049612

#### FIGURE 10.

**RESET**: Enables M/F as hardware RESET. '0' = Hardware RESET, .'1' = GPIO or current sink depending on the MODE bit. Default = '0'

**MODE**: Sets M/F mode. Default for MODE = '0'. '0' = GPI, and'1' = GPO

Note: When M/F is configured as an input, data is transfered from GPI to DATA whenever an I<sup>2</sup>C write command is issued to the LM3553. When configuring M/F as a GPO, the first write needs to take the LM3553 out of RESET mode and a second write can then set the pin to the GPO.

**DATA**: GPIO Data. When the M/F is configured as an output (GPO), DATA sets the GPO level. Example: DATA = '1', M/F is set high or logic '1'. When the M/F pin is configured as an input (GPI), DATA stores the GPI level. Example: M/F = '1', DATA will be set to a '1'. Default for DATA = '0'.

**OVP**: Enables high-voltage OVP (OVP Bit ='1') or low-voltage OVP (OVP Bit ='0'). Default = low-voltage mode '0'

**OCL**: SW Pin Current Limit Selector Bit: If OCL = '0', the inductor current limit is 2.5A typ. If OCL = '1', the inductor current limit is 1.7A typ.

# M/F Functionality Configuration Table

RESET	MODE	M/F Function
0	Х	RESET
1	0	GPI
1	1	GPO

# **Current Step Time Register**

MSB	Current Step Time Register Address: 0x50 LSB							
1	1	1	1	1	1	ST1	ST0	
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	

30049616

### FIGURE 11.

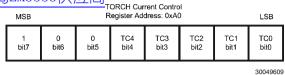
**ST1-ST0**: Sets current level stepping time for D1 and D2 during the beginning and end of the flash or torch current waveform.  $'00' = 25\mu s$ ,  $'01' = 50\mu s$ ,  $'10' = 100\mu s$ ,  $'11' = 200\mu s$ .

The current ramp-up/ramp-down times can be approximated by the following equation:

 $T_{RAMPUP/RAMPDOWN} = (N_{FLASH} - N_{START} + 1) \times t_{STEP}$  where N is equal to the decimal value of the brightness level (0  $\leq$   $N_{FLASH} \leq$  127 and 0  $\leq$   $N_{START} \leq$  31).  $N_{START} = N_{TORCH}$  if Torch is enabled before going into a flash. If going straight into a flash from an off-state,  $N_{START} = 0$ 

# **Torch Current Control Register**

≦询LM3553供应商



#### FIGURE 12.

TC6-TC0: Sets Torch current level for D1 and D2. xxx1 1111 = Full-scale

# Flash Current Control Register

MSB	FLASH Current Control Register Address: 0xB0 LSB							
1	FC6	FC5	FC4	FC3	FC2	FC1	FC0	
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	

30049610

6

#### FIGURE 13.

FC6-FC0: Sets Flash current level for D1 and D2, x111 1111 = Full-scale

# **Current Level Equation**

The Full-Scale Flash Current Level is set through the use of an external resistor ( $R_{SET}$ ) connected to the  $I_{SET}$  pin. The R<sub>SET</sub> selection equation can be used to set the current through each of the two current sinks, D1 and D2.

$$R_{SET} = 6770 \times 1.24V \div I_{Dx}$$

# **R<sub>SFT</sub> Selection Table**

I <sub>Flash</sub> = ID1 + ID2	R <sub>SET</sub>
500mA	33.6kΩ
600mA	28kΩ
1A	16.8kΩ
1.2A	14kΩ

The current through each current sink, D1 and D2, can be approximated by the following equation using the values stored in either the Torch or Flash Current Control registers.

# I<sub>FLASH</sub>≊ (N + 1) × I<sub>LED\_TOTAL</sub> ÷ 128

where N is the decimal equivalent number ( $0 \le N \le 127$  for Flash and  $0 \le N \le 31$  for Torch) stored in the Torch or Flash Current control registers and  $I_{LED\_TOTAL} = I_{D1} + I_{D2}$  @ Full-scale. Brightness codes 0 through 4 are repeated and each sets the total LED current to approximately 40mA.

# Flash Safety Timer Control Register

мѕв		FLASH Duration Control Register Address: 0xC0 LSB							
1 bit7	1 bit6	1 1 1 FD3 FD2 FD1 FD0 bit6 bit5 bit4 bit3 bit2 bit1 bit0							

FIGURE 14.

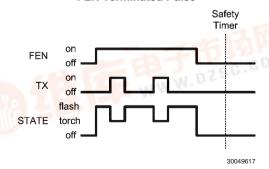
FD3-FD0: Sets Flash Duration for D1 and D2. 1111 = Fullscale

Safety Timer Duration Code (Binary)	Typical Safety Timer Duration (milliseconds)
0000	50
0001	100
0010	200
0011	300
0100	400
0101	500
0110	600
0111	700
1000	800
1001	900
1010	1000
1011	1100
1100	1200
1101	1300
1110	1400
1111	3200

# LM3553 Functionality Truth Table

LINGSOST Unclionality Truth Table								
EN1	EN0	F <sub>EN</sub>	T <sub>X</sub>	Result				
0	0	0	0	Shutdown				
0	0	0	1	Shutdown				
0	0	1	0	Flash				
0	0	1	1W	Torch				
0	1	0	0	Indicator				
0	1	0	1	Indicator				
0	1	1	0	Flash				
0	1	1	1	Torch				
1	0	0	0	Torch				
1	0	0	1	Torch				
1	0	1	0	Flash				
1	0	1	1	Torch				
1	1	0	0	Flash				
9.1	1	0	1	Torch				
1	1	1	0	Flash				
1	1	1	1	Torch				

# **FEN Terminated Pulse**



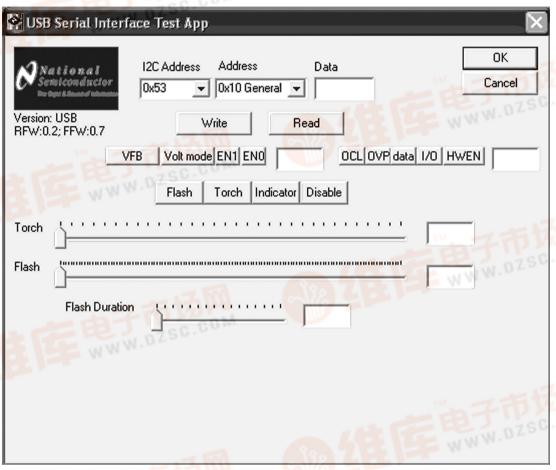
# Software Interface Information

前 M3553供应商 morder to fully evaluate the LM3553 part, an "I<sup>2</sup>C Compatible" interface must be used for any functionality to occur. A detailed description of the interface control is described in the LM3553 datasheet.

National has created an I2C compatible interface generation program and USB docking board that can help exercise the part in a simple way. Contained in this document is a description of how to use the USB docking board and interface software.

The LM3553 evaluation board has the means to "plug into" the USB docking board. The USB docking board provides all of the control signals for the simple interface. Power to the part must be provided externally. A standard USB cable must be connected to the board from a PC.

The I<sup>2</sup>C compatible interface program provides all of the control that the LM3553 part requires. For proper operation, the USB docking board should be plugged into the PC before the interface program is opened. Once connected, and the program is executed, a basic interface window will open.



**GUI Start-Up** 

30049621

Data

At the top of the interface, the user can read or write to any of the data registers on the LM3553 part using the two pull down menus (for the slave i.d. and the desired data address), the data field, and the read and write buttons.



12C Address

0x53

0x20 GPI0 0xA0 Torch Bri	D VI
Drop Down Menu	30049623

Just below the pull down menus are convenient toggle buttons to set/reset the control bits in the Control Registers.

Address

0x10 General

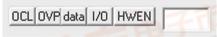
0x10 General



30049624



- VFB: Toggles the Feedback voltage between 450mV (default) and 350mV. When are ssed, the feedback voltage will be set to 350mV.
- Volt Mode: Places the LM3553 into voltage output mode. When depressed, the part will output 4.98V.
- EN1 and EN0: These bits place the part into either shutdown, indicator, torch or flash. '00' = Shutdown, '01'=Indicator, '10'=Torch, '11'=Flash.



30049625

- OCL: Toggles the inductor current limit between 2.5A (default) and 1.7A. When the OCL button is depressed, the current limit will be set to 1.7A
- OVP: Toggles the over-voltage protection level between 5.6V (default) and 18.9V. When the OVP button is depressed, the OVP level will be set to 18.9V
- Data, I/O, HWEN: These buttons control the functionality of the M/F pin. Please refer to the M/F pin description for a detailed description of the M/F pin operation.

	Flash	Torch	Indicator	Disable	
,	174		W	30049	627

- Flash: Starts a Flash event by setting the EN1 and EN0 bits to 1's.
- Torch: Starts a Torch event by setting the EN1 bit to a '1' and EN 0 bit to a '0'.
- Indicator: Starts an Indicator event by setting the EN1 bit to a '0' and EN 0 bit to a '1'.
- Disable: Shuts down the LM3553 by setting the EN1 and EN0 bits to 0's.

Torch	<u></u>	<u> </u>
Flash		
	Flash Duration	

30049626

- Torch Slider: Sets the Torch brightness to any allowable brightness code (0 to 31)
- Flash Slider: Sets the Flash brightness to any allowable brightness code (0 to 127)
- Flash Duration: Sets the Flash duration to one of the 16 built-in time durations (0 to 15)

Note: If the part is enabled to any level of brightness or state and the program is closed (by either hitting the OK or cancel buttons), the LM3553 part will remain in the last controlled state.



≦询LM3553供应商

# **Notes**

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers	19/6/1-	
LDOs	www.national.com/ldo	IIII	
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		17
Temperature Sensors	www.national.com/tempsensors		"二工而现
Wireless (PLL/VCO)	www.national.com/wireless	- 11.70	07SC.

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLÉTENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS. NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

## LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center Email:

new.feedback@nsc.com Tel: 1-800-272-9959

National Semiconductor Europe **Technical Support Center** Email: europe.support@nsc.com German Tel: +49 (0) 180 5010 771 English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com

National Semiconductor Japan **Technical Support Center**