LM3687 Evaluation Board

National Semiconductor
Application Note 1647
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Introduction

This evaluation board is designed to enable independent evaluation of the LM3687 electrical performance. Each board is pre-assembled and tested in the factory.

The evaluation kit is available in two options: LM3687TL-1812EV and LM3687TL-1815EV. For other voltage options, the device can be ordered from LM3687 product folder on National's website.

The board contains the LM3687, an inductor and input and output capacitors connected to GND.

This application note contains information about the evaluation board. For further information on device electrical characteristics and component selection please refer to the datasheet.

General Description

The LM3687 is a high efficiency synchronous switching step-down DC-DC converter with an integrated low dropout Linear Regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides a dual output with fixed output voltages and combined load current up to 750mA in post regulation mode or 1100mA in independent mode of operation.

The LM3687 is capable of operating with input voltage ranges from 2.7V ≤ V_{BATT} ≤ 5.5V and 0.7V ≤ V_{IN_LIN} ≤ 4.5V.

It also features internal protection against short-circuit and over-temperature conditions.

For the Evaluation Board the typical post regulation application is realized: the output voltage of the DC-DC converter is used as supply for the linear regulator ($V_{OUT\_DCDC} = V_{IN\_LIN}$). Thereby a higher efficiency and lower power dissipation of the system can be achieved compared to using the battery voltage V_{BATT} as supply for the linear regulator (V_{IN_LIN}).

For both available evaluation kit options the output voltage of the DC-DC converter is 1.8V and therefore sufficiently high as supply for both linear regulator output voltage options (the power input voltage applied at V_{IN_LIN} should be at least 0.25V above the nominal output voltage of the linear regulator). V_{BATT} should be at least 1.5V above the output voltage of the linear regulator (V_{OUT_LIN}) and 1.0V above the output voltage of the DC-DC converter (V_{OUT_DCDC}) (with a minimum of 2.7V) to operate the device within operating conditions. That means for the 1.8V-1.2V combination, the minimum V_{BATT} = 2.8V and for the 1.8V-1.5V combination it is 3.0V.

Input connections should be kept reasonably short (<20cm) to minimize input inductance and ensure optimum transient performance. It's good practice to twist the wires to the supply for minimum inductance.

ON/OFF control of the LM3687 outputs is provided on the evaluation board by a logic signal applied to the enable pins V_{EN_DCDC} and V_{EN_LIN}. To simplify the enabling of the outputs, two 'three pin jumpers' are provided on the board:

- J5: to enable the DC-DC converter,
- J6: to enable the linear regulator.

The middle pins of the two jumpers are directly connected to the appropriate enable pins of the device. A logic signal with a minimum of 1.0V to enable the output or with a maximum of 0.4V to disable it can be directly connected to this jumper pin in the middle. Alternatively the middle pin can be shorted to the pin next to it to the left (marked ON, shorted to V_{BATT}) or to the right.

A load of up to 750mA maximum may be connected from the V_{OUT_DCDC} pin to GND if no additional load is applied at the output of the linear regulator. For V_{OUT_LIN}, the maximum load is 350mA. As in the typical post regulation application the load of the linear regulator is supplied by the DC-DC converter, the combined maximum load conditions are:

350mA at V_{OUT_LIN} plus 400mA at V_{OUT_DCDC}.

At the top of the board the output voltage option (1812 or 1815) is printed.

The 'connectors' J1, J2, J3 and J4 represents a 'sense path' to V_{OUT_DCDC}, V_{IN_LIN}, V_{BATT} and V_{OUT_LIN}. They can be used for more precise voltage measurements or to connect a differential probe.

In case the two regulators shall be operated independently instead of in the post regulation mode, the connection from V_{OUT_DCDC} to V_{IN_LIN} can be removed by cutting the trace between the two pads at JP1. Then an external source needs to be connected to V_{IN_LIN}. V_{BATT} is still needed for the linear regulator as well, it supplies internal circuitry. **It's important that V_{IN_LIN} does not exceed V_{BATT} at any time**. An input capacitor of 1.0µF at V_{IN_LIN} needs to be added if no other filter bypass capacitor is present in this supply path.

The schematic and board layout are shown below.

Schematic Diagram

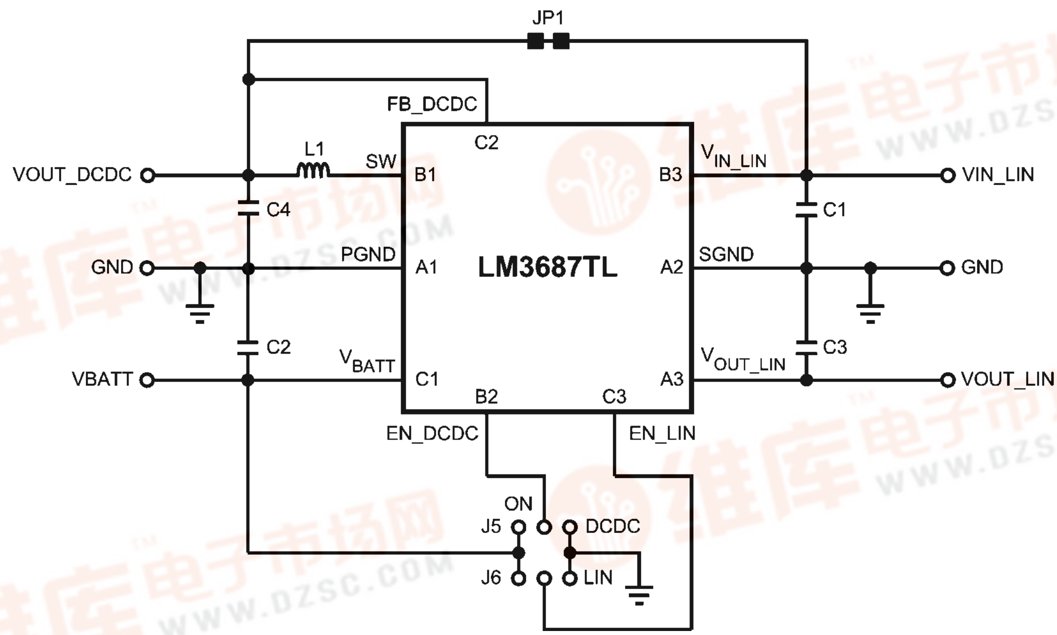

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FIGURE 1: Evaluation Board Schematic

Evaluation Board Top Layer Layout

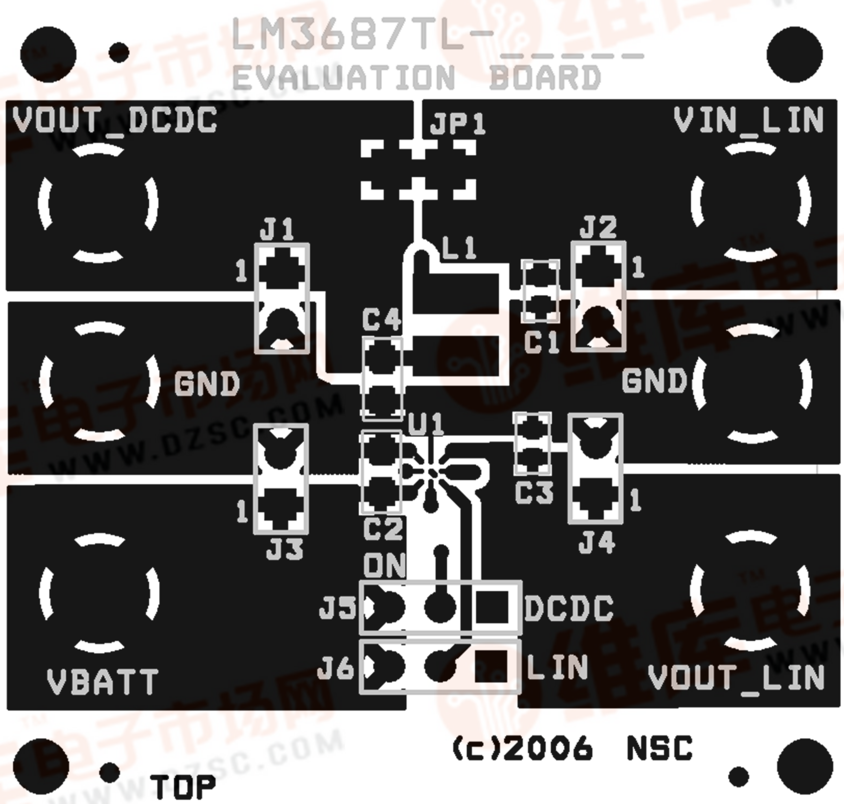

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FIGURE 2: Top Layer Board Layout
Board Size: 40mm x 45mm

Evaluation Board Picture Top Side

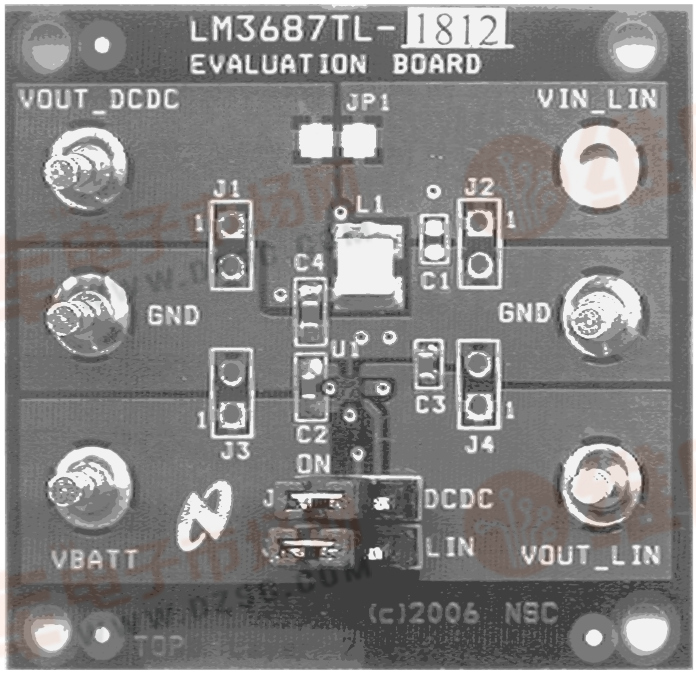

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FIGURE 3: Picture Top Side

Connection Diagram

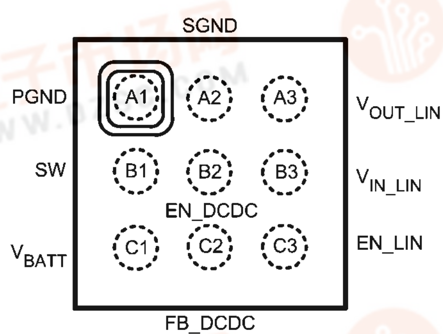

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FIGURE 4: Connection Diagram 9-Bump Thin Micro SMD Package, Large Bump, 0.5mm Pitch

Table 1: Pin Descriptions

Pin #	Name	Description
A1	PGND	Power Ground pin
A2	SGND	Signal Ground pin
A3	V_{OUT_LIN}	Voltage Output of the linear regulator
B1	SW	Switching Node Connection to the internal PFET switch and NFET synchronous rectifier
B2	EN_DCDC	Enable Input for the DC-DC converter. The DC-DC converter is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.0V. Do not leave this pin floating. Please see Table 2: Enable Combinations.
B3	V_{IN_LIN}	Power Supply Input for the linear regulator
C1	V_{BATT}	Power Supply for the DC-DC output stage and internal circuitry. Connected to the input filter capacitor.
C2	FB_DCDC	Feedback Analog Input for the DC-DC converter. Directly connected to the output filter capacitor.
C3	EN_LIN	Enable Input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.0V. Do not leave this pin floating. Please see Table 2: Enable Combinations.

Table 2: Enable Combinations

EN_DCDC	EN_LIN	Comments
0	0	No Outputs
0	1	Linear Regulator enabled only *
1	0	DC-DC converter enabled only
1	1	DC-DC converter and linear regulator active *

* Startup Mode:

V_{IN_LIN} must be higher than $V_{OUT\_LIN(NOM)}$ + 200mV in order to enable the main regulator (I_{MAX} = 350mA).

If $V_{IN\_LIN} < V_{OUT\_LIN(NOM)}$ + 100mV (100mV hysteresis), the startup LDO (I_{MAX} = 50mA) is active, supplied from V_{BATT}.

For example in the typical post regulation application the LDO will remain in startup mode until the DC-DC converter has ramped up its output voltage.

Table 3: Bill of Materials

Item	Description	Amount	Footprint	Mfg., Part Number
C1	C_{IN_LIN}, ceramic capacitor, 1µF, X5R at V_{IN_LIN}, optional, not needed in post regulation application due to C4	0	0603 / 0402	
C2	C_{BATT}, ceramic capacitor, 4.7µF, X5R at V_{BATT}	1	0805 / 0603	TDK, C1608X5R1A475K
C3	C_{OUT_LIN}, ceramic capacitor, 2.2µF, X5R at V_{OUT_LIN}	1	0603 / 0402	TDK, C1608X5R1A225K
C4	C_{OUT_DCDC}, ceramic capacitor, 10µF, X5R at V_{OUT_DCDC}	1	0805 / 0603	TDK, C1608X5R0J106K
L1	Inductor, 2.2µH, 1.6A I_{SAT}	1		Coilcraft, DO3314-222MLB
U1	LM3687TL	1	9-bump micro SMD TLA09BBA	National Semiconductor, LM3687TL-1815 or LM3687TL-1812
V_{BATT}, V_{OUT_DCDC}, V_{OUT_LIN}, 2x GND	Terminal	5		Cambion, 160-1026-02-05
J5, J6	3 pin jumper for enable function	2		

Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

The allowable power dissipation for the device in a given package can be calculated using the following equation:

$P_{D\_SYS} = (T_{J(MAX)} - T_A) / \theta_{JA}$

For the LM3687 there are two different main sources contributing to the systems power dissipation (P_{D_SYS}):

the DC-DC converter (P_{D_DCDC}) and

the linear regulator (P_{D_LIN}).

Neglecting switching losses and quiescent currents these two main contributors can be estimated by the following equations:

- $P_{D\_LIN} = (V_{IN\_LIN} - V_{OUT\_LIN}) * I_{OUT\_LIN}$
- $P_{D\_DCDC} = I_{OUT\_DCDC}^2 * [(R_{DSON(P)} * D) + (R_{DSON(N)} * (1-D))]$ with duty cycle $D = V_{OUT\_DCDC} / V_{BATT}$.

As an example, assuming the typical post regulation application, the conversion from $V_{BATT} = 3.6V$ to $V_{OUT\_DCDC} = 1.8V$ and further to $V_{OUT\_LIN} = 1.5V$, at maximum load currents, results in following power dissipations:

$P_{D\_DCDC} = (0.75A)^2 * (0.38\Omega * 1.8V / 3.6V + 0.25\Omega * (1 - 1.8V / 3.6V)) = 177mW$ and

$P_{D\_LIN} = (1.8V - 1.5V) * 0.35A = 105mW$.

$P_{D\_SYS} = 282mW$.

With a $\theta_{JA} = 70°C/W$ for the micro SMD 9 package this P_{D_SYS} will cause a rise of the junction temperature T_J of:

$\Delta T_J = P_{D\_SYS} * \theta_{JA} = 20K$.

For the same conditions but the linear regulator biased from V_{BATT}, this results in a P_{D_LIN} of 735mW, $P_{D\_DCDC} = 50mW$ (because $I_{OUT\_DCDC} = 400mA$) and therefore an increase of $T_J = 55K$. As lower total power dissipation translates to higher efficiency this example highlights the advantage of the post regulation setup.

Notes

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