LM3881 Power Sequencer Evaluation Board

National Semiconductor
Application Note 1785
Timothy Hegarty
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Introduction

The LM3881 evaluation board has been designed to permit the designer to connect it directly to the Enable or Remote ON/OFF pins of power supply devices of an existing system to facilitate system sequencing. The block diagram of a typical system application is given in *Figure 1*.

Upon enabling the device, the three open drain output flags will rise in sequential order, 1-2-3. Once the part is disabled, the shutdown sequence will occur in reverse order 3-2-1. Therefore the last power supply that started up will be the first to shutdown.

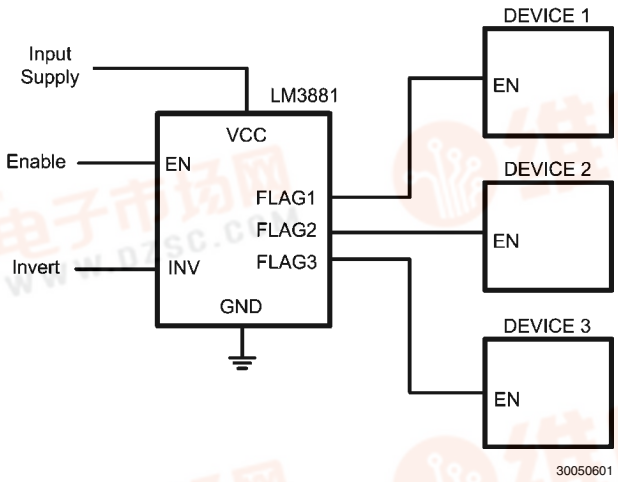

FIGURE 1. Typical System Application Using LM3881 Sequencer

Timing Sequence

Figure 2 and *Figure 3* present the power up and power down timing sequence of the output flags with the INV at logic level low and high respectively. The waveform labeled TADJ refers to the voltage on the timer adjust pin of the LM3881.

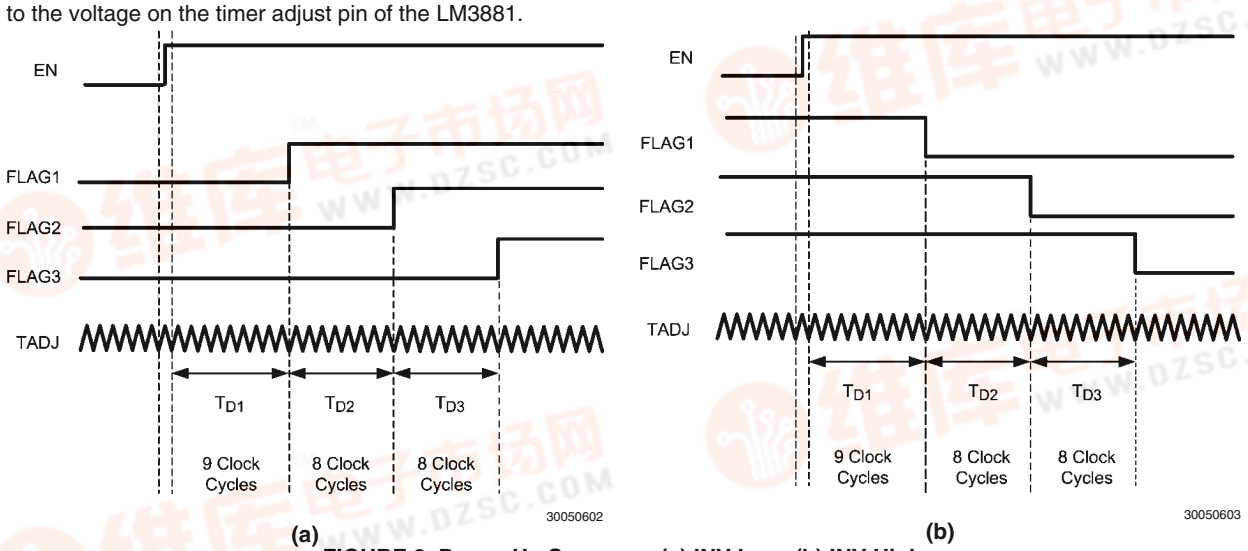

FIGURE 2. Power Up Sequence (a) INV Low, (b) INV High

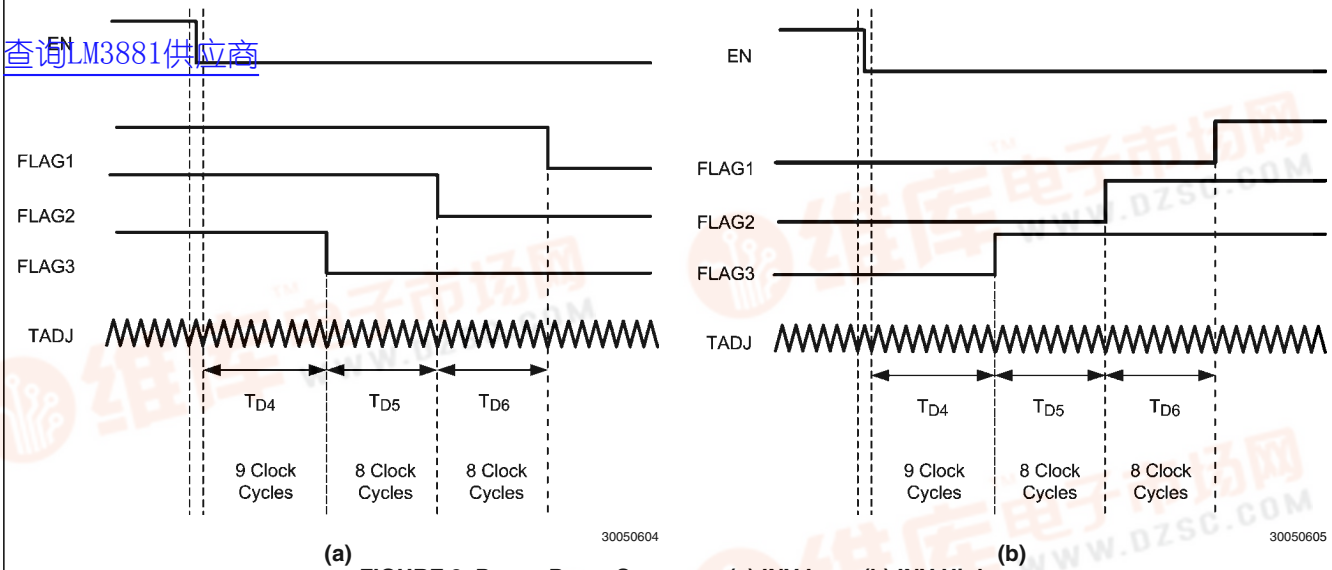

FIGURE 3. Power Down Sequence (a) INV Low, (b) INV High

LM3881 Circuit Schematic

The evaluation board schematic is given in *Figure 4*. The board contains the LM3881MFX device which has a timing capacitor, C_{ADJ}, of 10 nF so that each time delay between flags will be approximately 10 ms. The pull-up resistors of the flag outputs (R1, R2, R3) are each 100 kΩ.

The LM3881 has an enable pin that is pulled up by an internal 7 µA current source. Thus, the associated PCB terminal, labeled EN, can be left open circuit if desired. In this case, the flags will release when the LM3881 V_{CC} supply exceeds its UVLO level. Finally, the LM3881 has an invert pin that sets the polarity of the flags. The associated PCB terminal, labeled INV, needs to be connected to VCC or GND.

The evaluation board bill of materials, LM3881 pin-out and pin description are given in *Table 1*, *Figure 5* and *Table 2* respectively.

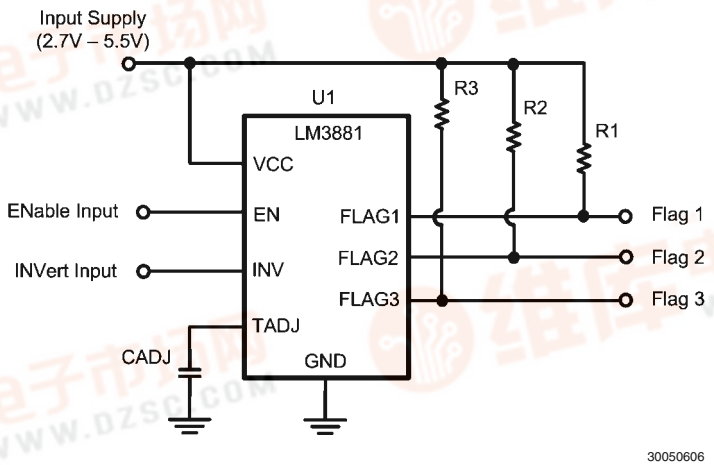

FIGURE 4. LM3881 Schematic

LM3881 Evaluation Board Bill of Materials

TABLE 1.

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	LM3881 Sequencer	MSOP-8	National Semiconductor	LM3881MFX
R1	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
R2	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
R3	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
CADJ	10 nF ±10% X7R 16V	0603	Murata	GRM188R71C103KA01

LM3881 Pin-Out

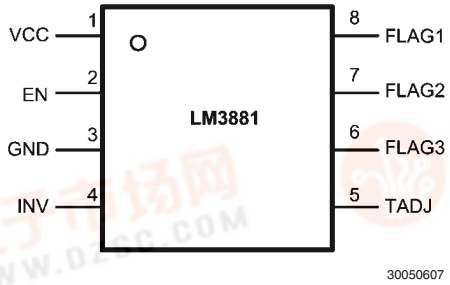

FIGURE 5. LM3881 Pin-Out

LM3881 Pin Descriptions

TABLE 2.

Pin #	Name	Function
1	VCC	Input Supply
2	EN	Precision Enable
3	GND	Ground
4	INV	Output Logic Invert
5	TADJ	Timer Adjust
6	FLAG3	Open Drain Output #3
7	FLAG2	Open Drain Output #2
8	FLAG1	Open Drain Output #1

PC Board Layout

The evaluation board is based on a small 1.09” x 0.76” FR4 PCB with two layers of copper. The actual layout can be seen in *Figure 6* and *Figure 7* below. When looking at the top layer, pin 1 of the LM3881 is on the upper left. An optional component, assigned reference designator R4, is placed on the bottom side of the PCB to facilitate connection of INV to GND.

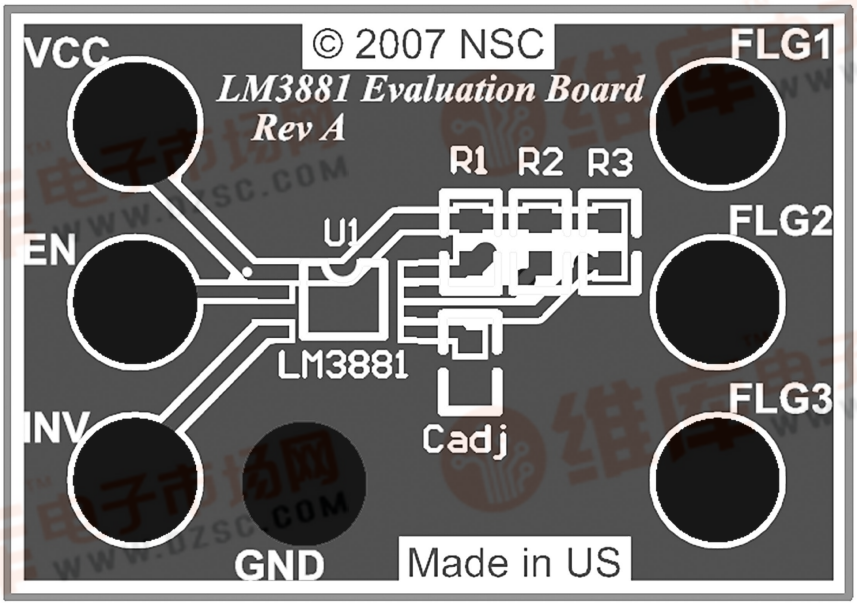

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FIGURE 6. Top Side PCB Layout

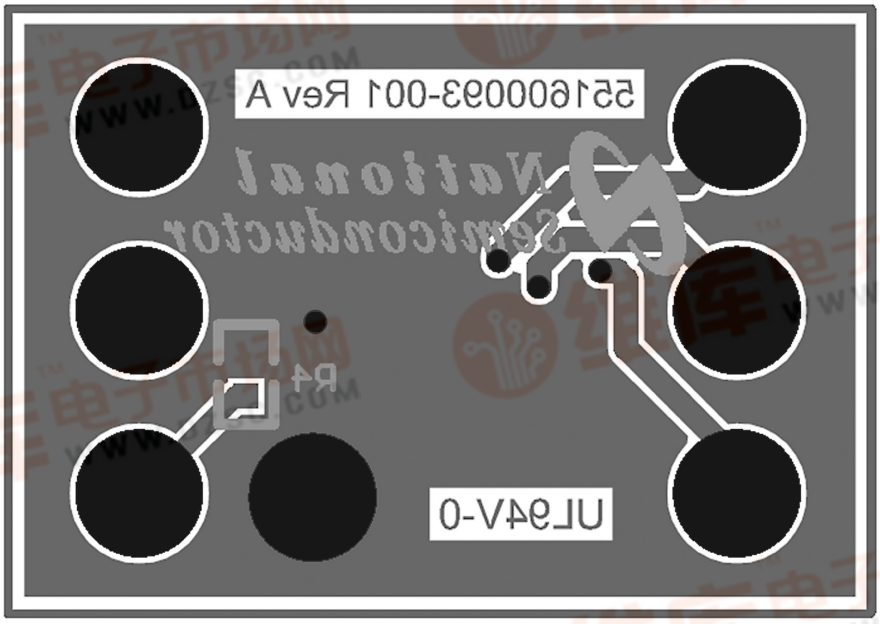

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FIGURE 7. Bottom Side PCB Layout

Notes

Notes

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