LP5551 Evaluation Board

National Semiconductor
Application Note 1467
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LP5551 Overview

The LP5551 is a PWI 1.0 compliant Energy Management Unit for reducing power consumption of stand-alone mobile phone processors such as base-band or applications processors.

The LP5551 contains two advanced, digitally controlled switching regulators for supplying variable voltage to processor core and memory. Two regulators provide P- and N- well biasing for threshold scaling applications. The device also integrates 4 programmable LDO-regulators for powering I/O, PLLs and maintaining memory retention in sleep-mode.

The device is controlled via the PWI 1.0 open-standard interface. The LP5551 operates cooperatively with PowerWise™ technology compatible processors to optimize supply voltages adaptively over process and temperature variations or dynamically using frequency/voltage pre-characterized look-up tables and provides P- and N-well biasing for threshold scaling.

Evaluation Board Overview

The LP5551 Evaluation Board can be operated standalone or from a motherboard such as the PowerWise Evaluation Kit (PEK) or USB interface board.

The evaluation board ships with the USB interface board and a graphical user interface (GUI) to easily control the features of the LP5551 from a PC. See AN-1535 for information on the GUI.

The LP5551 is configured to operate with the following conditions:

Parameter	Default Voltage	Programming Range	I_{OUT}
VBATT	3.6 V		
VAVS	1.2 V	0.6 - 1.2 V	300 mA
VDVS	1.2 V	0.6 - 1.2 V	300 mA
VO1	1.2 V	0.7 - 2.2 V	100 mA
VO2	3.3 V	1.5 - 3.3 V	250 mA
VO3	Tracks V_{AVS} (Active State)	V_{AVS} + 0.04 V	50 mA
	1.2 V (Sleep State)	0.6 - 1.35 V	5 mA
VO4	3.3 V	1.5 - 3.3 V	250 mA
VPWELL	0 V	-1 ~ 0.3 V	20 uA
VNWELL	V_{AVS} + 0 V	VAVS + (-0.3 ~ 1) V	7 mA

Note that all the regulators can be programmed to different output voltages once the part starts up.

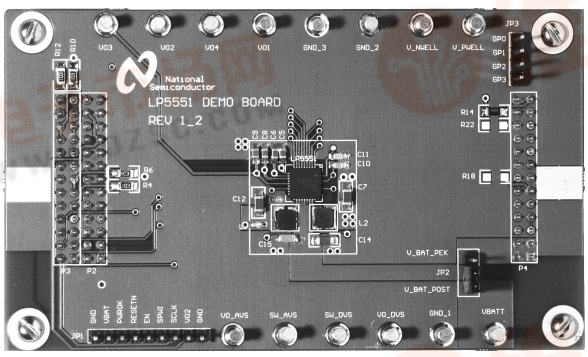

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FIGURE 1. LP5551 Evaluation Board

The LP5551 can be powered externally (bench supply), or from the PEK or USB interface board (depending on motherboard being used). Jumper J2 must be set the appropriate power source.

JUMPER	PURPOSE	NOTE
JP2	Input voltage selection	V_BAT_POST: LP5551 powered from external supply
		V_BAT_PEK: LP5551 powered from PEK or from USB interface board

Connecting the LP5551 to the USB2PWI interface board

The LP5551 evaluation board can be connected to the USB2PWI interface board for convenient control of the PWI and all the LP5551 functions via a GUI. *Figure 2* shows the USB2PWI interface board. See AN-1535 for instructions on how to use the GUI.

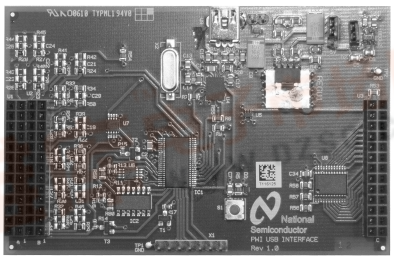

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FIGURE 2. USB Interface Board

Connecting the LP5551 Evaluation Board to an External Controller

Jumper J1 allows for external control of the PWI, used to communicate with the LP5551. It is a SIP-9 footprint. The pin list of J1 is shown in Table 1. VBAT and VO2 are provided on J1 as sense outputs to determine the drive levels for the inputs RESETN, EN, SPWI, and SCLK. The external controller should drive EN and RESETN to VBAT and ground, while SPWI and SCLK should be driven between VO2 and ground.

Pin	Function	Type	Description
1	GND	GND	Ground
2	VBAT	Output	VBAT Sense
3	PWROK	Output	PWROK Sense
4	RESETN	Input	VBAT: On GND: RESET LP5551
5	EN	Input	VBAT: On GND: Disable LP5551
6	SPWI	Input	PWI Data
7	SCLK	Input/Output	PWI Clock
8	VO2	Output	VO2 Sense
9	GND	GND	Ground

Connecting the LP5551 Evaluation Board to the PEK

The PEK is designed to quickly and easily control the LP5551 for PowerWise Interface (PWI) compliance testing. *Figure 3* shows the PEK. See the PEK User's Guide for more information.

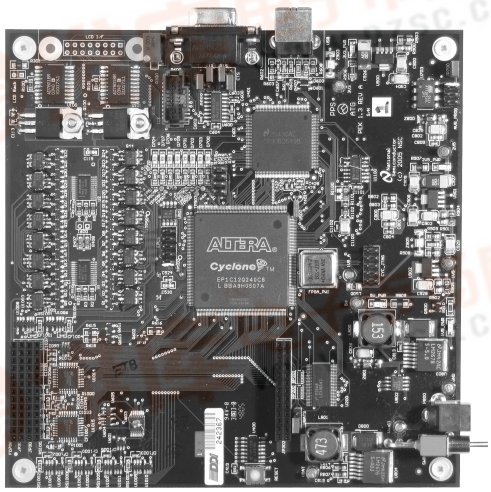

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FIGURE 3. PowerWise Evaluation Kit (PEK)

PCB Layout Considerations

The evaluation board layers from top to bottom are:

1. Top, component side
2. Ground plane
3. Power plane
4. Bottom

See *Figure 5*, *Figure 6*, and *Figure 7* for layout diagrams.

For good performance of the circuit, it is essential to place the input and output capacitors very close to the circuit and use wide routing for the traces allowing high currents. Decoupling capacitors should be close to circuit's VIN pins.

Sensitive components should be placed far from those components with high pulsating current.

It's a good practice to minimize high current and switching current paths.

LOW DROP OUT (LDO) REGULATORS

Place the filter capacitors very close to the input and output pins. Use large trace width for high current carrying traces and the returns to ground.

BUCK REGULATORS

Place the supply bypass, filter capacitor, and inductor close together and keep the traces short. The traces between these

components carry relatively high switching current and act as antennas. Following these rules reduces radiated noise.

Arrange the components so that the switching current loops curl in the same direction.

Connect the buck ground and the ground of the capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this back to the general board system ground plane at a single point. Place the pseudo-ground plane below these components and then have it tied to system ground of the output capacitor outside of the current loops. This prevents the switched current from injecting noise into the system ground. These components along with the inductor and output should be placed on the same side of the circuit board, and their connections should be made on the same layer.

Route noise sensitive traces such as the voltage feedback path away from the inductor. This is done by routing it on the bottom layer or by adding a grounded copper area between switching node and feedback path. To reduce noisy traces between the power components, keep any digital lines away from this section. Keep the Feedback node as small as possible so that the ground pin and ground traces will shield it from the SW or buck output.

Use wide traces between the power components and for power connections to the DC-DC converter circuit to reduce voltage errors caused by resistive losses.

For the sense lines, make sure to use a Kelvin contact connection.

Bill of Materials

P/N	Part Type	Designator	Footprint	Description	MNF
VJ0805X7R475MXAA	0.47uF	C15	805	Capacitor	Vishay
D251001501F	1.5K	R14	1206	Resistor	Vishay
D251001501F	1.5K	R13	1206	Resistor	Vishay
VJ0805X7R102MXAA	1nF	C11	805	Capacitor	Vishay
VJ0805X7R102MXAA	1nF	C10	805	Capacitor	Vishay
EMK212BJ475MG	4.7uF	C5	805	Capacitor	Taiyo Yuden
EMK212BJ475MG	4.7uF	C6	805	Capacitor	Taiyo Yuden
CRCW12061002F	10k	R6	1206	Resistor	Vishay
CRCW12061002F	10k	R4	1206	Resistor	Vishay
CRCW12061002F	10k	R2	1206	Resistor	Vishay
CRCW12061002F	10k	R5	1206	Resistor	Vishay
CRCW12061002F	10k	R12	1206	Resistor	Vishay
CRCW12061002F	10k	R7	1206	Resistor	Vishay
CRCW12061002F	10k	R11	1206	Resistor	Vishay
CRCW12061002F	10k	R10	1206	Resistor	Vishay
CRCW12061002F	10k	R9	1206	Resistor	Vishay
LMK316BJ226ML	22 uF	C14	1206	Capacitor	Taiyo Yuden
JMK316BJ226KL	22 uF	C7	805	Capacitor	Taiyo Yuden
JMK316BJ226KL	22 uF	C12	805	Capacitor	Taiyo Yuden
LMK212BJ105KG	1 uF	C9	805	Capacitor	Taiyo Yuden
LMK212BJ225KG	2.2 uF	C8	805	Capacitor	Taiyo Yuden
	LP5551	U1	SQA36A	PowerWise EMU	National Semiconductor
	NL	R22	1206	Resistor	
	NL	R18	1206	Resistor	
	NL	R20	1206	Resistor	
	NL	R21	1206	Resistor	
NR4012T4R7M	4.7 uH	L2	NR4012	Inductor	Taiyo Yuden
NR4012T4R7M	4.7 uH	L1	NR4012	Inductor	Taiyo Yuden

Schematic

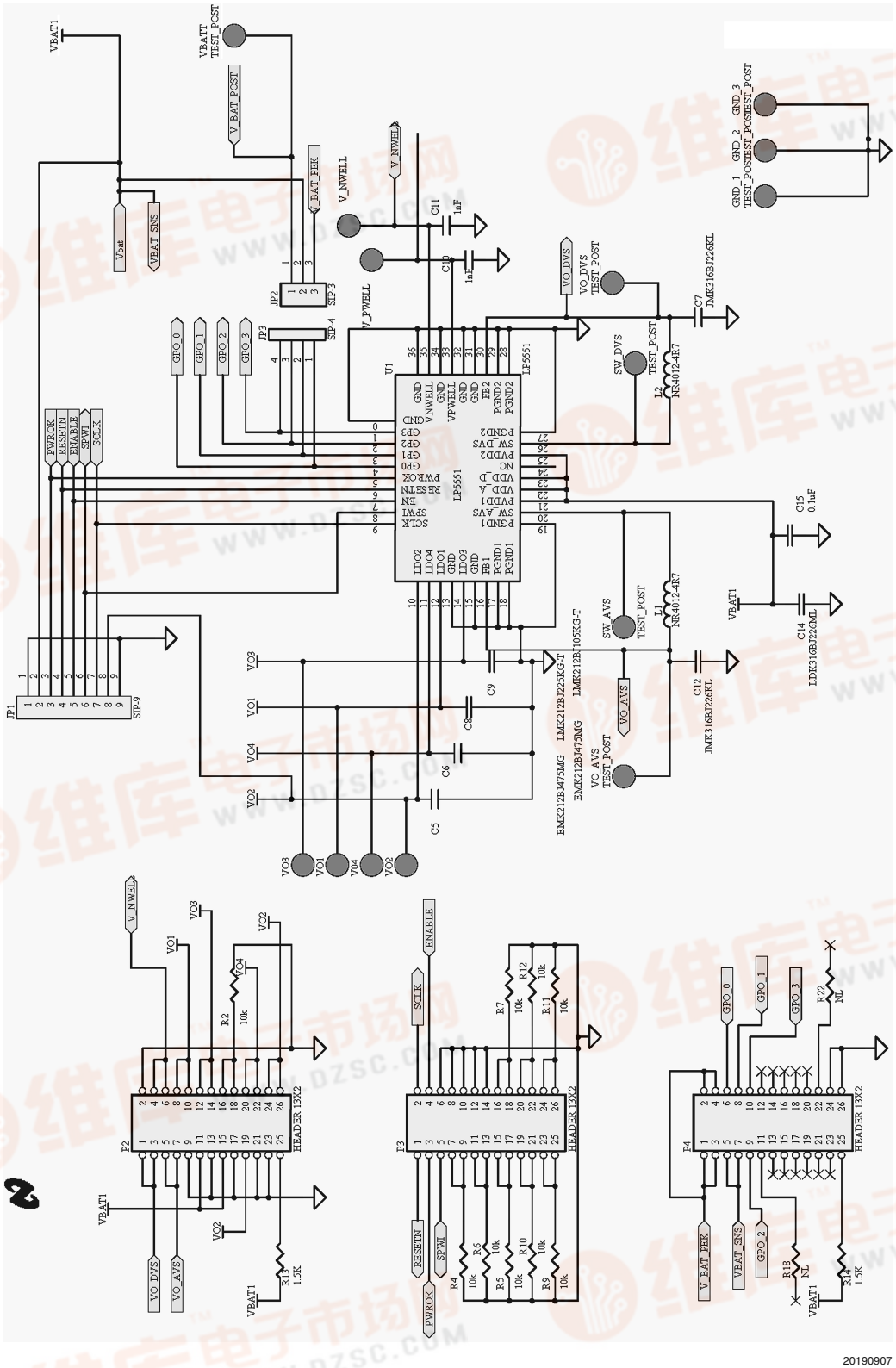

FIGURE 4. LP5551 Demo Board Schematic

Layout Diagrams

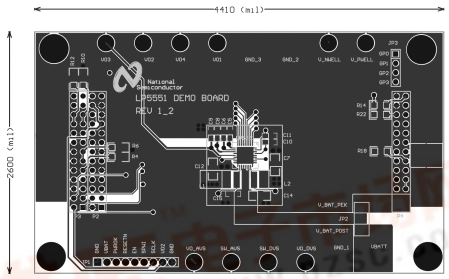

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FIGURE 5. Top Layer

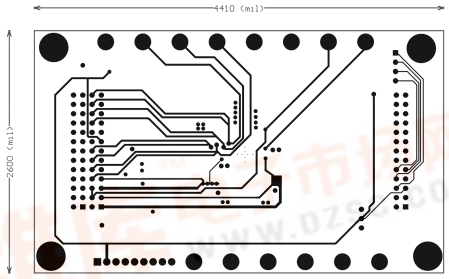

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FIGURE 6. Mid Layer

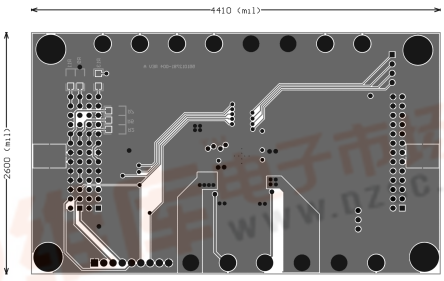

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FIGURE 7. Bottom Layer

Notes

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