MICROCHIP

MCP6286

Low Noise, Low Power Op Amp

Features

- Low Noise: 5.4 nV/√Hz (typical)
- Low Quiescent Current: 520 µA (typical)
- Rail-to-Rail Output
- Wide Supply Voltage Range: 2.2V to 5.5V
- Gain Bandwidth Product: 3.5 MHz (typical)
- Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C
- No Phase Reversal
- Small Package

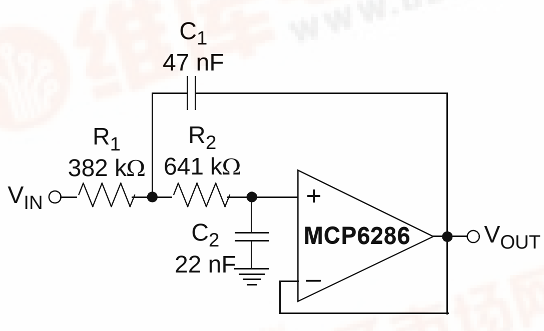
Applications

- Noise Cancellation Headphones
- Cellular Phones
- Analog Filters
- Sensor Conditioning
- Portable Instrumentation
- Medical Instrumentation
- Battery Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



f_P = 10 Hz G = +1 V/V

Second-Order, Low-Pass Butterworth Filter

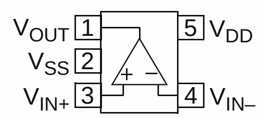
Description

The Microchip Technology Inc. MCP6286 operational amplifier (op amp) has low noise (5.4 nV/√Hz, typical), low power (520 µA, typical) and rail-to-rail output operation. It is unity gain stable and has a gain bandwidth product of 3.5 MHz (typical). This device operates with a single supply voltage as low as 2.2V, while drawing low quiescent current. These features make the product well suited for single-supply, low noise, battery-powered applications.

The MCP6286 op amp is offered in a space saving SOT-23-5 package. It is designed with Microchip's advanced CMOS process and available in the extended temperature range, with a power supply range of 2.2V to 5.5V.

Package Types

MCP6286
SOT-23-5



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins ....±2 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† .... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage .... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current ....continuous
Current at Output and Supply Pins ....±30 mA
Storage Temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J)......................... +150°C
ESD protection on all pins (HBM; MM) .... ≥ 4 kV; 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **4.1.2 “Input Voltage And Current Limits”**

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.2V to +5.5V, V_{SS}= GND, T_A= +25°C, $V_{CM} = V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-1.5	—	+1.5	mV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±1	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection Ratio	PSRR	80	100	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
		—	50	150	pA	T_A = +85°C
		—	1500	3000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||20	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||20	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}-1.2	V	**Note 1**
Common Mode Rejection Ratio	CMRR	76	95	—	dB	V_{CM} = -0.3V to 1.0V, V_{DD} = 2.2V
		80	100	—	dB	V_{CM} = -0.3V to 4.3V, V_{DD} = 5.5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	100	120	—	dB	0.2V < V_{OUT} <(V_{DD}-0.2V)
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS}+15	—	V_{DD}–15	mV	0.5V Input overdrive
		V_{SS}+75	—	V_{DD}–75	mV	0.5V Input overdrive R_L = 2 kΩ
Output Short-Circuit Current	I_{SC}	—	±20	—	mA	

Note 1: Figure 2-12 shows how V_{CMR} changes across temperature.

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.2V to +5.5V, V_{SS}= GND, T_A= +25°C, V_{CM} = V_{DD}/3, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.2	—	5.5	V	
Quiescent Current per Amplifier	I_Q	300	520	700	µA	I_O = 0, V_{DD} = 2.2V
		320	540	720	µA	I_O = 0, V_{DD} = 5.5V

Note 1: Figure 2-12 shows how V_{CMR} changes across temperature.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2 to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	3.5	—	MHz	
Phase Margin	PM	—	60	—	°	G = +1 V/V
Slew Rate	SR	—	2	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	1.0	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	22	—	nV/√Hz	f = 10 Hz
		—	5.4	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.2V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.2 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. It independently sets V_{CM} and V_{OUT}; see Equation 1-1. The circuit's common mode voltage is $(V_P + V_M)/2$, not V_{CM}. V_{OST} includes V_{OS} plus the effects of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$G_N = 1 + G_{DM}$$
$$V_{CM} = V_P(1 - 1/G_N) + V_{REF}(1/G_N)$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = V_{REF} + (V_P - V_M)G_{DM} + V_{OST}G_N$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
G_N	=	Noise Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

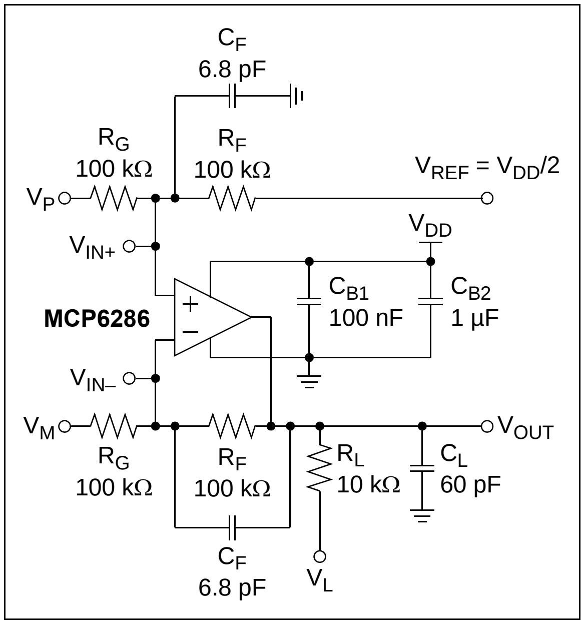


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

> **Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

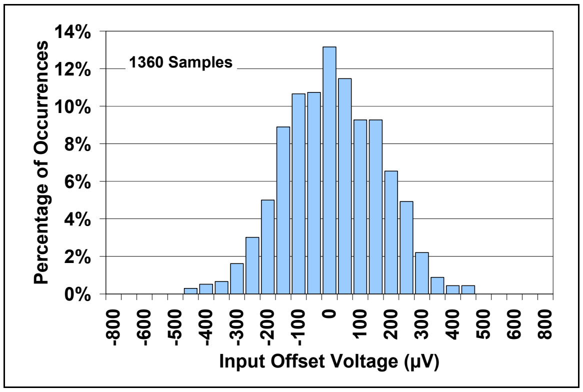


FIGURE 2-1: *Input Offset Voltage.*

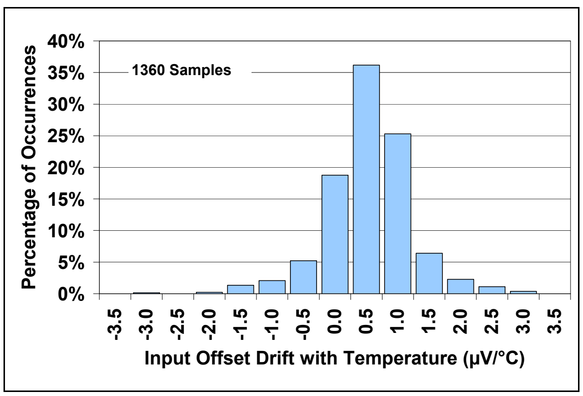


FIGURE 2-2: *Input Offset Voltage Drift.*

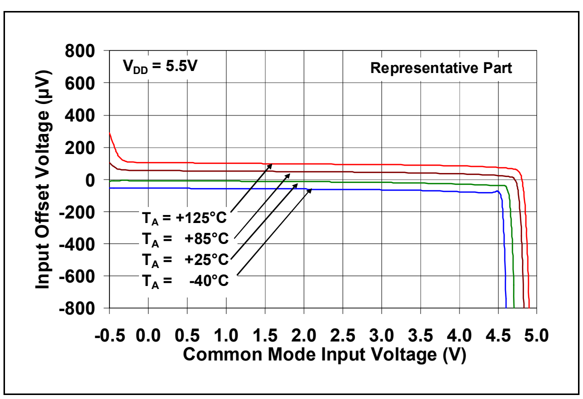


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

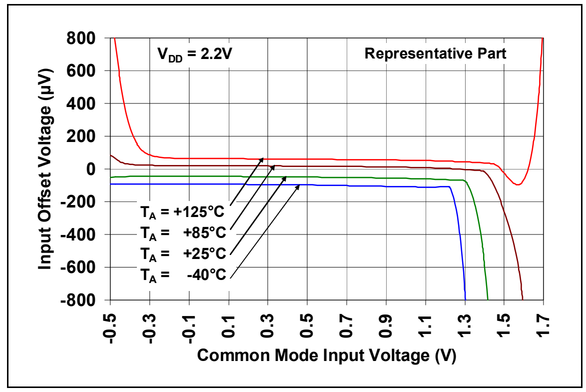


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 2.2V.*

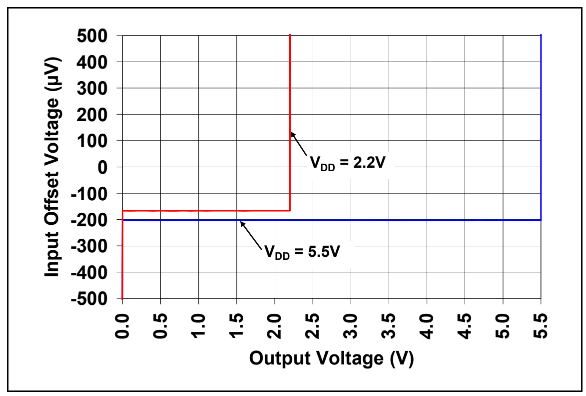


FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

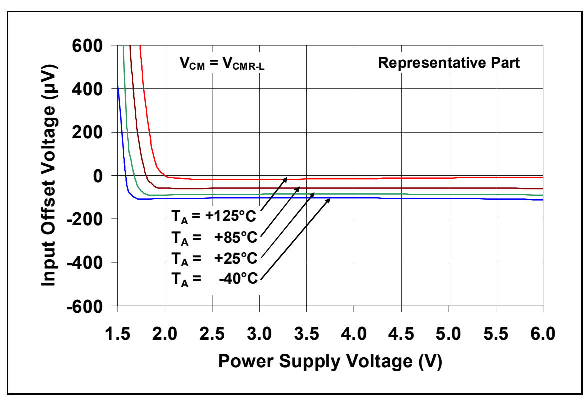


FIGURE 2-6: *Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CMR\_L}$.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

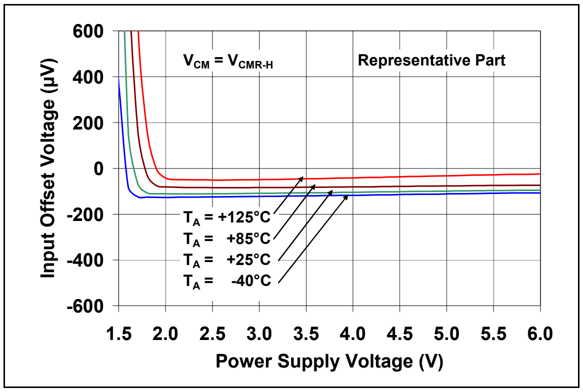


FIGURE 2-7: *Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CMR\_H}$.*

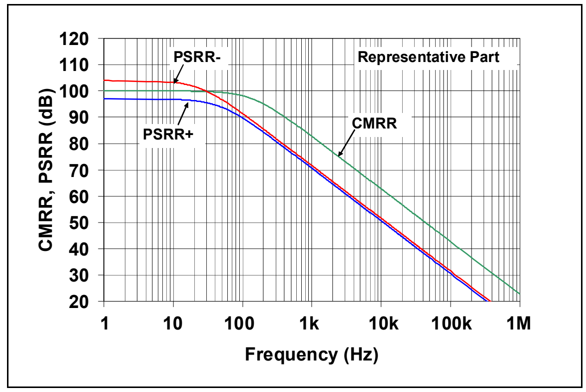


FIGURE 2-10: *CMRR, PSRR vs. Frequency.*

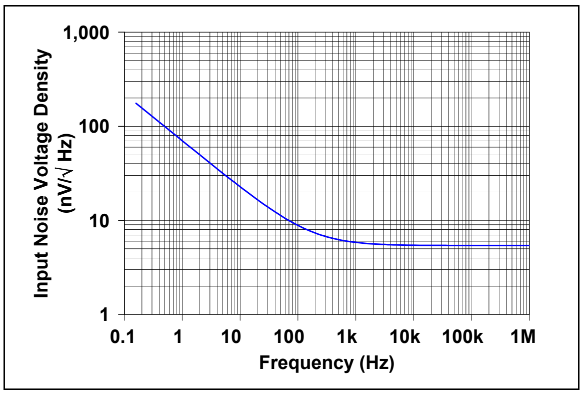


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

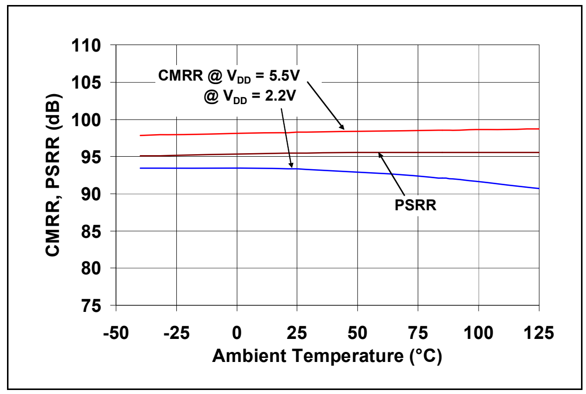


FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

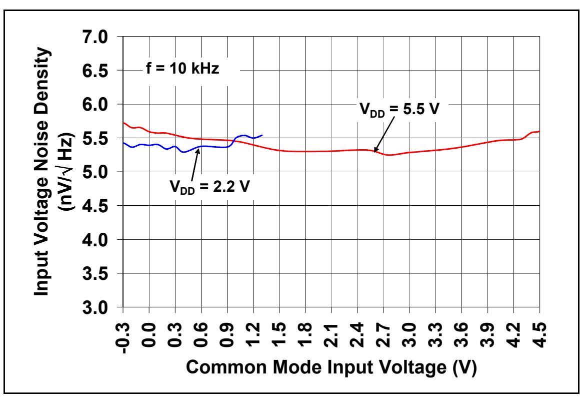


FIGURE 2-9: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

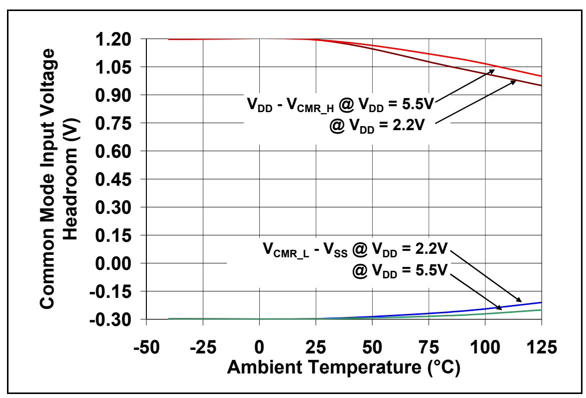


FIGURE 2-12: *Common Mode Input Voltage Headroom vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

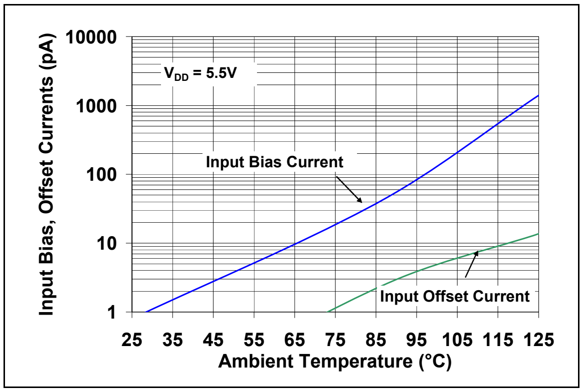


FIGURE 2-13: *Input Bias, Offset Currents vs. Ambient Temperature.*

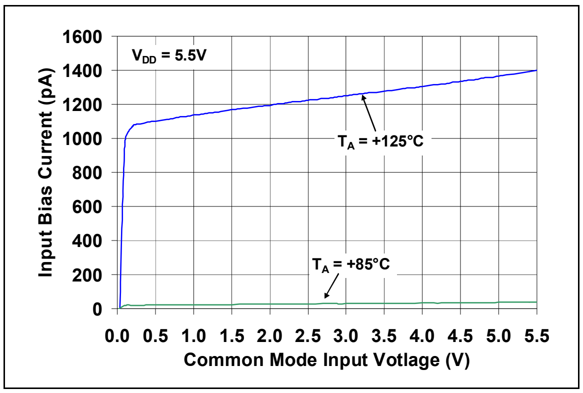


FIGURE 2-14: *Input Bias Current vs. Common Mode Input Voltage.*

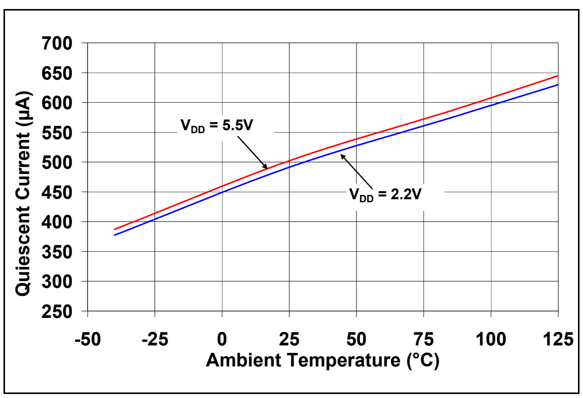


FIGURE 2-15: *Quiescent Current vs Ambient Temperature.*

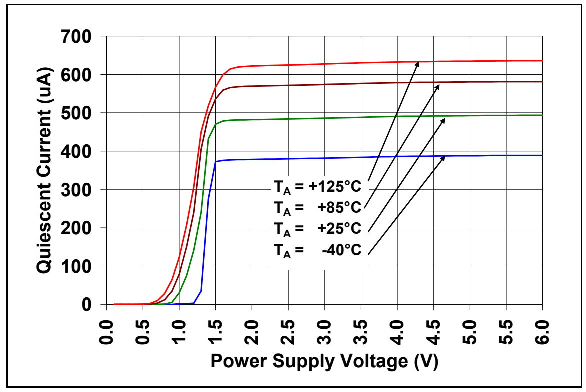


FIGURE 2-16: *Quiescent Current vs. Power Supply Voltage.*

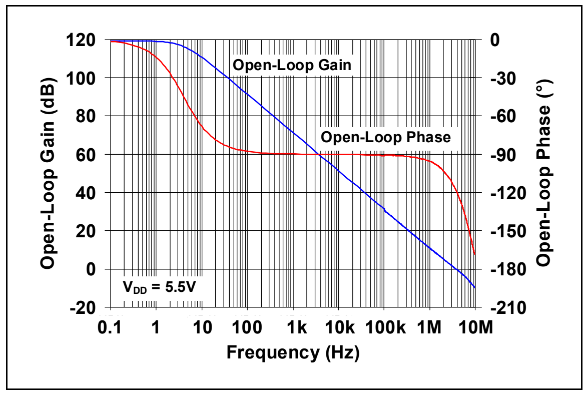


FIGURE 2-17: *Open-Loop Gain, Phase vs. Frequency.*

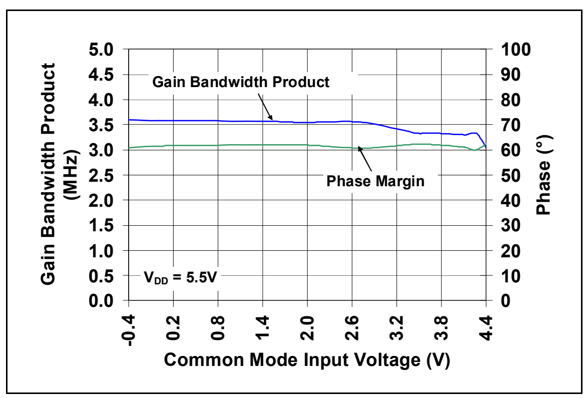


FIGURE 2-18: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF

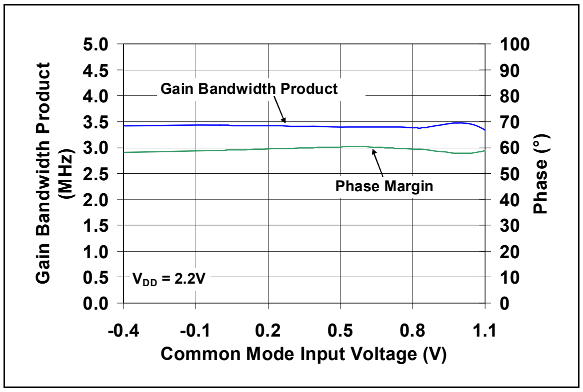


FIGURE 2-19: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage with V_{DD} = 2.2V.*

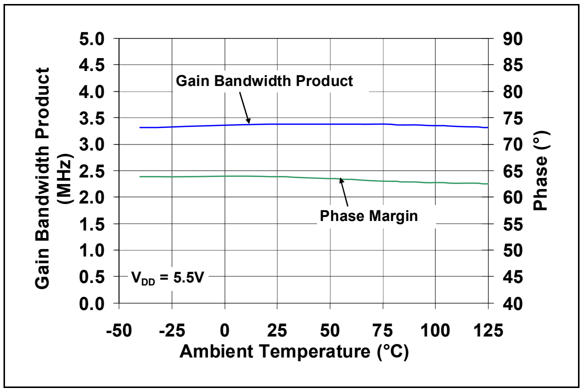


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 5.5V.*

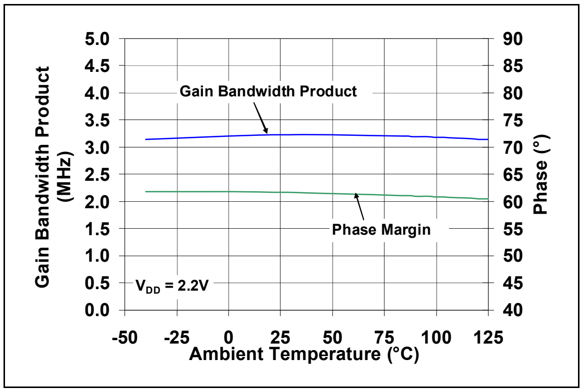


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 2.2V.*

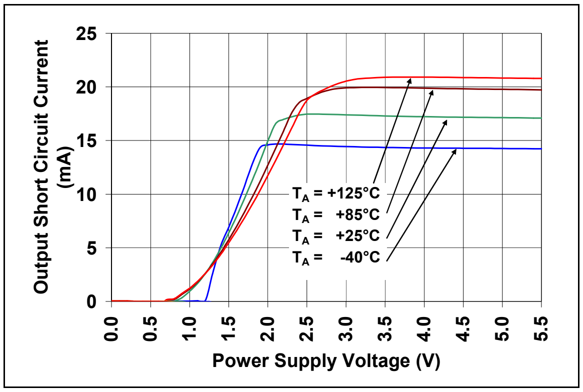


FIGURE 2-22: *Ouput Short Circuit Current vs. Power Supply Voltage.*

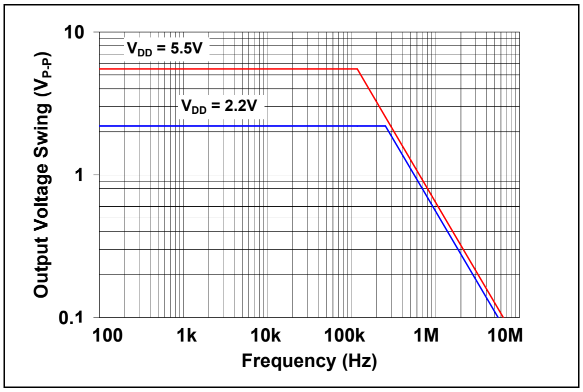


FIGURE 2-23: *Output Voltage Swing vs. Frequency.*

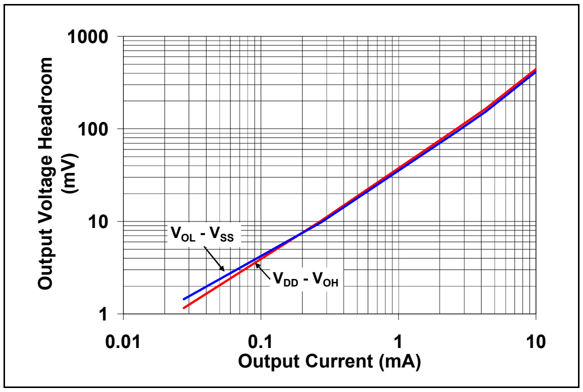


FIGURE 2-24: *Output Voltage Headroom vs. Output Current.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.2V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

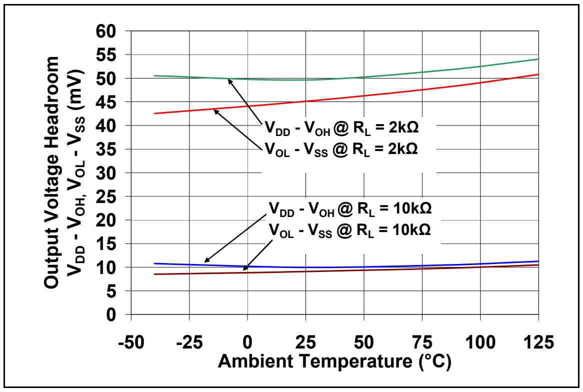


FIGURE 2-25: *Output Voltage Headroom vs. Ambient Temperature.*

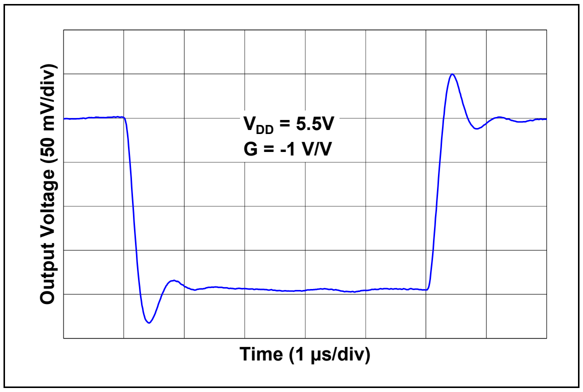


FIGURE 2-28: *Small Signal Inverting Pulse Response.*

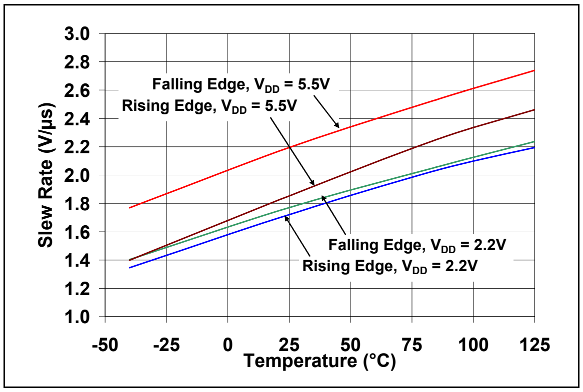


FIGURE 2-26: *Slew Rate vs. Ambient Temperature.*

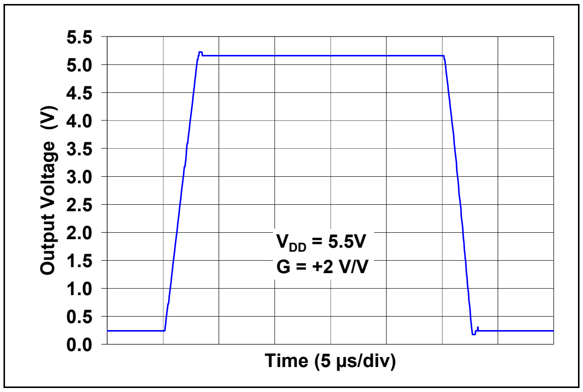


FIGURE 2-29: *Large Signal Non-Inverting Pulse Response.*

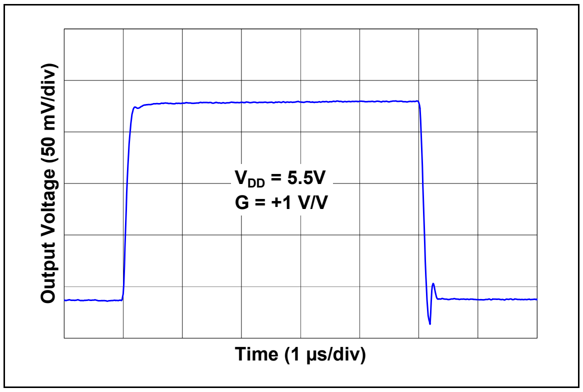


FIGURE 2-27: *Small Signal Non-Inverting Pulse Response.*

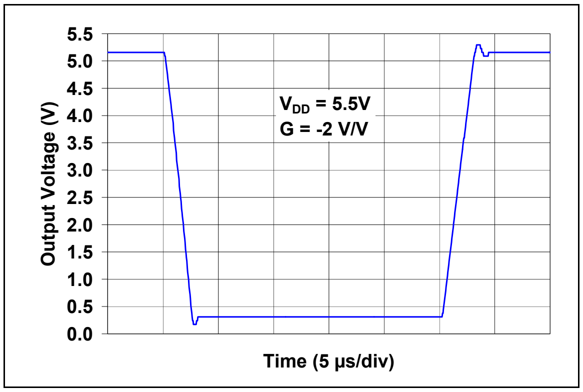


FIGURE 2-30: *Large Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

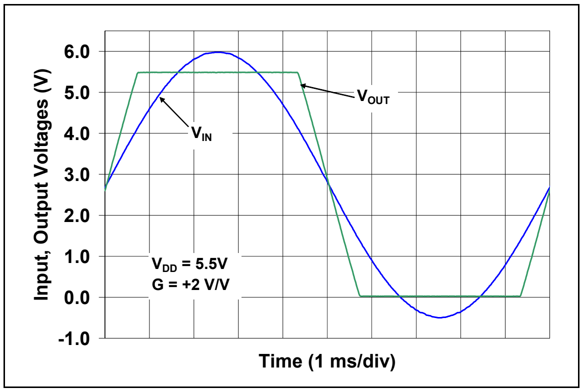


FIGURE 2-31: *The MCP6286 Shows No Phase Reversal.*

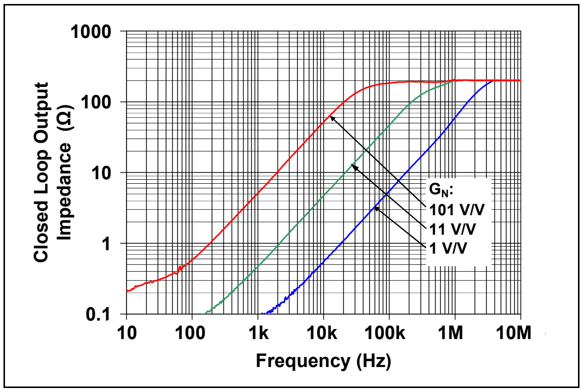


FIGURE 2-32: *Closed Loop Output Impedance vs. Frequency.*

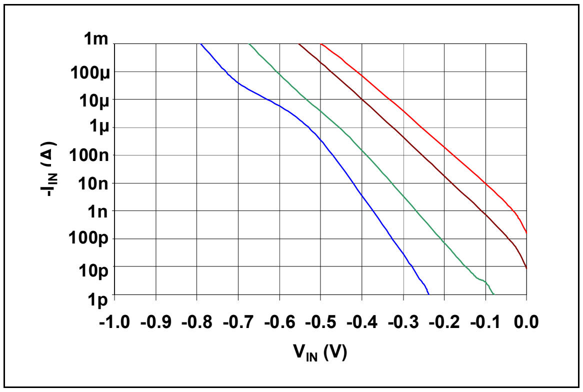


FIGURE 2-33: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6286 SOT-23-5	Symbol	Description
1	V_{OUT}	Analog Output
2	V_{SS}	Negative Power Supply
3	$V_{IN}+$	Non-inverting Input
4	$V_{IN}-$	Inverting Input
5	V_{DD}	Positive Power Supply

3.1 Analog Output

The output pin is low-impedance voltage source.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.2V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

NOTES:

4.0 APPLICATION INFORMATION

The MCP6286 op amp is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, low-noise applications.

4.1 Input

4.1.1 PHASE REVERSAL

The MCP6286 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-31 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltage that goes too far above V_{DD}; their breakdown voltage is high enough to allow normal operation and low enough to bypass ESD events within the specified limits.

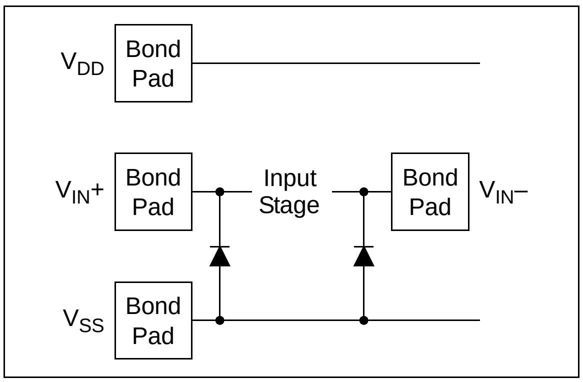
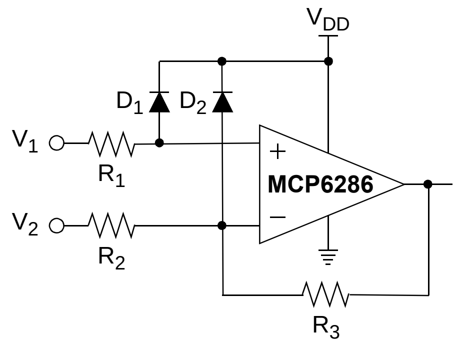


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the voltages and currents at the V_{IN+} and V_{IN-} pins (see **Absolute Maximum Ratings** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN+} and V_{IN-}) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN+} and V_{IN-}) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC currents into the input pins (V_{IN+} and V_{IN-}) should be very small. A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}). (See Figure 2-33).

4.1.3 NORMAL OPERATION

The input stage of the MCP6286 op amp uses a PMOS input stage. It operates at low common mode input voltage (V_{CM}), including ground. With this topology, the device operates with a V_{CM} up to V_{DD} - 1.2V and 0.3V below V_{SS}. (See Figure 2-12).The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and V_{DD} - 1.2V to ensure proper operation.

For a unity gain buffer, since V_{OUT} is the same voltage as the inverting input, V_{OUT} must be maintained below V_{DD} –1.2V for correct operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6286 op amp is V_{SS} + 15 mV (minimum) and V_{DD} – 15 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-24 and Figure 2-25 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

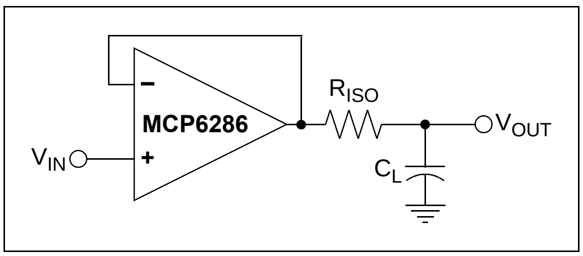


FIGURE 4-3: Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

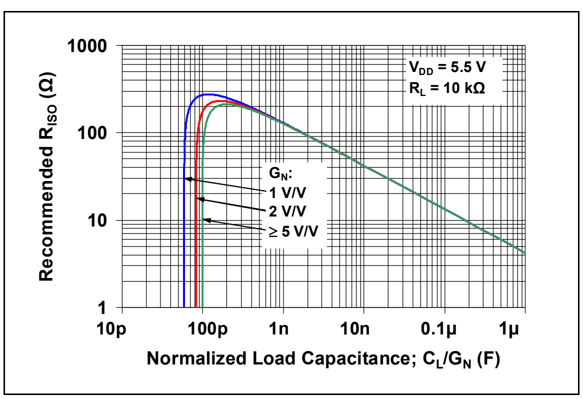


FIGURE 4-4: Recommended R_{ISO} Values for Capacitive Loads.

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6286 SPICE macro model are very helpful.

4.4 Supply Bypass

MCP6286 op amp's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6286 op amp's bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-5.

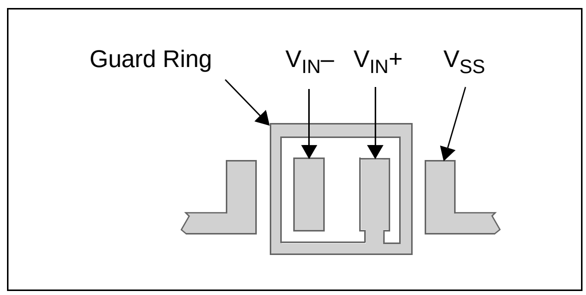


FIGURE 4-5: Example Guard Ring Layout for Inverting Gain.

1. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.6 Application Circuits

4.6.1 ACTIVE LOW-PASS FILTER

The MCP6286 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Figure 4-6 and Figure 4-7 show low-pass, second-order, Butterworth filters with a cut-off frequency of 10 Hz. The filter in Figure 4-6 has a non-inverting gain of +1 V/V, and the filter in Figure 4-7 has an inverting gain of -1 V/V.

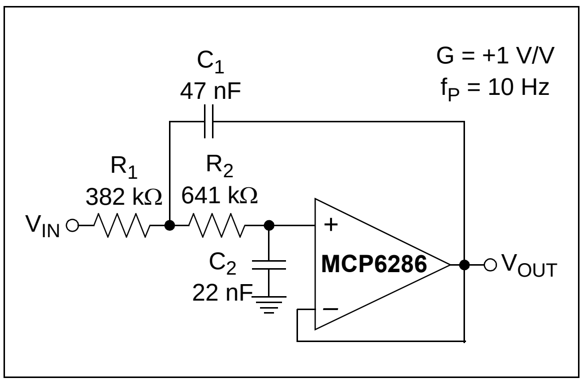


FIGURE 4-6: *Second-Order, Low-Pass Butterworth Filter with Sallen-Key Topology.*

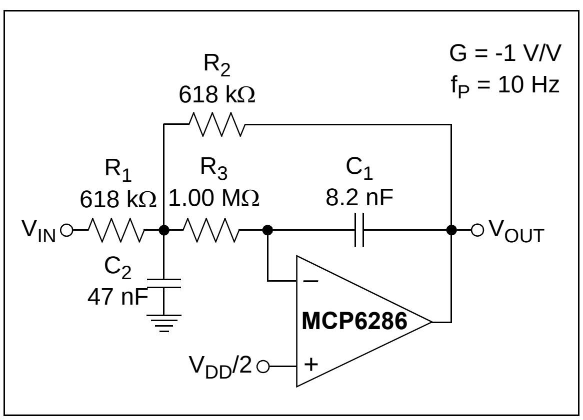


FIGURE 4-7: *Second-Order, Low-Pass Butterwork Filter with Multiple-Feedback Topology.*

4.6.2 PHOTO DETECTION

The MCP6286 op amps can be used to easily convert the signal from a sensor that produces an output current (such as a photo diode) into a voltage (a transimpedance amplifier). This is implemented with a single resistor (R_2) in the feedback loop of the amplifiers shown in Figure 4-8 and Figure 4-9. The optional capacitor (C_2) sometimes provides stability for these circuits.

A photodiode configured in the Photovoltaic mode has zero voltage potential placed across it (Figure 4-8). In this mode, the light sensitivity and linearity is maximized, making it best suited for precision applications. The key amplifier specifications for this application are: low input bias current, low noise, common mode input voltage range (including ground), and rail-to-rail output.

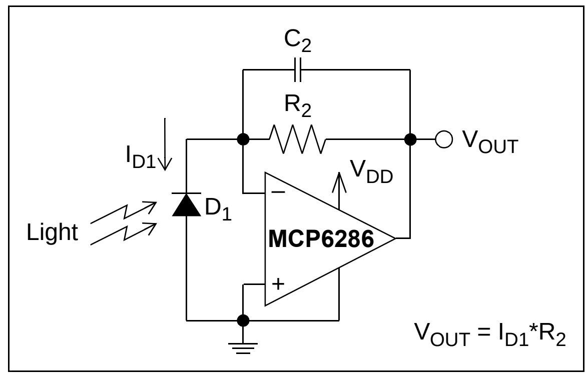


FIGURE 4-8: *Photovoltaic Mode Detector.*

In contrast, a photodiode that is configured in the Photoconductive mode has a reverse bias voltage across the photo-sensing element (Figure 4-9). This decreases the diode capacitance, which facilitates high-speed operation (e.g., high-speed digital communications). The design trade-off is increased diode leakage current and linearity errors. The op amp needs to have a wide Gain Bandwidth Product (GBWP).

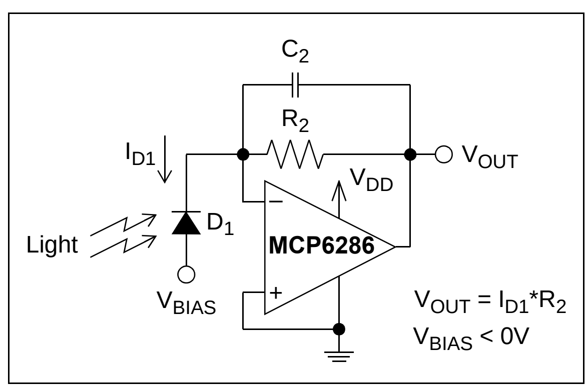


FIGURE 4-9: *Photoconductive Mode Detector.*

NOTES:

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6286 op amp.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6286 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2

5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise",* DS01228

These application notes and others are listed in the design guide:

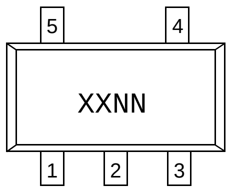
- *"Signal Chain Design Guide",* DS21825

NOTES:

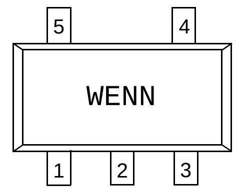
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

5-Lead SOT-23



Example:

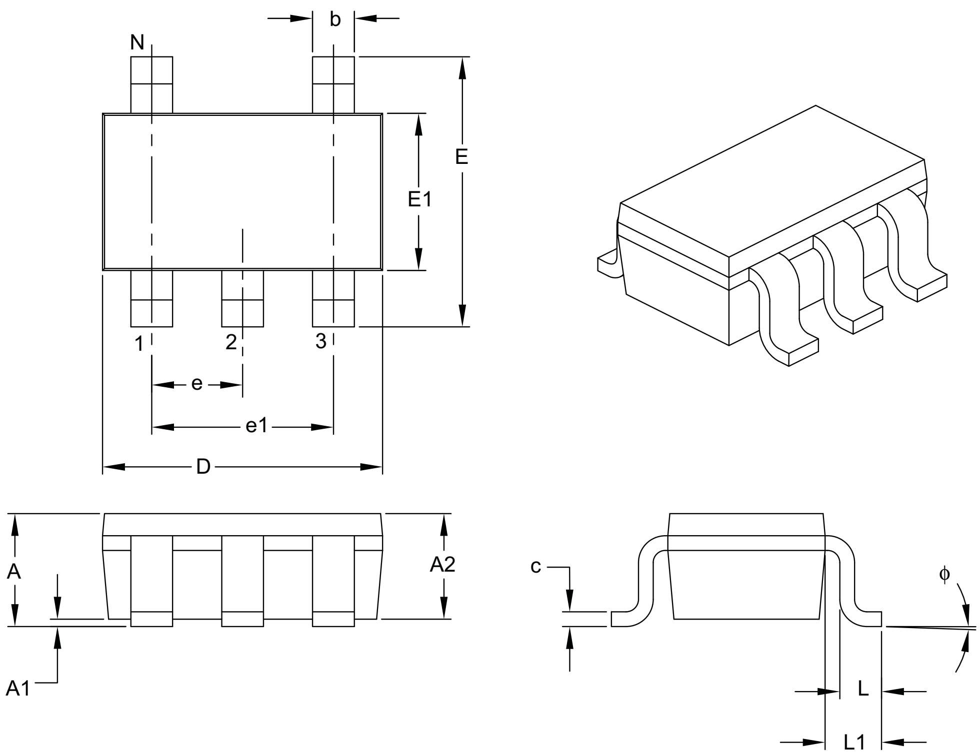


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

APPENDIX A: REVISION HISTORY

Revision A (August 2009)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6286T:	Single Op Amp (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C
Package:	OT =	Plastic Small Outline Transistor, 5-lead

Examples:

a) MCP6286T-E/OT: Tape and Reel, 5-LD SOT-23 package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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