



---

# PIC18F6393/6493/8393/8493 Data Sheet

64/80-Pin High-Performance,  
Flash Microcontrollers with LCD Driver,  
12-Bit ADC and nanoWatt Technology

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**



# MICROCHIP PIC18F6393/6493/8393/8493

## 64/80-Pin High-Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

### LCD Driver Module Features:

- Direct Driving of LCD Panel
- Up to 192 Pixels: Software-Selectable
- Programmable LCD Timing module:
  - Multiple LCD timing sources available
  - Up to four commons: Static, 1/2, 1/3 or 1/4 multiplex
  - Static, 1/2 or 1/3 bias configuration
- Can Drive LCD Panel while in Sleep mode for Low-Power Operation

### Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Ultra Low 50 nA Input Leakage
- Run mode Current Down to 14  $\mu$ A Typical
- Idle mode Currents Down to 2.3  $\mu$ A Typical
- Sleep mode Currents Down to 0.1  $\mu$ A Typical
- Timer1 Oscillator: 1.0  $\mu$ A, 32 kHz, 2V Typical
- Watchdog Timer: 1.7  $\mu$ A Typical
- Two-Speed Oscillator Start-up

### Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - Fast wake from Sleep and Idle, 1  $\mu$ s typical
  - Eight selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User-tunable to compensate for frequency drift
- Secondary Oscillator Using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

### Peripheral Highlights:

- 12-Bit, up to 12-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
- High-Current Sink/Source 25 mA/25 mA
- Four External Interrupts
- Four Input Change Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Real-Time Clock (RTC) Software module:
  - Configurable 24-hour clock, calendar, automatic 100-year or 12,800-year, day-of-week calculator
  - Uses Timer1
- Up to Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module Supporting Three-Wire SPI (all four modes) and I<sup>2</sup>C™ Master and Slave modes
- Addressable USART module:
  - Supports RS-485 and RS-232
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- Programmable 16-Level High/Low-Voltage Detection (HLVD) module:
  - Supports interrupt on High/Low-Voltage Detection

### Special Microcontroller Features:

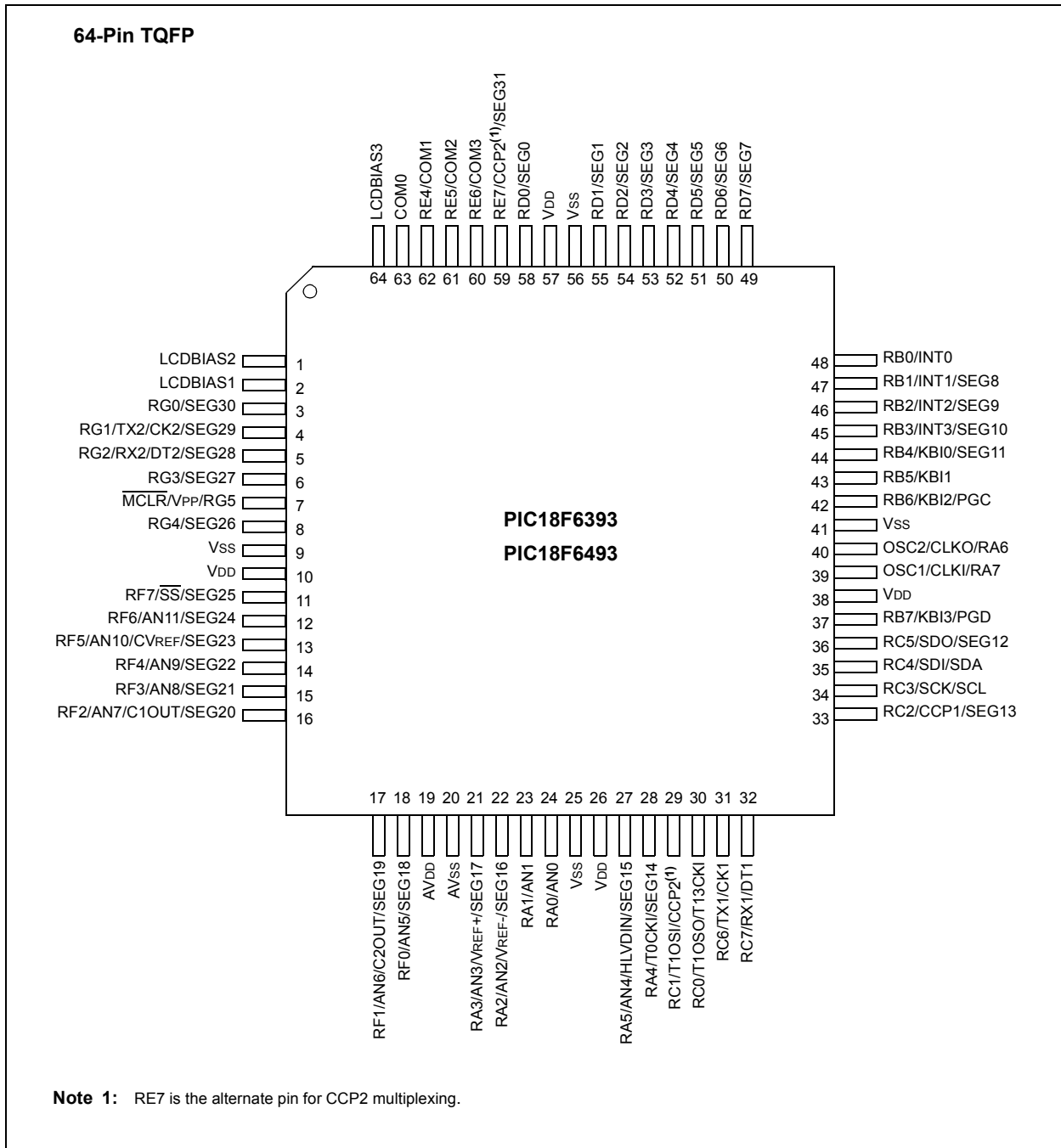
- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 1000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention: 100 Years Typical
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 132s
  - 2% stability over VDD and temperature
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Programmable Brown-out Reset (BOR) with Software Enable Option

**Note:** This document is supplemented by the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629). See Section 1.0 "Device Overview".

Device	Program Memory		Data Memory	I/O	LCD (pixel)	12-Bit A/D (channels)	CCP (PWM)	MSSP		EUSART/AUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)					SPI	Master I <sup>2</sup> C™			
PIC18F6393	8K	4096	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F6493	16K	8192	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F8393	8K	4096	768	66	192	12	2	Y	Y	1/1	2	1/3
PIC18F8493	16K	8192	768	66	192	12	2	Y	Y	1/1	2	1/3

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)  
**Pin Diagrams**

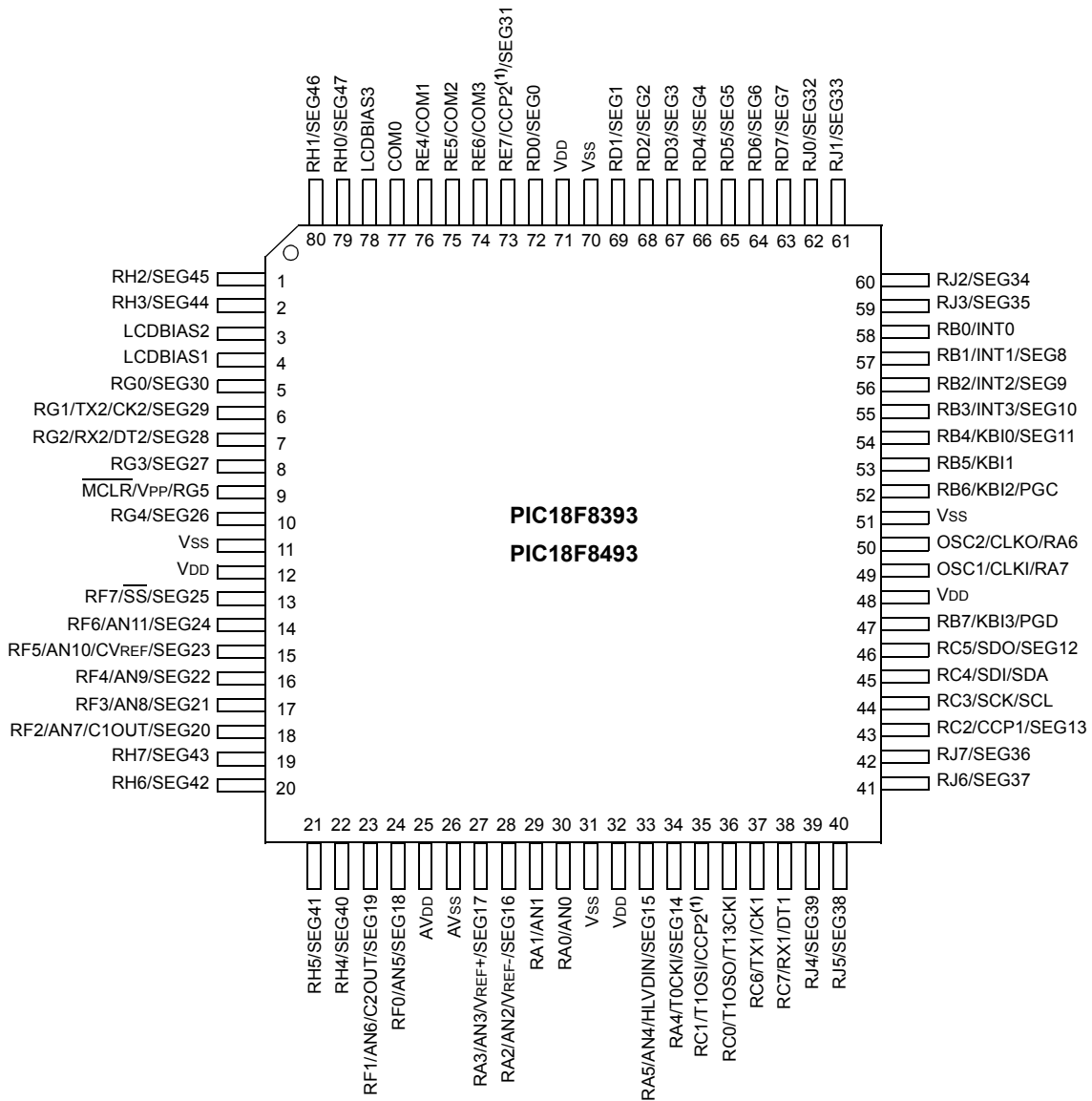


# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## Pin Diagrams (Continued)

### 80-Pin TQFP



**Note 1:** RE7 is the alternate pin for CCP2 multiplexing.

# PIC18F6393/6493/8393/8493

---

[查询PIC18F8493供应商](#)

## Table of Contents

1.0	Device Overview .....	9
2.0	12-Bit Analog-to-Digital Converter (A/D) Module .....	31
3.0	Special Features of the CPU .....	41
4.0	Electrical Characteristics .....	43
5.0	Packaging Information.....	47
	Appendix A: Revision History.....	53
	Appendix B: Device Differences.....	53
	Appendix C: Conversion Considerations .....	54
	Appendix D: Migration from Baseline to Enhanced Devices.....	54
	Appendix E: migration from Mid-Range to Enhanced Devices .....	55
	Appendix F: Migration from High-End to Enhanced Devices.....	55
	Index .....	57
	The Microchip Web Site .....	59
	Customer Change Notification Service .....	59
	Customer Support .....	59
	Reader Response .....	60
	Product Identification System.....	61

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@microchip.com](mailto:docerrors@microchip.com) or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.

# PIC18F6393/6493/8393/8493

---

[查询PIC18F8493供应商](#)

**NOTES:**



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F8393
- PIC18F6493
- PIC18F8493

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

## 1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

- I/O Ports:
  - 64-pin devices – 7 bidirectional ports
  - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
  - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
  - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
  - PIC18FX393 devices – 8 Kbytes
  - PIC18FX493 devices – 16 Kbytes

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating V<sub>DD</sub> range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended V<sub>DD</sub> range of 2.0V to 5.5V.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

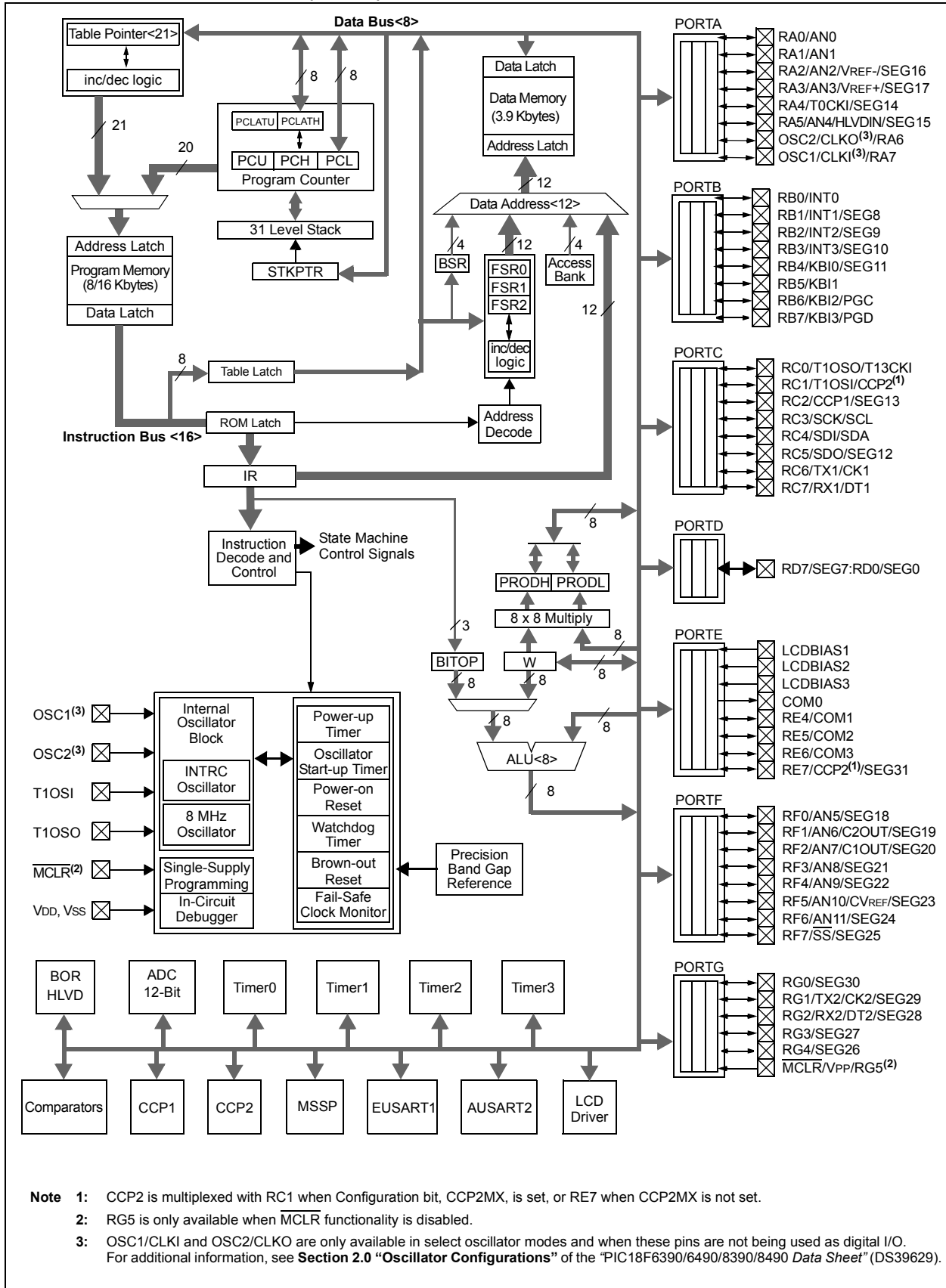
**TABLE 1-1: DEVICE FEATURES**

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	8K	16K	8K	16K
Program Memory (Instructions)	4096	8192	4096	8192
Data Memory (Bytes)	768	768	768	768
Interrupt Sources	22	22	22	22
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Number of Pixels the LCD Driver Can Drive	128 (32 SEGs x 4 COMs)	128 (32 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	12 Input Channels	12 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

# PIC18F6393/6493/8393/8493

查询PIC18F8493供应商

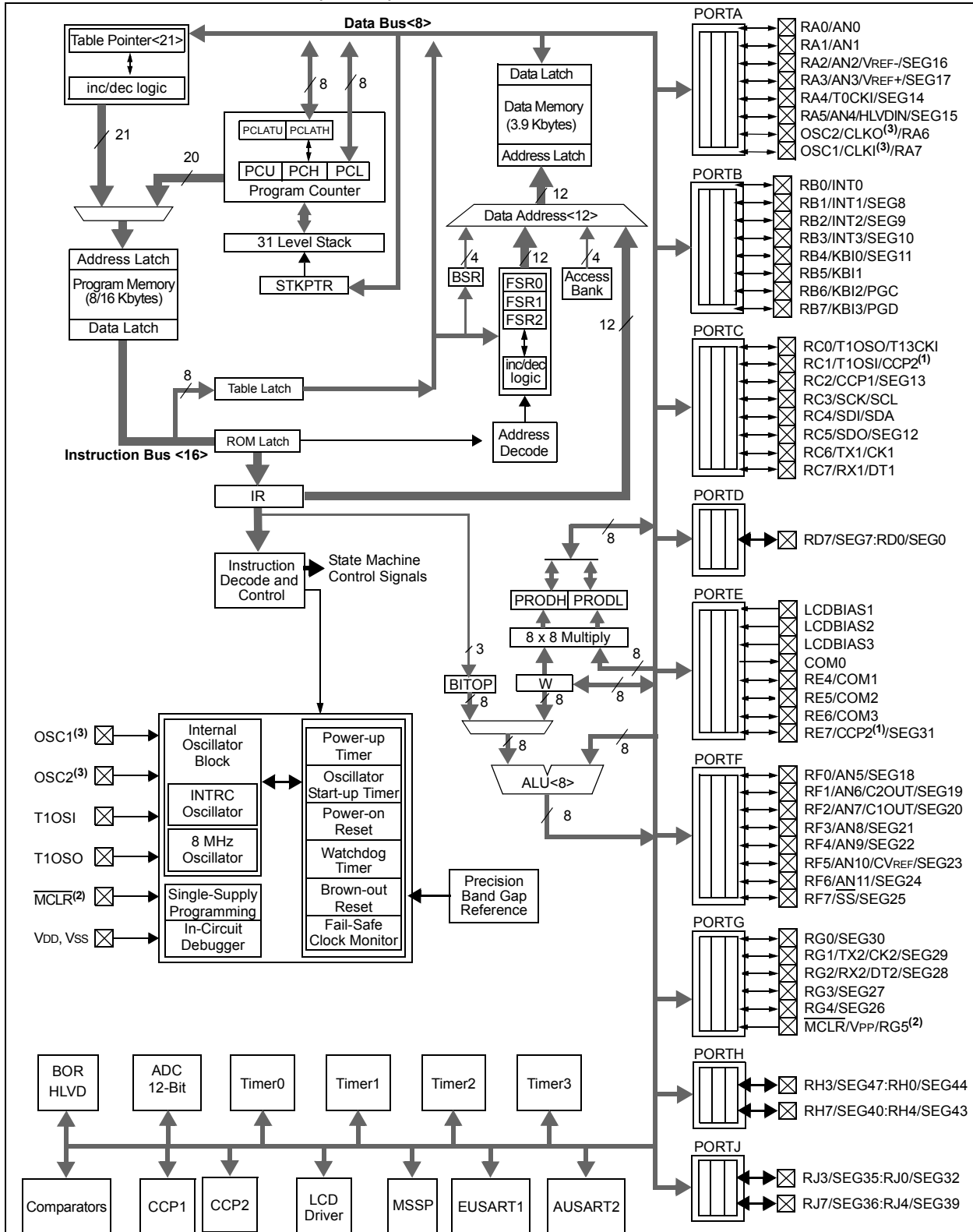
FIGURE 1-1: PIC18F6X93 (64-PIN) BLOCK DIAGRAM



# PIC18F6393/6493/8393/8493

查询PIC18F8493供应商

FIGURE 1-2: PIC18F8X93 (80-PIN) BLOCK DIAGRAM



- Note**
- 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set and RE7 when CCP2MX is not set.
  - 2: RG5 is only available when MCLR functionality is disabled.
  - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5 MCLR  VPP RG5	7	I  P I	ST   ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	39	I  I  I/O	ST  CMOS  TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	40	O  O  I/O	—  —  TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input  
 ST = Schmitt Trigger input with CMOS levels  
 I = Input  
 P = Power  
 CMOS = CMOS compatible input or output  
 Analog = Analog input  
 O = Output  
 I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

- Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0 AN0				Digital I/O. Analog Input 0.
RA1/AN1	23	I/O I	TTL Analog	Digital I/O.
RA1 AN1				Analog Input 1.
RA2/AN2/VREF-/SEG16	22	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA2 AN2				Analog Input 2.
VREF-				A/D reference voltage (Low) input.
SEG16				SEG16 output for LCD.
RA3/AN3/VREF+/SEG17	21	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA3 AN3				Analog Input 3.
VREF+				A/D reference voltage (High) input.
SEG17				SEG17 output for LCD.
RA4/T0CKI/SEG14	28	I/O I O	ST ST Analog	Digital I/O.
RA4 T0CKI				Timer0 external clock input.
SEG14				SEG14 output for LCD.
RA5/AN4/HLVDIN/SEG15	27	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA5 AN4				Analog Input 4.
HLVDIN				Low-Voltage Detect input.
SEG15				SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	48	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.  Digital I/O. External Interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	47	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	46	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	45	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	44	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	43	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	30			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	29			
RC1		I/O	ST	Digital I/O.
T1OSI		I	Analog	Timer1 oscillator input.
CCP2 <sup>(1)</sup>		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	33			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	34			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	I <sup>2</sup> C	Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC4/SDI/SDA	35			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	I <sup>2</sup> C	I <sup>2</sup> C data I/O.
RC5/SDO/SEG12	36			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	31			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	32			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0 RD0 SEG0	58	I/O O	ST Analog	PORTD is a bidirectional I/O port.  Digital I/O. SEG0 output for LCD.
RD1/SEG1 RD1 SEG1	55	I/O O	ST Analog	Digital I/O. SEG1 output for LCD.
RD2/SEG2 RD2 SEG2	54	I/O O	ST Analog	Digital I/O. SEG2 output for LCD.
RD3/SEG3 RD3 SEG3	53	I/O O	ST Analog	Digital I/O. SEG3 output for LCD.
RD4/SEG4 RD4 SEG4	52	I/O O	ST Analog	Digital I/O. SEG4 output for LCD.
RD5/SEG5 RD5 SEG5	51	I/O O	ST Analog	Digital I/O. SEG5 output for LCD.
RD6/SEG6 RD6 SEG6	50	I/O O	ST Analog	Digital I/O. SEG6 output for LCD.
RD7/SEG7 RD7 SEG7	49	I/O O	ST Analog	Digital I/O. SEG7 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTE is a bidirectional I/O port.
LCDBIAS1 LCDBIAS1	2	I	Analog	BIAS1 input for LCD.
LCDBIAS2 LCDBIAS2	1	I	Analog	BIAS2 input for LCD.
LCDBIAS3 LCDBIAS3	64	I	Analog	BIAS3 input for LCD.
COM0 COM0	63	O	Analog	COM0 output for LCD.
RE4/COM1 RE4 COM1	62	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	61	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	60	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 <sup>(2)</sup> SEG31	59	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description	
	TQFP				
RF0/AN5/SEG18	18	I/O	ST	PORTF is a bidirectional I/O port. Digital I/O.	
RF0			I		Analog
AN5			O		Analog
SEG18				SEG18 output for LCD.	
RF1/AN6/C2OUT/SEG19	17	I/O	ST	Digital I/O.	
RF1			I		Analog
AN6			O		—
C2OUT			O		Analog
SEG19				SEG19 output for LCD.	
RF2/AN7/C1OUT/SEG20	16	I/O	ST	Digital I/O.	
RF2			I		Analog
AN7			O		—
C1OUT			O		Analog
SEG20				SEG20 output for LCD.	
RF3/AN8/SEG21	15	I/O	ST	Digital I/O.	
RF3			I		Analog
AN8			O		Analog
SEG21				SEG21 output for LCD.	
RF4/AN9/SEG22	14	I/O	ST	Digital I/O.	
RF4			I		Analog
AN9			O		Analog
SEG22				SEG22 output for LCD.	
RF5/AN10/CVREF/SEG23	13	I/O	ST	Digital I/O.	
RF5			I		Analog
AN10			O		Analog
CVREF			O		Analog
SEG23				Comparator reference voltage output. SEG23 output for LCD.	
RF6/AN11/SEG24	12	I/O	ST	Digital I/O.	
RF6			I		Analog
AN11			O		Analog
SEG24				SEG24 output for LCD.	
RF7/ $\overline{SS}$ /SEG25	11	I/O	ST	Digital I/O.	
RF7			I		TTL
$\overline{SS}$			O		Analog
SEG25					

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
PORTG is a bidirectional I/O port.				
RG0/SEG30 RG0 SEG30	3	I/O O	ST Analog	Digital I/O. SEG30 output for LCD.
RG1/TX2/CK2/SEG29 RG1 TX2 CK2 SEG29	4	I/O O I/O O	ST — ST Analog	Digital I/O. AUSART2 asynchronous transmit. AUSART2 synchronous clock (see related RX2/DT2). SEG29 output for LCD.
RG2/RX2/DT2/SEG28 RG2 RX2 DT2 SEG28	5	I/O I I/O O	ST ST ST Analog	Digital I/O. AUSART2 asynchronous receive. AUSART2 synchronous data (see related TX2/CK2). SEG28 output for LCD.
RG3/SEG27 RG3 SEG27	6	I/O O	ST Analog	Digital I/O. SEG27 output for LCD.
RG4/SEG26 RG4 SEG26	8	I/O O	ST Analog	Digital I/O. SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$ pin.
Vss	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVss	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5 MCLR	9	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		
RG5		I	ST	Digital input.
OSC1/CLKI/RA7 OSC1	49	I	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI		I	CMOS	
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6 OSC2	50	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	30	I/O	TTL	PORTA is a bidirectional I/O port. Digital I/O. Analog Input 0.
RA0 AN0		I	Analog	
RA1/AN1	29	I/O	TTL	Digital I/O. Analog Input 1.
RA1 AN1		I	Analog	
RA2/AN2/VREF-/SEG16	28	I/O	TTL	Digital I/O. Analog Input 2. A/D reference voltage (Low) input. SEG16 output for LCD.
RA2		I	Analog	
AN2		I	Analog	
VREF- SEG16		O	Analog	
RA3/AN3/VREF+/SEG17	27	I/O	TTL	Digital I/O. Analog Input 3. A/D reference voltage (High) input. SEG17 output for LCD.
RA3		I	Analog	
AN3		I	Analog	
VREF+ SEG17		O	Analog	
RA4/T0CKI/SEG14	34	I/O	ST	Digital I/O. Timer0 external clock input. SEG14 output for LCD.
RA4		I	ST	
T0CKI SEG14		O	Analog	
RA5/AN4/HLVDIN/SEG15	33	I/O	TTL	Digital I/O. Analog Input 4. Low-Voltage Detect input. SEG15 output for LCD.
RA5		I	Analog	
AN4		I	Analog	
HLVDIN SEG15		O	Analog	
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	58	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.  Digital I/O. External interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	57	I/O I O	TTL ST Analog	Digital I/O. External interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	56	I/O I O	TTL ST Analog	Digital I/O. External interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	55	I/O I O	TTL ST Analog	Digital I/O. External interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	54	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	53	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	52	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	47	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 <sup>(1)</sup>		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	I <sup>2</sup> C	Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC4/SDI/SDA	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	I <sup>2</sup> C	I <sup>2</sup> C data I/O.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0 RD0 SEG0	72	I/O O	ST Analog	PORTD is a bidirectional I/O port.  Digital I/O. SEG0 output for LCD.
RD1/SEG1 RD1 SEG1	69	I/O O	ST Analog	Digital I/O. SEG1 output for LCD.
RD2/SEG2 RD2 SEG2	68	I/O O	ST Analog	Digital I/O. SEG2 output for LCD.
RD3/SEG3 RD3 SEG3	67	I/O O	ST Analog	Digital I/O. SEG3 output for LCD.
RD4/SEG4 RD4 SEG4	66	I/O O	ST Analog	Digital I/O. SEG4 output for LCD.
RD5/SEG5 RD5 SEG5	65	I/O O	ST Analog	Digital I/O. SEG5 output for LCD.
RD6/SEG6 RD6 SEG6	64	I/O O	ST Analog	Digital I/O. SEG6 output for LCD.
RD7/SEG7 RD7 SEG7	63	I/O O	ST Analog	Digital I/O. SEG7 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
LCDBIAS1 LCDBIAS1	4	I	Analog	BIAS1 input for LCD.
LCDBIAS2 LCDBIAS2	3	I	Analog	BIAS2 input for LCD.
LCDBIAS3 LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
COM0 COM0	77	O	Analog	COM0 output for LCD.
RE4/COM1 RE4 COM1	76	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	75	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	74	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 <sup>(2)</sup> SEG31	73	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF0/AN5/SEG18	24	I/O	ST	PORTF is a bidirectional I/O port. Digital I/O. Analog Input 5. SEG18 output for LCD.
RF0		I	Analog	
AN5		O	Analog	
SEG18		O	Analog	
RF1/AN6/C2OUT/SEG19	23	I/O	ST	Digital I/O. Analog Input 6. Comparator 2 output. SEG19 output for LCD.
RF1		I	Analog	
AN6		O	—	
C2OUT		O	Analog	
SEG19		O	Analog	
RF2/AN7/C1OUT/SEG20	18	I/O	ST	Digital I/O. Analog Input 7. Comparator 1 output. SEG20 output for LCD.
RF2		I	Analog	
AN7		O	—	
C1OUT		O	Analog	
SEG20		O	Analog	
RF3/AN8/SEG21	17	I/O	ST	Digital I/O. Analog Input 8. SEG21 output for LCD.
RF3		I	Analog	
AN8		O	Analog	
SEG21		O	Analog	
RF4/AN9/SEG22	16	I/O	ST	Digital I/O. Analog Input 9. SEG22 output for LCD.
RF4		I	Analog	
AN9		O	Analog	
SEG22		O	Analog	
RF5/AN10/CVREF/SEG23	15	I/O	ST	Digital I/O. Analog Input 10. Comparator reference voltage output. SEG23 output for LCD.
RF5		I	Analog	
AN10		O	Analog	
CVREF		O	Analog	
SEG23		O	Analog	
RF6/AN11/SEG24	14	I/O	ST	Digital I/O. Analog Input 11. SEG24 output for LCD.
RF6		I	Analog	
AN11		O	Analog	
SEG24		O	Analog	
RF7/ $\overline{SS}$ /SEG25	13	I/O	ST	Digital I/O. SPI slave select input. SEG25 output for LCD.
RF7		I	TTL	
$\overline{SS}$		O	Analog	
SEG25		O	Analog	

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/SEG30 RG0 SEG30	5	I/O O	ST Analog	PORTG is a bidirectional I/O port.  Digital I/O. SEG30 output for LCD.
RG1/TX2/CK2/SEG29 RG1 TX2 CK2 SEG29	6	I/O O I/O O	ST — ST Analog	Digital I/O. AUSART2 asynchronous transmit. AUSART2 synchronous clock (see related RX2/DT2). SEG29 output for LCD.
RG2/RX2/DT2/SEG28 RG2 RX2 DT2 SEG28	7	I/O I I/O O	ST ST ST Analog	Digital I/O. AUSART2 asynchronous receive. AUSART2 synchronous data (see related TX2/CK2). SEG28 output for LCD.
RG3/SEG27 RG3 SEG27	8	I/O O	ST Analog	Digital I/O. SEG27 output for LCD.
RG4/SEG26 RG4 SEG26	10	I/O O	ST Analog	Digital I/O. SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$ pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/SEG47 RH0 SEG47	79	I/O O	ST Analog	Digital I/O. SEG47 output for LCD.
RH1/SEG46 RH1 SEG46	80	I/O O	ST Analog	Digital I/O. SEG46 output for LCD.
RH2/SEG45 RH2 SEG45	1	I/O O	ST Analog	Digital I/O. SEG45 output for LCD.
RH3/SEG44 RH3 SEG44	2	I/O O	ST Analog	Digital I/O. SEG44 output for LCD.
RH4/SEG40 RH4 SEG40	22	I/O O	ST Analog	Digital I/O. SEG40 output for LCD.
RH5/SEG41 RH5 SEG41	21	I/O O	ST Analog	Digital I/O. SEG41 output for LCD.
RH6/SEG42 RH6 SEG42	20	I/O O	ST Analog	Digital I/O. SEG42 output for LCD.
RH7/SEG43 RH7 SEG43	19	I/O O	ST Analog	Digital I/O. SEG43 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0/SEG32 RJ0 SEG32	62	I/O O	ST Analog	PORTJ is a bidirectional I/O port.  Digital I/O. SEG32 output for LCD.
RJ1/SEG33 RJ1 SEG33	61	I/O O	ST Analog	Digital I/O. SEG33 output for LCD.
RJ2/SEG34 RJ2 SEG34	60	I/O O	ST Analog	Digital I/O. SEG34 output for LCD.
RJ3/SEG35 RJ3 SEG35	59	I/O O	ST Analog	Digital I/O. SEG35 output for LCD.
RJ4/SEG39 RJ4 SEG39	39	I/O O	ST Analog	Digital I/O. SEG39 output for LCD.
RJ5/SEG38 RJ5 SEG38	40	I/O O	ST Analog	Digital I/O SEG38 output for LCD.
RJ6/SEG37 RJ6 SEG37	41	I/O O	ST Analog	Digital I/O. SEG37 output for LCD.
RJ7/SEG36 RJ7 SEG36	42	I/O O	ST Analog	Digital I/O. SEG36 output for LCD.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVSS	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module converts an analog input signal to a 12-bit digital number. The module has 12 inputs for both PIC18F6393/6493 (64-pin) and PIC18F8393/8493 (80-pin) devices.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

#### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

- bit 7-6      **Unimplemented:** Read as '0'
- bit 5-2      **CHS<3:0>:** Analog Channel Select bits
- 0000 = Channel 0 (AN0)
  - 0001 = Channel 1 (AN1)
  - 0010 = Channel 2 (AN2)
  - 0011 = Channel 3 (AN3)
  - 0100 = Channel 4 (AN4)
  - 0101 = Channel 5 (AN5)
  - 0110 = Channel 6 (AN6)
  - 0111 = Channel 7 (AN7)
  - 1000 = Channel 8 (AN8)
  - 1001 = Channel 9 (AN9)
  - 1010 = Channel 10 (AN10)
  - 1011 = Channel 11 (AN11)
  - 1100 = Unimplemented<sup>(1)</sup>
  - 1101 = Unimplemented<sup>(1)</sup>
  - 1110 = Unimplemented<sup>(1)</sup>
  - 1111 = Unimplemented<sup>(1)</sup>
- bit 1      **GO/DONE:** A/D Conversion Status bit
- When **ADON** = 1:
- 1 = A/D conversion in progress
  - 0 = A/D Idle
- bit 0      **ADON:** A/D On bit
- 1 = A/D Converter module is enabled
  - 0 = A/D Converter module is disabled

**Note 1:** Performing a conversion on unimplemented channels will return a floating input measurement.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

**Unimplemented:** Read as '0'

bit 5-4

**VCFG<1:0>:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0

**PCFG<3:0>:** A/D Port Configuration Control bits

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD<sup>(1)</sup>

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

The analog reference voltage is software-selectable to either the device's positive and negative supply voltage (AVDD and AVSS), or the voltage level on the RA3/AN3/VREF+/SEG17 and RA2/AN2/VREF-/SEG16 pins.

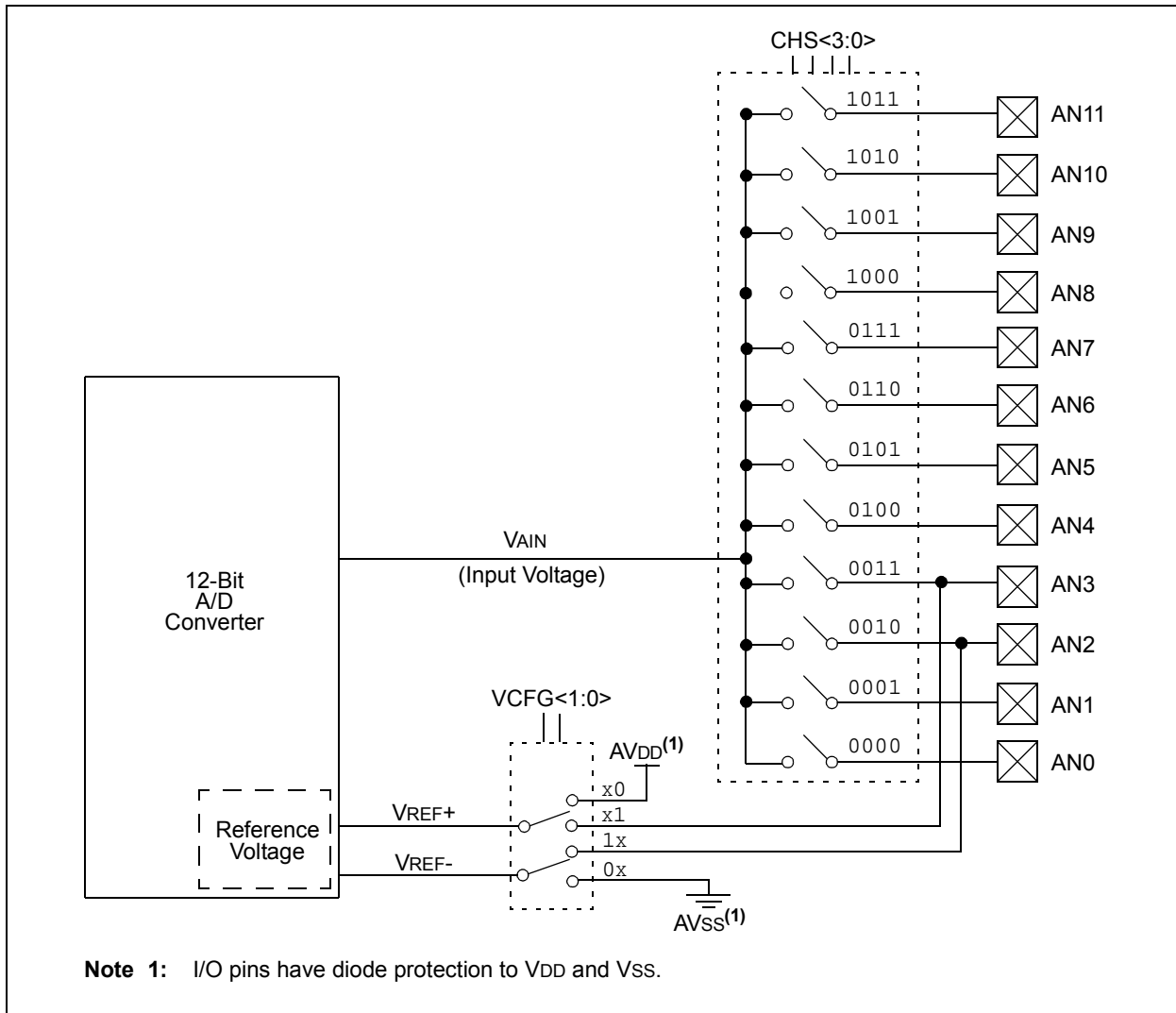
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**



# PIC18F6393/6493/8393/8493

## 查询PIC18F8493供应商

The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

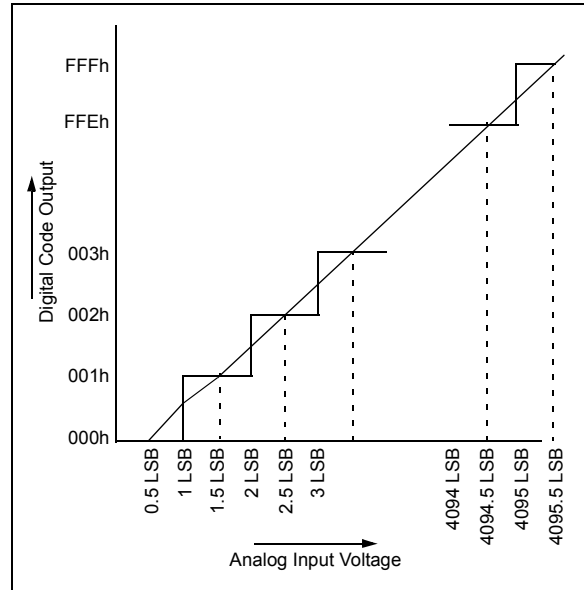
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

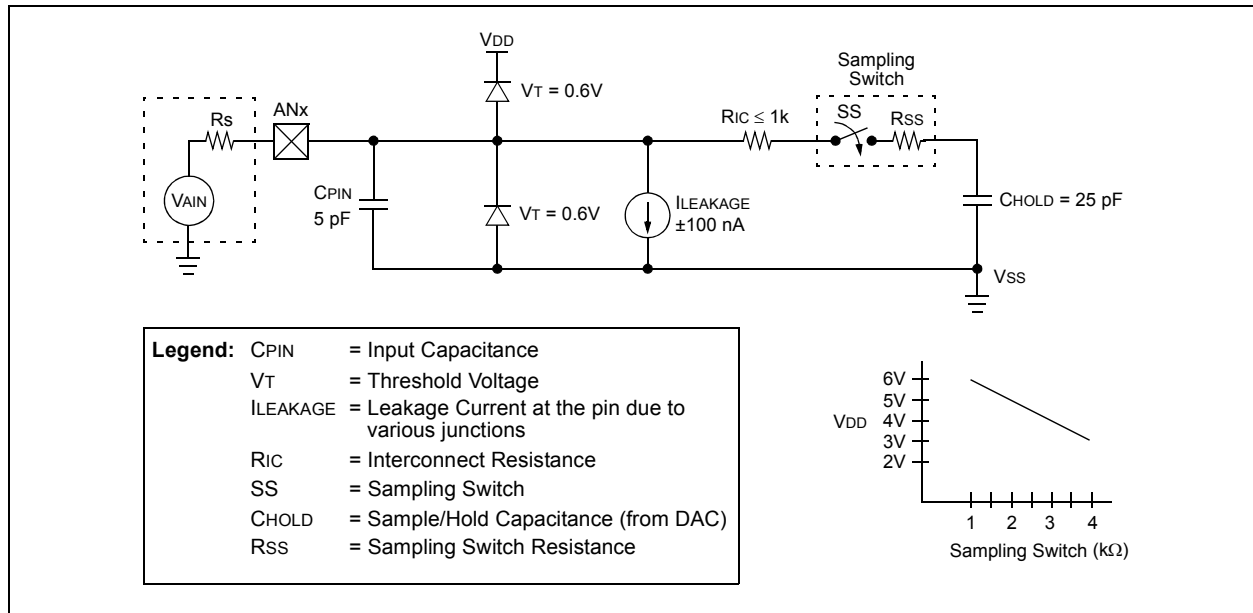
1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
  - Clear ADIF bit
  - Set ADIE bit
  - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
  - Set GO/DONE bit (ADCON0<1>)

5. Wait for A/D conversion to complete by either:
  - Polling for the GO/DONE bit to be cleared
  - OR
  - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For the next conversion, go to Step 1 or Step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**



**FIGURE 2-3: ANALOG INPUT MODEL**



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

### EQUATION 2-1: A/D ACQUISITION TIME

$$\begin{aligned}TACQ &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF\end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned}V_{\text{HOLD}} &= (V_{\text{REF}} - (V_{\text{REF}}/4096)) \cdot (1 - e^{-(Tc/CHOLD)(R_{\text{IC}} + R_{\text{SS}} + R_{\text{S}})}) \\ \text{or} \\ Tc &= (CHOLD)(R_{\text{IC}} + R_{\text{SS}} + R_{\text{S}}) \ln(1/4096)\end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$TACQ = TAMP + TC + TCOFF$$

$$TAMP = 0.2 \mu\text{s}$$

$$\begin{aligned}TCOFF &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &= (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &= 1.2 \mu\text{s}\end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

$$\begin{aligned}Tc &= -(CHOLD)(R_{\text{IC}} + R_{\text{SS}} + R_{\text{S}}) \ln(1/4096) \mu\text{s} \\ &= -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu\text{s} \\ &= 1.56 \mu\text{s}\end{aligned}$$

$$\begin{aligned}TACQ &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &= 2.96 \mu\text{s}\end{aligned}$$

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software-selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (See parameter 130 for more information.)

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 $\mu$ s
Operation	ADCS<2:0>	Maximum Fosc
2 TOSC	000	2.5 MHz
4 TOSC	100	5 MHz
8 TOSC	001	10 MHz
16 TOSC	101	20 MHz
32 TOSC	010	40 MHz
64 TOSC	110	40 MHz
RC <sup>(1)</sup>	x11	1 MHz <sup>(2)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.4 Operation in Power-Managed Modes

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used in that mode. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction, and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

**Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the  $\text{ACQT}\langle 2:0 \rangle$  bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set, the  $\text{ACQT}\langle 2:0 \rangle$  bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will *not* be updated with the partially completed A/D conversion sample. This means the  $\text{ADRESH:ADRESL}$  registers will continue to contain the value of the last completed conversion (or the last value written to the  $\text{ADRESH:ADRESL}$  registers).

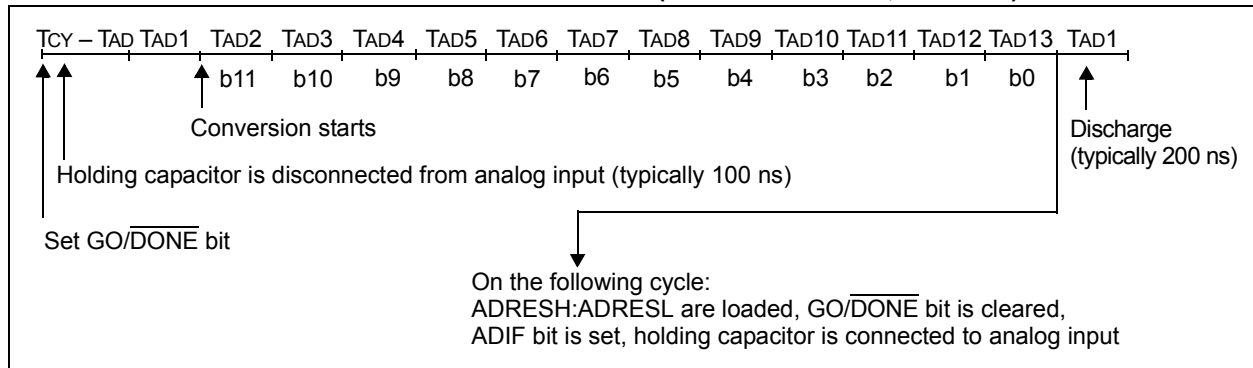
After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2  $\mu\text{s}$  after enabling the A/D before beginning an acquisition and conversion cycle.

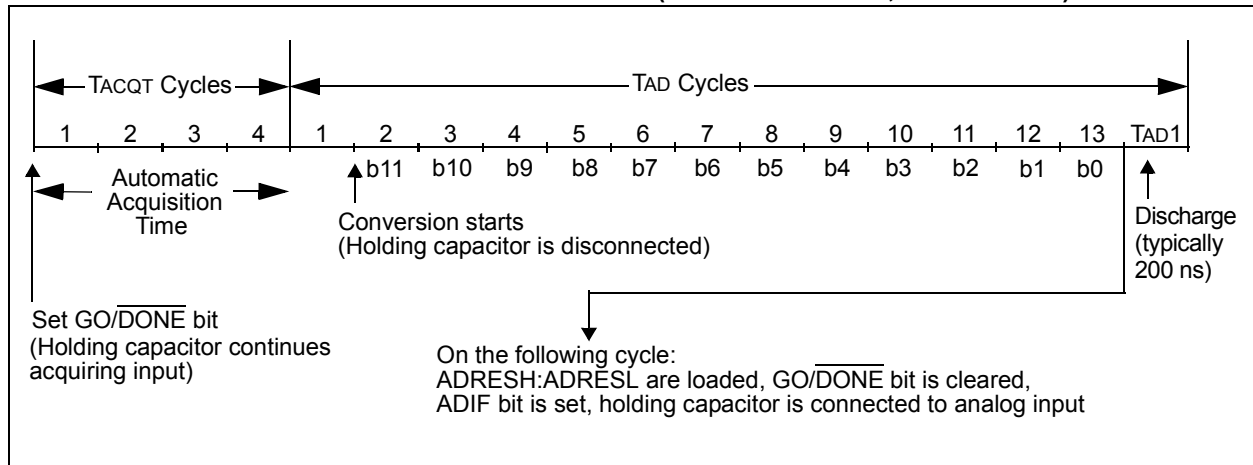
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES ( $\text{ACQT}\langle 2:0 \rangle = 000, \text{TACQ} = 0$ )**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES ( $\text{ACQT}\langle 2:0 \rangle = 010, \text{TACQ} = 4 \text{TAD}$ )**



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location).

The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(3)
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	(3)
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	—	—	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	—	—	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	—	—	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte								(3)
ADRESL	A/D Result Register Low Byte								(3)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(3)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7 <sup>(1)</sup>	TRISA6 <sup>(1)</sup>	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH <sup>(2)</sup>	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**2:** These registers are not implemented on 64-pin devices.

**3:** For these Reset values, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to **Section 23.1 “Configuration Bits”** in the “PIC18F6390/6490/8390/8490 Data Sheet” (DS39629). Device ID information presented in this section is for the PIC18F6393/6493/8393/8493 devices only.

PIC18F6393/6493/8393/8493 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

## 3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh   DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(1)</sup>
3FFFFFh   DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(1)</sup>

**Legend:** x = unknown

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

### Legend:

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-5                      **DEV<2:0>**: Device ID bits  
 See Register 3-2 for a complete listing.

bit 4-0                      **REV<4:0>**: Revision ID bits  
 These bits are used to indicate the device revision.

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

### Legend:

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-0                      **DEV10:DEV3**: Device ID bits

Device	DEV<10:3> (DEVID2<7:0>)	DEV<2:0> (DEVID1<7:5>)
PIC18F6393	0001 1010	000
PIC18F6493	0000 1110	000
PIC18F8393	0001 1010	001
PIC18F8493	0000 1110	001

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 4.0 ELECTRICAL CHARACTERISTICS

**Note:** Other than some basic data, this section documents only the PIC18F6393/6493/8393/8493 devices' specifications that differ from those of the PIC18F6390/6490/8390/8490 devices. For detailed information on the electrical specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 *Data Sheet*" (DS39629).

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to V <sub>SS</sub> (except V <sub>DD</sub> and $\overline{\text{MCLR}}$ ) .....	-0.3V to (V <sub>DD</sub> + 0.3V)
Voltage on V <sub>DD</sub> with respect to V <sub>SS</sub> .....	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V <sub>SS</sub> ( <b>Note 2</b> ) .....	0V to +13.25V
Total power dissipation ( <b>Note 1</b> ) .....	1.0W
Maximum current out of V <sub>SS</sub> pin .....	300 mA
Maximum current into V <sub>DD</sub> pin .....	250 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> ) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> ) .....	±20 mA
Maximum output current sunk by any I/O pin .....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports .....	200 mA

**Note 1:** Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

**2:** Voltage spikes below V<sub>SS</sub> at the  $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the  $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$  pin, rather than pulling this pin directly to V<sub>SS</sub>.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

FIGURE 4-1: PIC18F6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

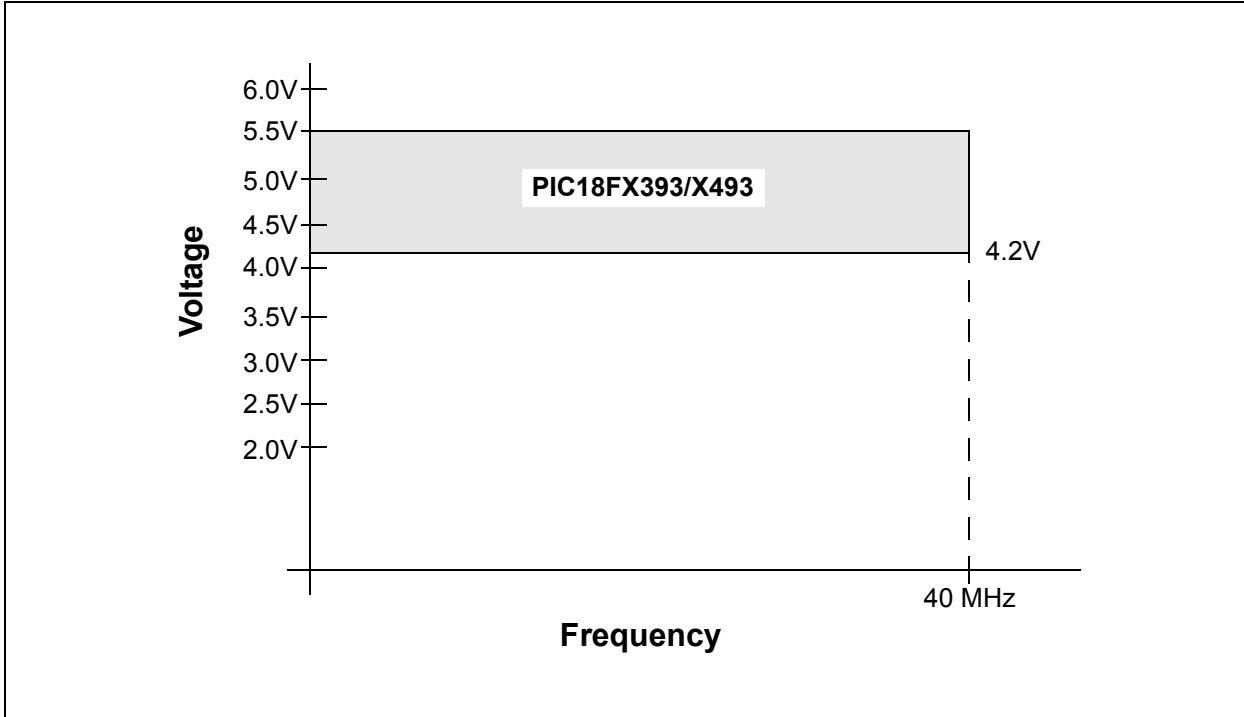
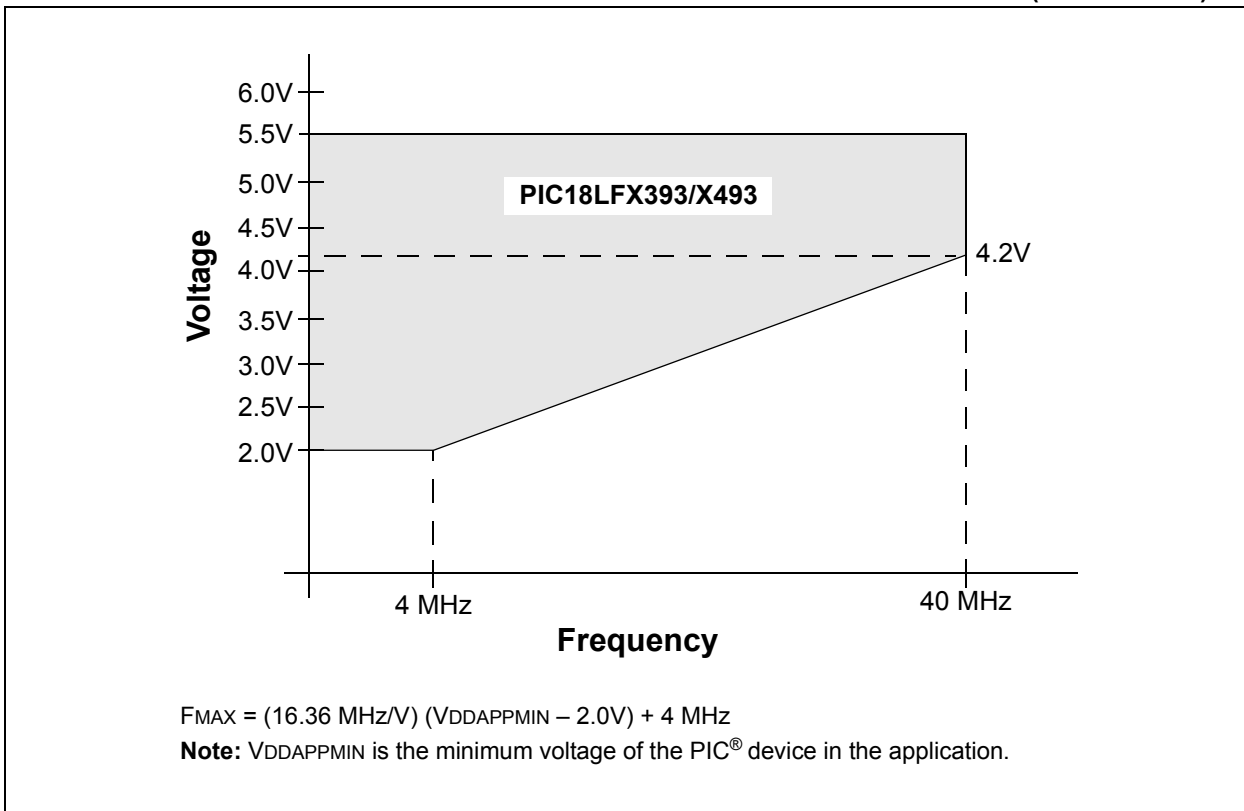


FIGURE 4-2: PIC18LF6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F6393/6493/8393/8493 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	$\pm 2.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.0$	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	+1.5/-1.0	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	+1.5/-1.0	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	$\pm 5$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 3$	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	$\pm 2.00$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.00$	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed <sup>(1)</sup>			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$	
A20	$\Delta V_{REF}$	Reference Voltage Range ( $V_{REFH} - V_{REFL}$ )	3	—	$V_{DD} - V_{SS}$	V	For 12-bit resolution	
A21	$V_{REFH}$	Reference Voltage High	$V_{SS} + \Delta V_{REF}$	—	$V_{DD}$	V	For 12-bit resolution	
A22	$V_{REFL}$	Reference Voltage Low	$V_{SS}$	—	$V_{DD} - \Delta V_{REF}$	V	For 12-bit resolution	
A25	$V_{AIN}$	Analog Input Voltage	$V_{REFL}$	—	$V_{REFH}$	V		
A30	$Z_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	k $\Omega$		
A50	IREF	$V_{REF}$ Input Current <sup>(2)</sup>	—	—	5	$\mu A$	During $V_{AIN}$ acquisition. During A/D conversion cycle.	
			—	—	150	$\mu A$		

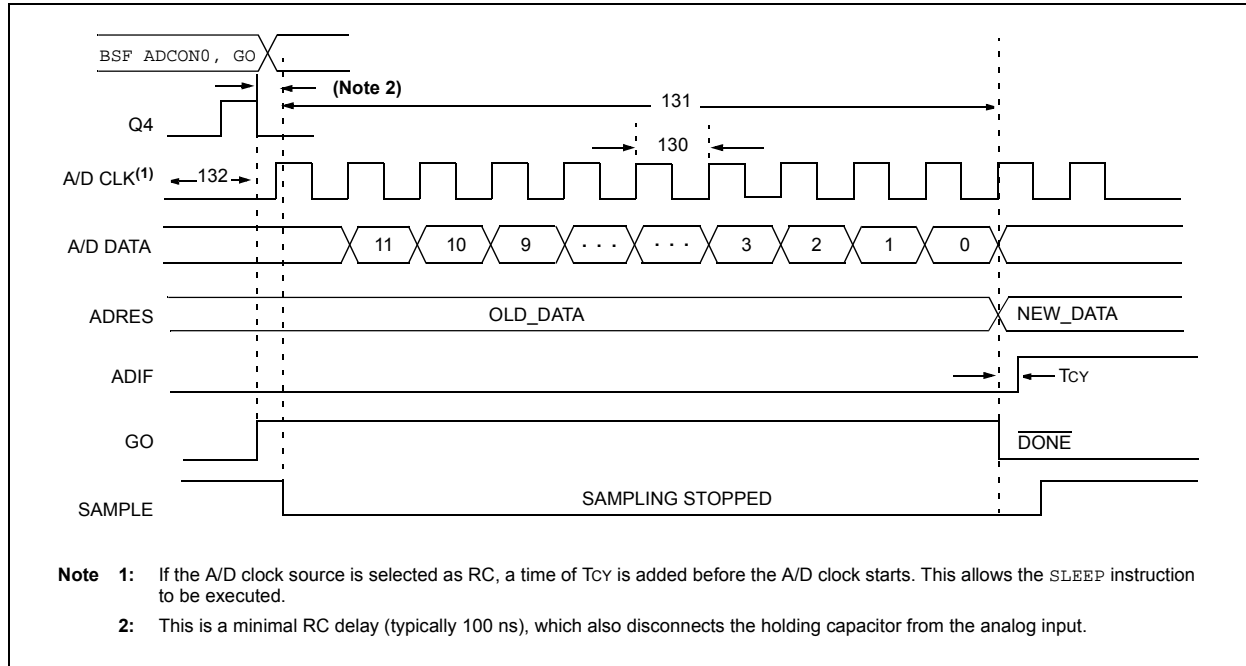
**Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**Note 2:**  $V_{REFH}$  current is from the RA3/AN3/ $V_{REF+}$ /SEG17 pin or  $V_{DD}$ , whichever is selected as the  $V_{REFH}$  source.  $V_{REFL}$  current is from the RA2/AN2/ $V_{REF-}$ /SEG16 pin or  $V_{SS}$ , whichever is selected as the  $V_{REFL}$  source.

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

**FIGURE 4-3: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	μs	TOSC based, VREF ≥ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	μs	VDD = 3.0V; TOSC based, VREF full range
		PIC18FXXXX	—	1	μs	A/D RC mode	
		PIC18LFXXXX	—	3	μs	VDD = 3.0V; A/D RC mode	
131	T <sub>cnv</sub>	Conversion Time (not including acquisition time) <sup>(2)</sup>	13	14	TAD		
132	T <sub>acq</sub>	Acquisition Time <sup>(3)</sup>	1.4	—	μs		
135	T <sub>swc</sub>	Switching Time from Convert → Sample	—	(Note 4)			
137	T <sub>dis</sub>	Discharge Time	0.2	—	μs		

- Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
- Note 2:** ADRES registers may be read on the following T<sub>cy</sub> cycle.
- Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (R<sub>s</sub>) on the input channels is 50Ω.
- Note 4:** On the following cycle of the device clock.

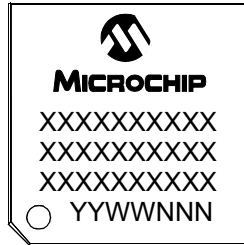
# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

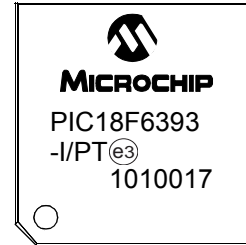
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

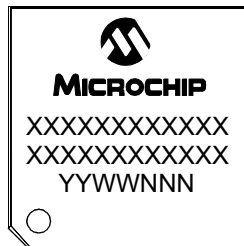
64-Lead TQFP (10x10x1mm)



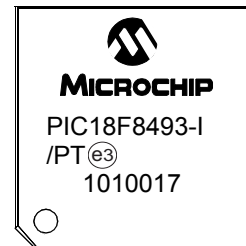
Example



80-Lead TQFP (12x12x1mm)



Example



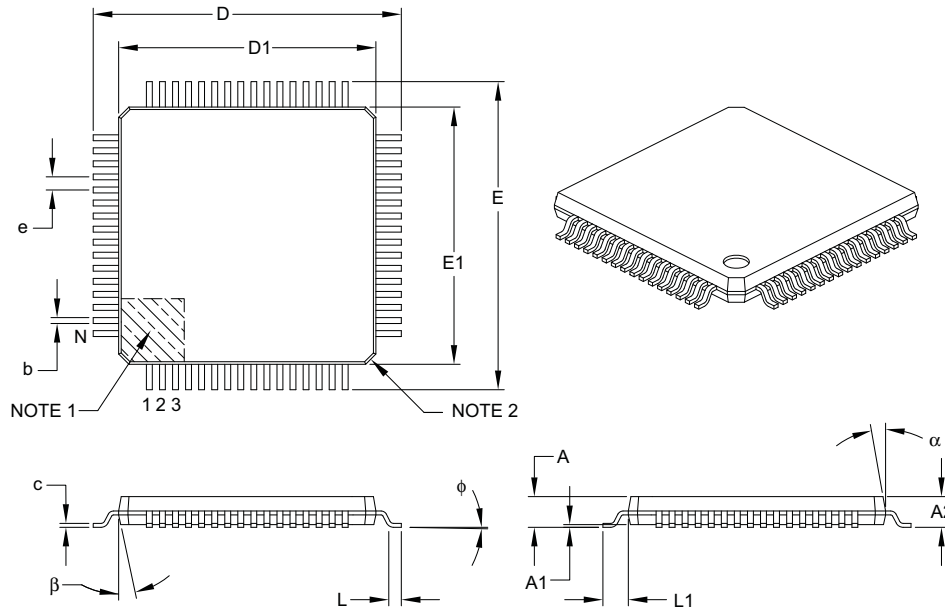
<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	$\phi$	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	$\alpha$	11°	12°	13°
Mold Draft Angle Bottom	$\beta$	11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

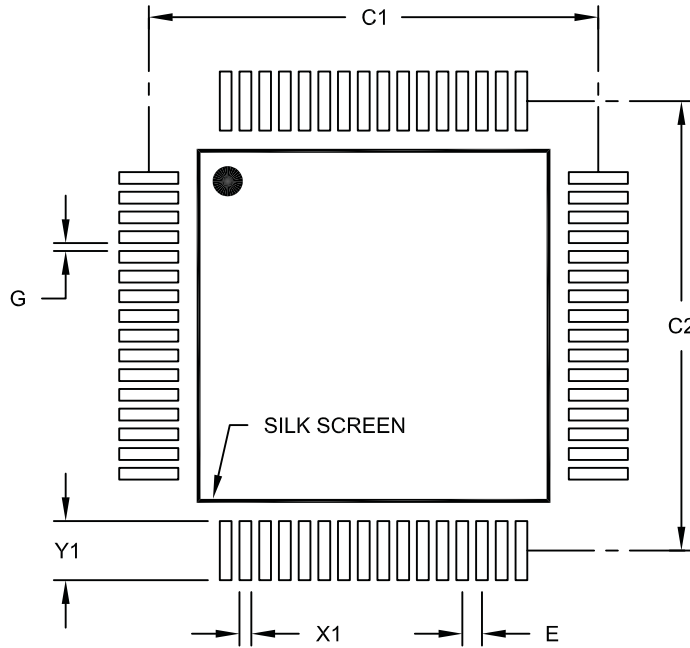


# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		MILLIMETERS		
		MIN	NOM	MAX
Dimension Limits	Units			
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

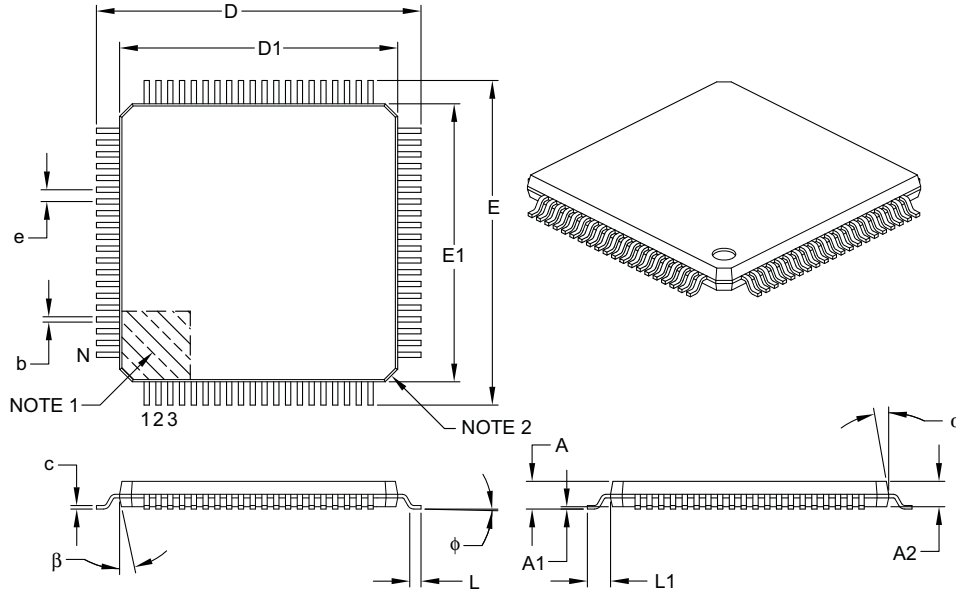
Microchip Technology Drawing No. C04-2085A

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	80		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

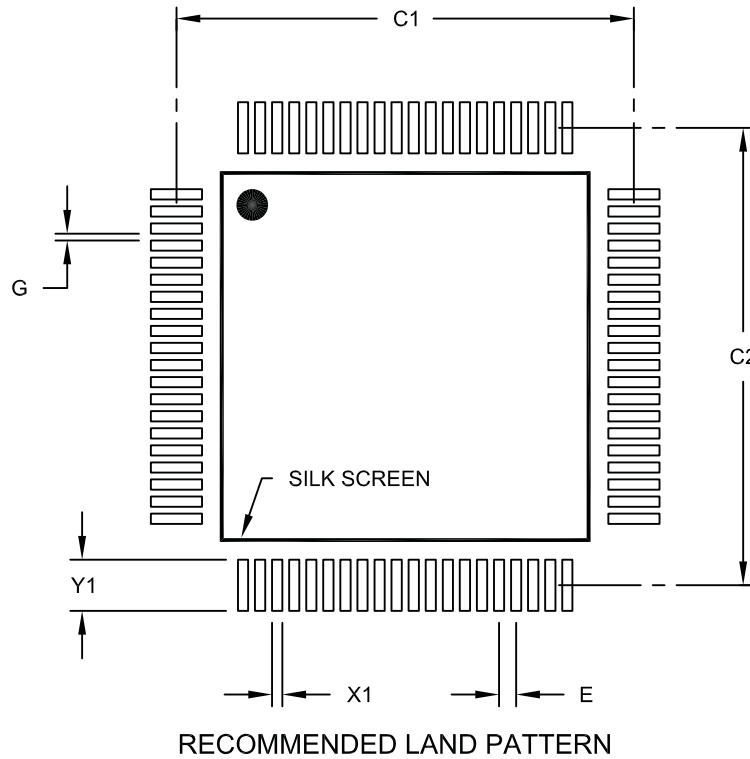
Microchip Technology Drawing C04-092B

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## 80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092A

# PIC18F6393/6493/8393/8493

---

[查询PIC18F8493供应商](#)

**NOTES:**

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## APPENDIX A: REVISION HISTORY

### Revision A (September 2007)

Original data sheet for the PIC18F6393/6493/8393/8493 devices.

### Revision B (October 2009)

Removed "Preliminary" marking.

### Revision C (August 2010)

Changes and additions were made to the "Power-Managed Modes", "Flexible Oscillator Structure", "Peripheral Highlights" and "Special Microcontroller Features" sections. Changes were made to Figure 1-1, Figure 1-2, Table 1-2 and Table 1-3, including edits to the

legends of those tables. New text has replaced all in 2.4 "Operation in Power-Managed Modes". Corrections have been made to 4.0 "Electrical Characteristics". The extended temperature has been removed from the "Product Identification System" information. New packaging diagrams were added because the diagrams referenced in the document, "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629), have not been updated. Minor typographical edits throughout the document.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Number of Pixels the LCD Driver Can Drive	128 (4 x 32)	128 (4 x 32)	192 (4 x 48)	192 (4 x 48)
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Flash Program Memory	8 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

# PIC18F6393/6493/8393/8493

---

[查询PIC18F8493供应商](#)

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**

[查询PIC18F8493供应商](#)

## **APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES**

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, “*Migrating Designs from PIC16C74A/74B to PIC18C442*”. The changes discussed, while device-specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

## **APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES**

A detailed discussion of the migration pathway, and differences between the high-end MCU devices (i.e., PIC17CXXX), and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, “*PIC17CXXX to PIC18CXXX Migration*”. This Application Note is available as Literature Number DS00726.

# PIC18F6393/6493/8393/8493

---

[查询PIC18F8493供应商](#)

**NOTES:**



# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## INDEX

### A

A/D	31
A/D Converter Interrupt, Configuring	35
Acquisition Requirements	36
ADCON0 Register	31
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31, 34
ADRESL Register	31
Analog Port Pins, Configuring	38
Associated Registers	40
Configuring the Module	35
Conversion Clock (TAD)	37
Conversion Requirements	46
Conversion Status (GO/DONE Bit)	34
Conversions	39
Converter Characteristics	45
Discharge	39
Operation in Power-Managed Modes	38
Selecting and Configuring Acquisition Time	37
Special Event Trigger (ECCP2)	40
Transfer Function	35
Use of the ECCP2 Trigger	40
Absolute Maximum Ratings	43
ADCON0 Register	31
GO/DONE Bit	34
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31
ADRESL Register	31, 34
Analog-to-Digital Converter. See A/D.	

### B

Block Diagrams	
A/D	34
Analog Input Model	35
PIC18F6X93 (64-Pin)	11
PIC18F8X93 (80-Pin)	12

### C

Compare (ECCP2 Module)	
Special Event Trigger	40
Conversion Considerations	54
Customer Change Notification Service	59
Customer Notification Service	59
Customer Support	59

### D

Device Differences	53
Device ID Registers	41
Device Overview	9
Details of Individual Devices	9
Features (table)	10
Special Features	9
Documentation	
Most Current Versions	7
Related Data Sheet	9

### E

Electrical Characteristics	43
A/D Converter	45
Absolute Maximum Ratings	43
Low-Power Voltage-Frequency Graph	44
Voltage-Frequency Graph	44
Equations	
A/D Acquisition Time	36
A/D Minimum Charging Time	36
Calculating the Minimum Required Acquisition Time	36
Errata	7

### I

Internet Address	59
Interrupt Sources	
A/D Conversion Complete	35

### L

LCD Driver	
Features	3

### M

Microchip Internet Web Site	59
Microcontroller	
Special Features	3
Migration from Baseline to Enhanced Devices	54
Migration from High-End to Enhanced Devices	55
Migration from Mid-Range to Enhanced Devices	55

### O

Oscillator Structure	
Features	3

### P

Packaging	
Information	47
Marking	47
Peripheral Highlights	3
Pin Diagrams	
64-Pin TQFP	4
80-Pin TQFP	5
Pin Functions	
AVDD	30
AVDD	20
AVss	20
AVss	30
COM0	18, 26
LCDBIAS1	18, 26
LCDBIAS2	18, 26
LCDBIAS3	18, 26
MCLR/VPP/RG5	13, 21
OSC1/CLKI/RA7	13, 21
OSC2/CLKO/RA6	13, 21
RA0/AN0	14, 22
RA1/AN1	14, 22
RA2/AN2/VREF-/SEG16	14, 22

# PIC18F6393/6493/8393/8493

## [查询PIC18F8493供应商](#)

RA3/AN3/VREF+/SEG17 .....	14, 22	RH2/SEG45 .....	29
RA4/T0CKI/SEG14 .....	14, 22	RH3/SEG44 .....	29
RA5/AN4/HLVDIN/SEG15 .....	14, 22	RH4/SEG40 .....	29
RB0/INT0 .....	15, 23	RH5/SEG41 .....	29
RB1/INT1/SEG8 .....	15, 23	RH6/SEG42 .....	29
RB2/INT2/SEG9 .....	15, 23	RH7/SEG43 .....	29
RB3/INT3/SEG10 .....	15, 23	RJ0/SEG32 .....	30
RB4/KBI0/SEG11 .....	15, 23	RJ1/SEG33 .....	30
RB5/KBI1 .....	15, 23	RJ2/SEG34 .....	30
RB6/KBI2/PGC .....	15, 23	RJ3/SEG35 .....	30
RB7/KBI3/PGD .....	15, 23	RJ4/SEG39 .....	30
RC0/T1OSO/T13CKI .....	16, 24	RJ5/SEG38 .....	30
RC1/T1OSI/CCP2 .....	16, 24	RJ6/SEG37 .....	30
RC2/CCP1/SEG13 .....	16, 24	RJ7/SEG36 .....	30
RC3/SCK/SCL .....	16, 24	VDD .....	30
RC4/SDI/SDA .....	16, 24	VDD .....	20
RC5/SDO/SEG12 .....	16, 24	Vss .....	30
RC6/TX1/CK1 .....	16, 24	Vss .....	20
RC7/RX1/DT1 .....	16, 24	Pinout I/O Descriptions	
RD0/SEG0 .....	17, 25	PIC18F6X93 .....	13
RD0/SEG1 .....	17	PIC18F8X93 .....	21
RD1/SEG1 .....	25	Power-Managed Modes	
RD2/SEG2 .....	17, 25	and A/D Operation .....	38
RD3/SEG3 .....	17, 25	Features .....	3
RD4/SEG4 .....	17, 25	Product Identification System .....	61
RD5/SEG5 .....	17, 25	<b>R</b>	
RD6/SEG6 .....	17, 25	Reader Response .....	60
RD7/SEG7 .....	17, 25	Registers	
RE4/COM1 .....	18, 26	ADCON0 (A/D Control 0) .....	31
RE5/COM2 .....	18, 26	ADCON1 (A/D Control 1) .....	32
RE6/COM3 .....	18, 26	ADCON2 (A/D Control 2) .....	33
RE7/CCP2/SEG31 .....	18, 26	DEVID1 (Device ID 1) .....	42
RF0/AN5/SEG18 .....	19, 27	DEVID2 (Device ID 2) .....	42
RF1/AN6/C2OUT/SEG19 .....	19, 27	Revision History .....	53
RF2/AN7/C1OUT/SEG20 .....	19, 27	<b>S</b>	
RF3/AN8/SEG21 .....	19, 27	Special Features of the CPU .....	41
RF4/AN9/SEG22 .....	19, 27	Device ID Registers .....	41
RF5/AN10/CVREF/SEG23 .....	19, 27	<b>T</b>	
RF6/AN11/SEG24 .....	19, 27	Timing Diagrams	
RF7/SS/SEG25 .....	19, 27	A/D Conversion .....	46
RG0/SEG30 .....	20, 28	<b>W</b>	
RG1/TX2/CK2/SEG29 .....	20, 28	WWW Address .....	59
RG2/RX2/DT2/SEG28 .....	20, 28	WWW, On-Line Support .....	7
RG3/SEG27 .....	20, 28		
RG4/SEG26 .....	20, 28		
RG5 .....	20, 28		
RH0/SEG47 .....	29		
RH1/SEG46 .....	29		

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com), click on Customer Change Notification and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: <http://support.microchip.com>**

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager  
RE: Reader Response  
Total Pages Sent \_\_\_\_\_

From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: PIC18F6393/6493/8393/8493 Literature Number: DS39896C

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

# PIC18F6393/6493/8393/8493

[查询PIC18F8493供应商](#)

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device <sup>(1), (2)</sup>	PIC18F6393, PIC18F6493, PIC18F8393, PIC18F8493 – V <sub>DD</sub> range: 4.2V to 5.5V PIC18LF6393, PIC18LF6493, PIC18LF8393, PIC18LF8493 – V <sub>DD</sub> range: 2.0V to 5.5V		
Temperature Range	I	= -40°C to +85°C (Industrial)	
Package	PT	= TQFP (Thin Quad Flatpack)	
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18LF6393-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301.
- b) PIC18LF6393-I/PT = Industrial temp., TQFP package, Extended VDD limits.

**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range

**2:** T = in Tape and Reel TQFP packages only.

## WORLDWIDE SALES AND SERVICE

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

**Kokomo**  
Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**Santa Clara**  
Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

**Toronto**  
Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hong Kong SAR**  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

**Japan - Yokohama**  
Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-6578-300  
Fax: 886-3-6578-370

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830  
Fax: 886-7-330-9305

**Taiwan - Taipei**  
Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820