

### Microprocessor Supervisory Circuit with Mannual Reset

NO.EA-170-100127

### OUTLINE

The R5107G Series are CMOS-based microprocessor supervisory circuit, or high accuracy and ultra low supply current voltage detector with built-in delay circuit and watchdog timer. When the supply voltage is down across the threshold, or the watchdog timer does not detect the system clock from the microprocessor, the reset output is generated.

The voltage detector circuit is used for the system reset, etc. The detector threshold is fixed internally, and the accuracy is  $\pm 1.0\%$ . The released delay time (Power-on Reset Delay) circuit is built-in, and output delay time is adjustable with an external capacitor, and the accuracy is  $\pm 16\%^*$ . When the supply voltage becomes the released voltage, the reset state will be maintained during the delay time. The output type of the reset is selectable, Nch open-drain, or CMOS.

The time out period of the watchdog timer can be also set with an external capacitor, and the accuracy is  $\pm 33\%^*$ .

The function to stop supervising clock by the watchdog timer (INH function) and manual reset function are built in this IC.

There are another 4 products by the difference of packages and the function of voltage detector and watchdog timer. The package of R5107G is SSOP-8G.

### FEATURES

- Supply Current..... Typ. 11 $\mu$ A
- Operating Voltage Range ..... 0.9V to 6.0V

#### < Voltage Detector Part >

- Detector Threshold Range..... 1.5V to 5.5V (0.1V steps)
- Detector Threshold Accuracy.....  $\pm 1.0\%$
- Power-on Reset Delay Time accuracy .....  $\pm 16\%^*$  ( $-40^{\circ}\text{C} \leq T_{\text{opt}} \leq 105^{\circ}\text{C}$ )
- Power-on reset delay time of the voltage detector ..... Typ. 370ms with an external capacitor : 0.1 $\mu$ F
- With Mannual Reset pin (MR) ..... Able to reset voltage detector and watchdog timer

#### < Watchdog Timer Part >

- Built-in a watchdog timer's time out period accuracy .....  $\pm 33\%^*$  ( $-40^{\circ}\text{C} \leq T_{\text{opt}} \leq 105^{\circ}\text{C}$ )
- Timeout period for watchdog timer ..... Typ. 310ms with an external capacitor : 0.1 $\mu$ F
- Reset timer for watchdog timer..... Typ. 34ms with an external capacitor : 0.1 $\mu$ F
- With Inhibit pin (INH)..... Able to stop watchdog timer
- Package ..... SSOP-8G

\*) Accuracy to center value of (Min.+Max.)/2

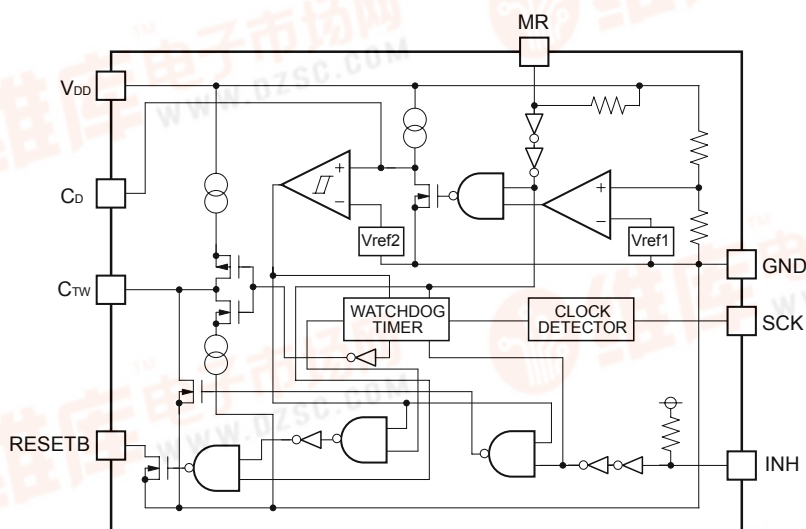
### APPLICATIONS

- Supervisory circuit for equipment with using microprocessors.

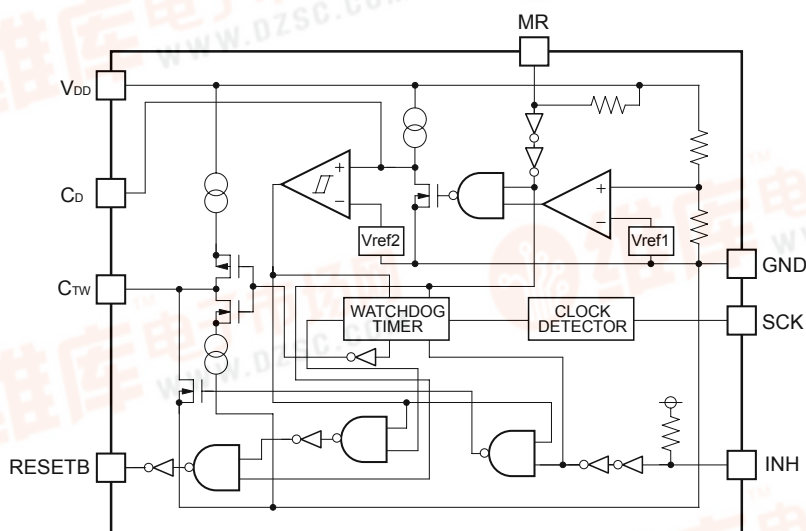


## BLOCK DIAGRAMS

**Nch Open Drain Output (R5107Gxx1A)**



**CMOS Output (R5107Gxx1C)**



## SELECTION GUIDE

The detector threshold, the output type and the taping type for the ICs can be selected at the users' request. The selection can be made with designating the part number as shown below;

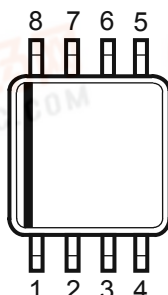
| Product Name                                                                                       | Package | Quantity per Reel | Pb Free | Halogen Free |
|----------------------------------------------------------------------------------------------------|---------|-------------------|---------|--------------|
| R5107Gxx1*-TR-FE                                                                                   | SSOP-8G | 3,000 pcs         | Yes     | Yes          |
| xx: The detector threshold can be designated in the range from 1.5V(15) to 5.5V(55) in 0.1V steps. |         |                   |         |              |
| * : Designation of Output Type<br>(A) Nch Open Drain<br>(C) CMOS                                   |         |                   |         |              |

## SERIES SELECTION

|                            | R5105N   | R5106N                                                        | R5107G  | R5108G                               | R5109G                |
|----------------------------|----------|---------------------------------------------------------------|---------|--------------------------------------|-----------------------|
| Package                    | SOT-23-6 |                                                               | SSOP-8G |                                      |                       |
| With INH pin (Inhibit)     | No       | Yes                                                           |         |                                      |                       |
| 2 clock input              | No       |                                                               |         |                                      | Yes                   |
| With MR pin (Manual Reset) | No       |                                                               | Yes     | No                                   |                       |
| With SENSE pin             | No       |                                                               |         | Yes                                  | No                    |
| Remarks                    |          | C <sub>D</sub> pin and C <sub>TW</sub> pin are combined uses. |         | Operating Voltage Range 1.5V to 6.0V | Supply Current 11.5μA |

## PIN CONFIGURATION

● SSOP-8G



## PIN DESCRIPTIONS

| Pin No. | Symbol          | Description                                                                                                                                |
|---------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | RESETB          | Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output "L" at detecting Detector Threshold and Watchdog Timer Reset.) |
| 2       | MR              | Manual Reset Pin (Active"L")                                                                                                               |
| 3       | C <sub>D</sub>  | External Capacitor Pin for Setting Delay Time of Voltage Detector                                                                          |
| 4       | GND             | Ground Pin                                                                                                                                 |
| 5       | SCK             | Clock Input Pin from Microprocessor                                                                                                        |
| 6       | INH             | Inhibit Pin ("L": Inhibit the watchdog timer)                                                                                              |
| 7       | C <sub>TW</sub> | External Capacitor Pin for Setting Reset and Watchdog Timeout Periods                                                                      |
| 8       | V <sub>DD</sub> | Power supply Pin                                                                                                                           |

## ABSOLUTE MAXIMUM RATINGS

T<sub>opt</sub>=25°C

| Symbol              | Item                         |                                | Rating                        | Unit |
|---------------------|------------------------------|--------------------------------|-------------------------------|------|
| V <sub>DD</sub>     | Supply Voltage               |                                | −0.3 to 7.0                   | V    |
| V <sub>CD</sub>     | Output Voltage               | Voltage of C <sub>D</sub> Pin  | −0.3 to V <sub>DD</sub> + 0.3 | V    |
| V <sub>CTW</sub>    |                              | Voltage of C <sub>TW</sub> Pin | −0.3 to V <sub>DD</sub> + 0.3 | V    |
| V <sub>RESETB</sub> |                              | Voltage of RESETB Pin          | −0.3 to 7.0                   | V    |
| V <sub>SCK</sub>    | Input Voltage                | Voltage of SCK Pin             | −0.3 to 7.0                   | V    |
| V <sub>INH</sub>    |                              | Voltage of INH Pin             | −0.3 to 7.0                   | V    |
| V <sub>MR</sub>     |                              | Voltage of MR Pin              | −0.3 to 7.0                   | V    |
| I <sub>RESETB</sub> | Output Current               | Current of RESETB Pin          | 20                            | mA   |
| P <sub>d</sub>      | Power Dissipation (SSOP-8G)* |                                | 380                           | mW   |
| T <sub>opt</sub>    | Operating Temperature Range  |                                | −40 to 105                    | °C   |
| T <sub>stg</sub>    | Storage Temperature Range    |                                | −55 to 125                    | °C   |

\* ) For Power Dissipation, please refer to PACKAGE INFORMATION.

## ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.

The functional operation at or over these absolute maximum ratings is not assured.

## ELECTRICAL CHARACTERISTICS

$V_{DD}=6.0V$ ,  $C_{TW}=0.1\mu F$ ,  $C_D=0.1\mu F$ , In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of  $100k\Omega$  (R5107Gxx1A), unless otherwise noted.

The specification in ☐ is checked and guaranteed by design engineering at  $-40^{\circ}C \leq T_{opt} \leq 105^{\circ}C$ .

### • R5107Gxx1A/C

$T_{opt}=25^{\circ}C$

| Symbol   | Item              | Conditions                                        | Min. | Typ. | Max. | Unit    |
|----------|-------------------|---------------------------------------------------|------|------|------|---------|
| $V_{DD}$ | Operating Voltage |                                                   | 0.9  |      | 6.0  | V       |
| $I_{SS}$ | Supply Current    | $V_{DD} = -V_{DET} + 0.5V$ ,<br>Clock pulse input |      | 11   | 15   | $\mu A$ |

### • VD Part

| Symbol                           | Item                                       | Conditions                                    | Min.                        | Typ.                        | Max.                        | Unit             |
|----------------------------------|--------------------------------------------|-----------------------------------------------|-----------------------------|-----------------------------|-----------------------------|------------------|
| $-V_{DET}$                       | Detector Threshold                         | $T_{opt}=25^{\circ}C$                         | $\times 0.990$              |                             | $\times 1.010$              | V                |
|                                  |                                            | $-40^{\circ}C \leq T_{opt} \leq 105^{\circ}C$ | $\times 0.972$              |                             | $\times 1.015$              |                  |
| $V_{HYS}$                        | Detector Threshold Hysteresis              |                                               | $-V_{DET}$<br>$\times 0.03$ | $-V_{DET}$<br>$\times 0.05$ | $-V_{DET}$<br>$\times 0.07$ | V                |
| $\Delta -V_{DET}/\Delta T_{opt}$ | Detector Threshold Temperature Coefficient | $-40^{\circ}C \leq T_{opt} \leq 105^{\circ}C$ |                             | $\pm 100$                   |                             | ppm/ $^{\circ}C$ |
| $t_{PLH}$                        | Output Delay Time                          | $C_D=0.1\mu F$ *1                             | 340                         | 370                         | 467                         | ms               |
| $I_{RESETB}$                     | Output Current (RESETB Output pin)         | Nch<br>$V_{DD}=1.2V$<br>$V_{DS}=0.1V$         | 0.38                        | 0.8                         |                             | mA               |
|                                  |                                            | Pch *2<br>$V_{DD}=6.0V$<br>$V_{DS}=0.5V$      | 0.65                        | 0.9                         |                             | mA               |
| $V_{MRH}$                        | MR Input "H" *3                            |                                               | 1.0                         |                             | 6.0                         | V                |
| $V_{MRL}$                        | MR Input "L"                               |                                               | 0                           |                             | 0.35                        | V                |
| $t_{MRW}$                        | MR Input Pulse Width *4                    |                                               | 3                           |                             |                             | $\mu s$          |
| $R_{MR}$                         | MR Pull-up Resistance                      |                                               | 60                          | 110                         | 164                         | $k\Omega$        |

### • WDT Part

| Symbol      | Item                    | Conditions                                                   | Min.                | Typ. | Max.                | Unit      |
|-------------|-------------------------|--------------------------------------------------------------|---------------------|------|---------------------|-----------|
| $t_{WD}$    | Watchdog Timeout period | $C_{TW}=0.1\mu F$ *1                                         | 230                 | 310  | 450                 | ms        |
| $t_{WR}$    | Reset Hold Time of WDT  | $C_{TW}=0.1\mu F$ *1                                         | 29                  | 34   | 48                  | ms        |
| $V_{SCKH}$  | SCK Input "H"           |                                                              | $V_{DD} \times 0.8$ |      | 6.0                 | V         |
| $V_{SCKL}$  | SCK Input "L"           |                                                              | 0                   |      | $V_{DD} \times 0.2$ | V         |
| $V_{INH H}$ | INH Input "H"           |                                                              | 1.0                 |      | 6.0                 | V         |
| $V_{INH L}$ | INH Input "L"           |                                                              | 0                   |      | 0.35                | V         |
| $R_{INH}$   | INH pull-up Resistance  |                                                              | 64                  | 110  | 152                 | $k\Omega$ |
| $t_{SCKW}$  | SCK Input Pulse Width   | $V_{SCKL}=V_{DD} \times 0.2$<br>$V_{SCKH}=V_{DD} \times 0.8$ | 500                 |      |                     | ns        |

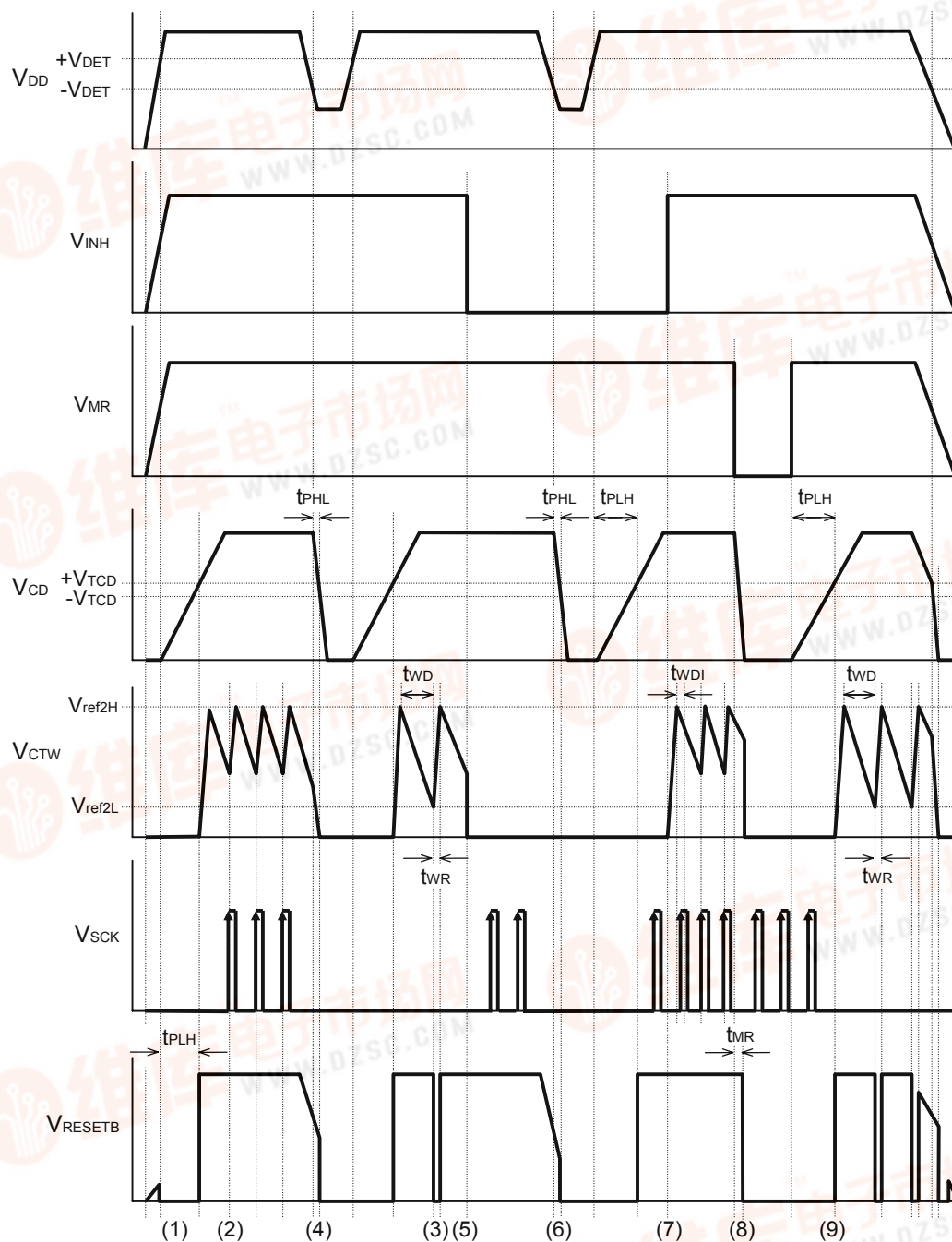
All of unit are tested and specified under load conditions such that  $T_{opt}=25^{\circ}\text{C}$  except for Detector Threshold Temperature Coefficient and MR Input Pulse Width.

- \*1) The specification does not contain the temperature characteristics of the external capacitor.
- \*2) In case of CMOS type (R5107Gxx1C)
- \*3) In case of Nch open drain type (R5107Gxx1A)
- \*4) MR input pulse width specification guarantee the minimum input pulse width of MR pin for output "L" from RESETB pin. If the "L" pulse width of MR is short,  $t_{PLH}$  may be short. Refer to the timing diagram for details.

**RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)**

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge.  
And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## TIMING CHART



\*)  $V_{TCD}$  : Threshold voltage of C<sub>D</sub> pin when a power-on reset pulse inverting.

\*)  $V_{ref2H}$  : C<sub>TW</sub> pin voltage at the end of WDT timeout period.

\*)  $V_{ref2L}$  : C<sub>TW</sub> pin voltage at the begin of WDT timeout period.

## OPERATION

- (1) When the power supply,  $V_{DD}$  pin voltage becomes more than the released voltage ( $+V_{DET}$ ), after the released delay time (or the power on reset time  $t_{PLH}$ ), the output of RESETB becomes "H" level.
- (2) When the SCK pulse is input, the watchdog timer is cleared, and  $C_{TW}$  pin mode changes from the discharge mode to the charge mode. When the  $C_{TW}$  pin voltage becomes higher than  $V_{ref2H}$ , the mode will change into the discharge mode, and next watchdog time count starts.
- (3) Unless the SCK pulse is input, WDT will not be cleared, and during the charging period of  $C_{TW}$  pin, RESETB="L".
- (4) When the  $V_{DD}$  pin becomes lower than the detector threshold voltage ( $-V_{DET}$ ), RESETB outputs "L" after the  $t_{PHL}$ .
- (5) If "L" signal is input to the INH pin, the RESETB outputs "H", regardless the SCK clock state.
- (6) During the "L" period of INH pin, the voltage detector monitors the supply voltage.
- (7) When the signal to the INH pin is set from "L" to "H", the watchdog starts supervising the system clock, or charge cycle to the  $C_{TW}$  pin starts, the capacitor connected to the  $C_{TW}$  pin is charged with the current of setting Reset time of WDT.
- (8) If "L" signal is input to the MR pin, the RESETB outputs "L" after the  $t_{MR}$ , regardless the SCK clock state and  $V_{DD}$  voltage.
- (9) When the signal to the MR pin is set from "L" to "H", the RESETB outputs "H" after the  $t_{PLH}$ , the watchdog starts supervising the system clock.

### • Watchdog Timeout period/Reset hold time

The watchdog timeout period and reset hold time can be set with an external capacitor to  $C_{TW}$  pin.

The next equations describe the relation between the watchdog timeout period and the external capacitor value, or the reset hold time and the external capacitor value.

$$t_{WD}(s) = 3.1 \times 10^6 \times C(F)$$

$$t_{WR}(s) = t_{WD}/9$$

The watchdog timer (WDT) timeout period is determined with the discharge time of the external capacitor.

During the watchdog timeout period, if the clock pulse from the system is detected, WDT is cleared and the capacitor is charged. When the charge of the capacitor completes, another watchdog timeout period starts again. During the watchdog timeout period, if the clock pulse from the system is not detected, during the next reset hold time RESETB pin outputs "L".

During the reset time, (while charging the external capacitor) and after starting the watchdog timeout period, (just after from the discharge of the external capacitor) even if the clock pulse is input during the time period " $t_{WDI}$ ", the clock pulse is ignored.

$$t_{WDI}(s) = t_{WD}/10$$

### • Released Delay Time (Power-on Reset delay time)

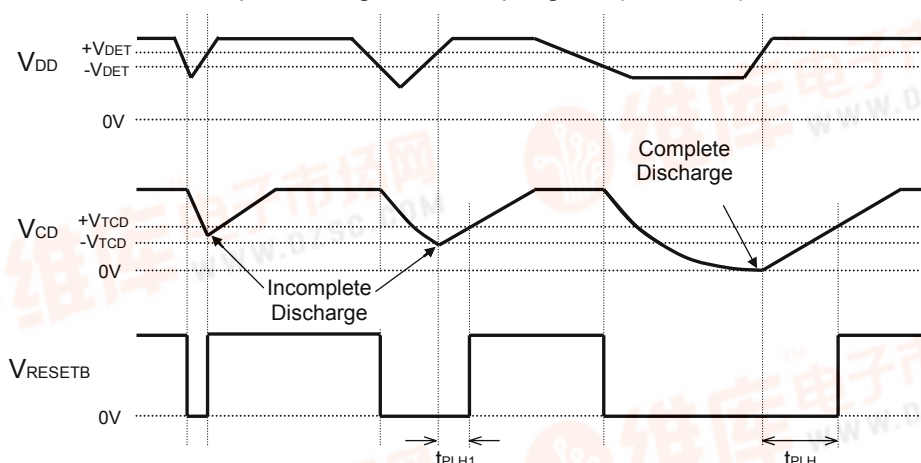
The released delay time can be set with an external capacitor connected to the  $C_D$  pin. The next equation describes the relation between the capacitance value and the released delay time ( $t_{PLH}$ ).

$$t_{PLH} (s) = 3.7 \times 10^6 \times C (F)$$

The capacitor connected to  $C_D$  pin determines  $t_{WD}$ ,  $t_{WR}$ , and  $t_{PLH}$ .

When the  $V_{DD}$  voltage becomes equal or less than  $(-V_{DET})$ , discharge of the capacitor connected to the  $C_D$  pin starts. Therefore, if the discharge is not enough and  $V_{DD}$  voltage returns to  $(+V_{DET})$  or more, thereafter the delay time will be shorter than  $t_{PLH}$  which is expected.

Power on Reset Operation against the input glitch ( $t_{PLH1} < t_{PLH}$ )



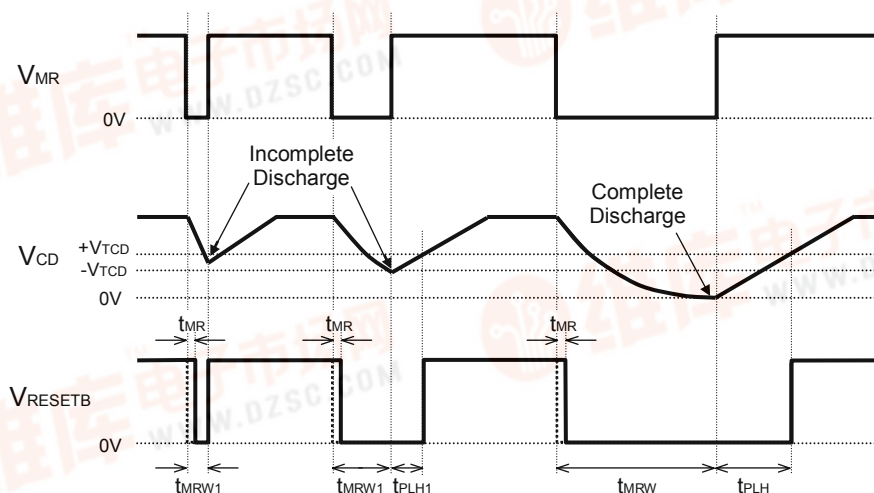
### • Minimum Operating Voltage

We specified the minimum operating voltage as the minimum input voltage in which the condition of RESETB pin being  $0.1V$  or lower than  $0.1V$ . (Herein, pull-up resistance is set as  $100k\Omega$  in the case of the Nch open-drain output type.)

### • Manual Reset (MR) Function

By setting MR pin as "L", the output of RESETB can be forced to set "L". After pull-down the MR pin to "L", the delay time ( $t_{MR}$ ) to the output "L" from RESETB is  $1\mu s$  as maximum. MR pin is pulled-up via the built-in resistor. (Typ.  $110k\Omega$ ). If MR pin voltage  $> V_{DD}$  voltage, a current flows into MR pin. However, the current value is limit by the pull-up resistor, therefore there is not bad impact on the operation. When the "L" signal is input to MR pin, the discharge of  $C_D$  pin capacitor ( $C_D$ ) starts. If the term of "L" for MR pin is short,  $C_D$  will not be discharged enough. As a result, the delay time after setting "H" for MR pin will be shorter than expected. Because of this, confirm the operation under the same conditions as users' applications. For example, in case of  $C_D$  is set at  $0.1\mu F$ , and the condition to maintain the delay time value after MR pin's returning to "H", is described as the minimum "L" term of MR pin, or  $150\mu s$ . When MR input pulse ( $t_{MRW}$ ) is less than  $3.0\mu s$ , output delay time ( $t_{PLH}$ ) might not exist.

Power on Reset Operation with MR pin input ( $t_{PLH1} < t_{PLH}$ ,  $t_{MRW1} < t_{MRW}$ )



### • Inhibit (INH) Function

If INH pin is set at "L", the watchdog timer stops monitoring the clock, and the RESETB output will be dominant by the voltage detector's operation. Therefore, if the supply voltage is set at more than the detector threshold level, RESETB outputs "H" regardless the clock pulse. INH pin is pulled up with a resistor (Typ.  $110k\Omega$ ) internally.

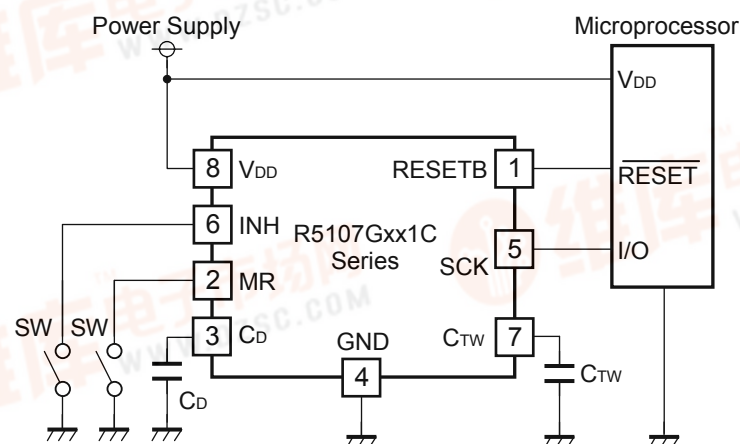
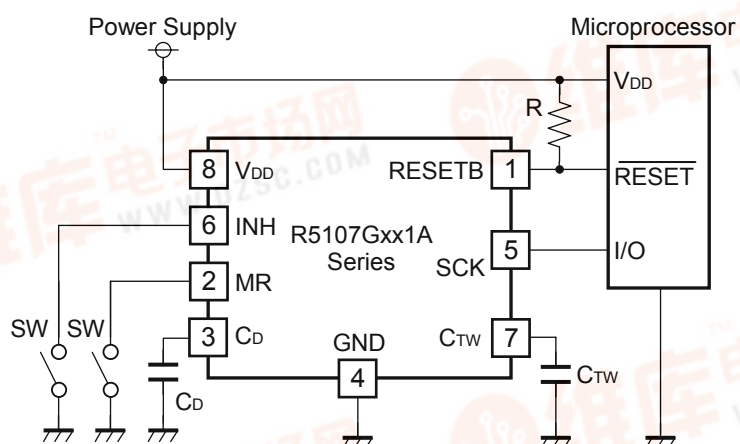
### • RESETB Output

RESETB pin's output type is selectable either the Nch open-drain output or CMOS output. If the Nch open-drain type output is selected, the RESETB pin is pulled up with an external resistor to an appropriate voltage source.

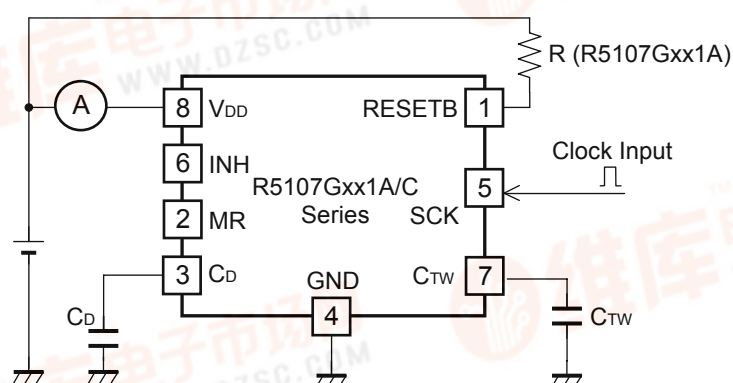
### • Clock Pulse Input

Built-in watchdog timer is cleared with the SCK clock pulse within the watchdog timeout period.

## TYPICAL APPLICATIONS



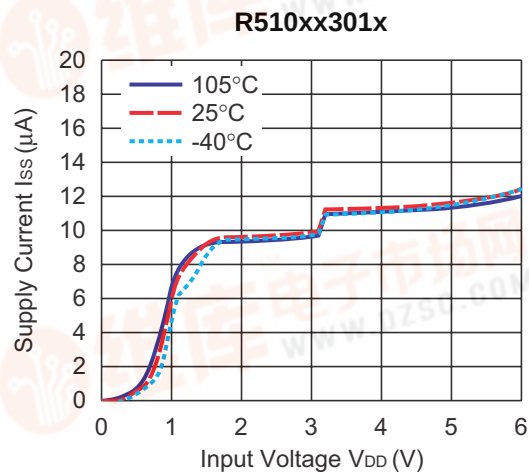
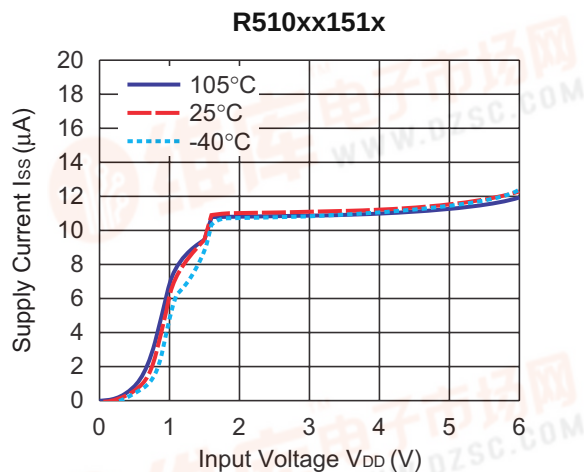
## TEST CIRCUIT



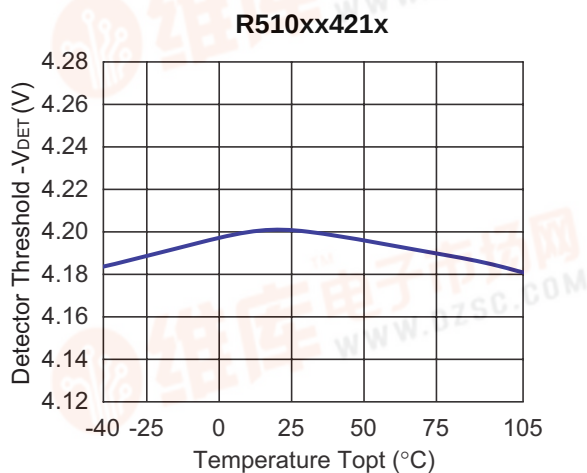
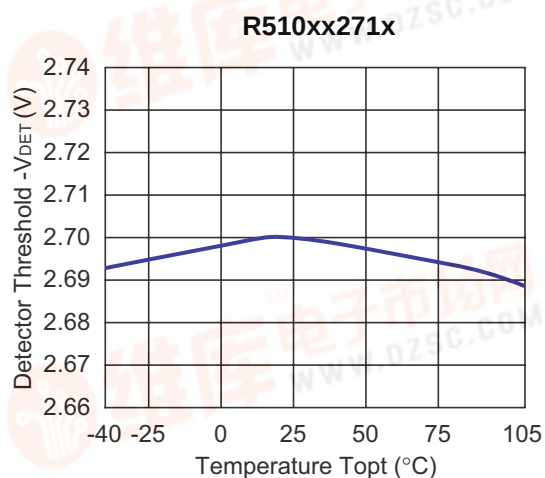
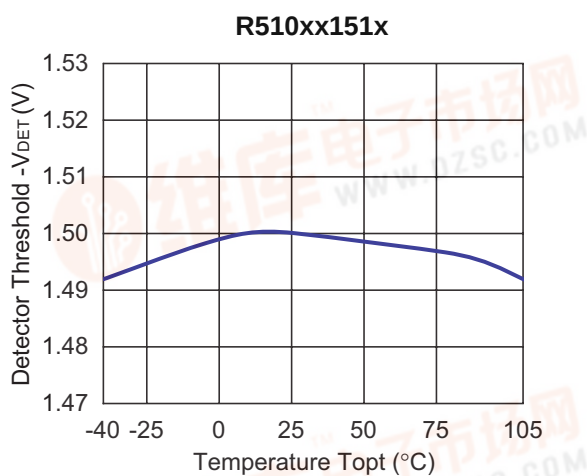
Supply Current Test Circuit

## TYPICAL CHARACTERISTICS

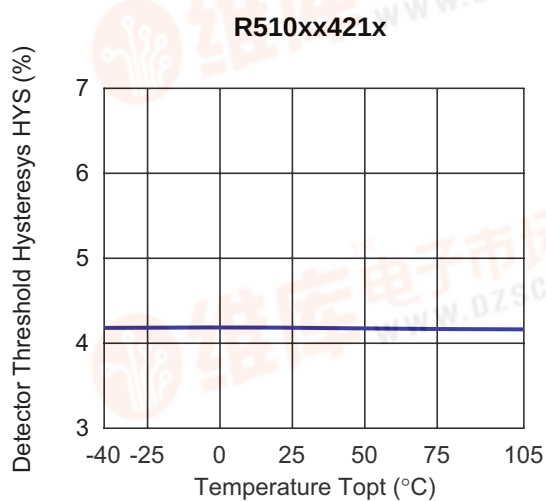
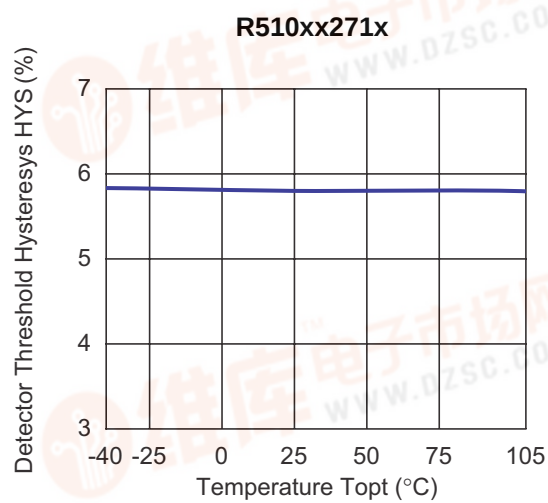
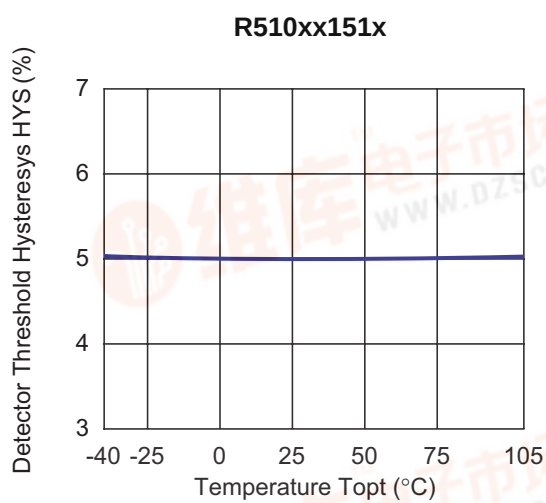
### 1) Supply Current vs. Input Voltage



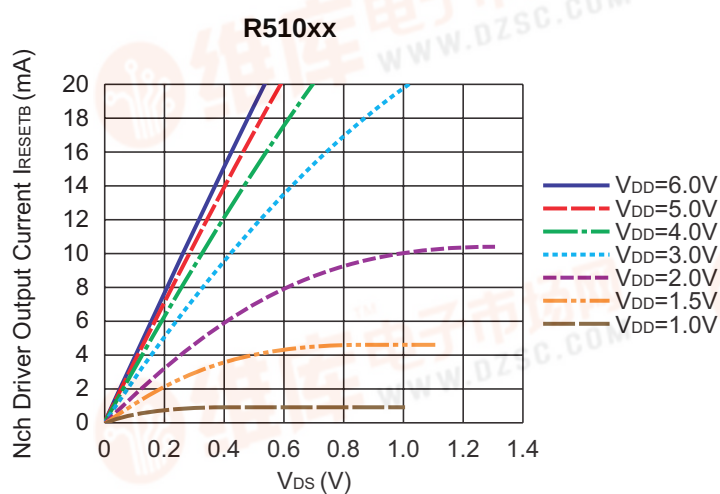
### 2) Detector Threshold vs. Temperature



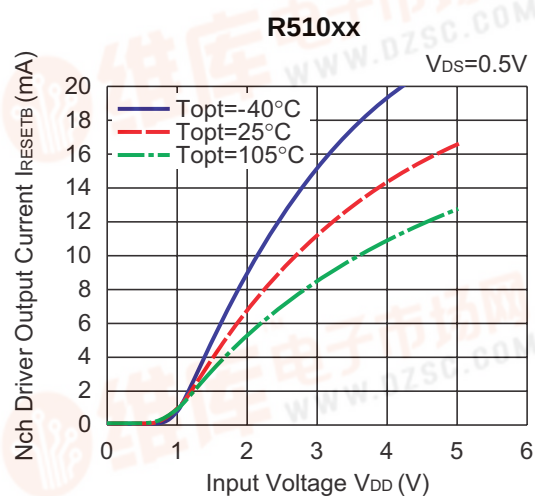
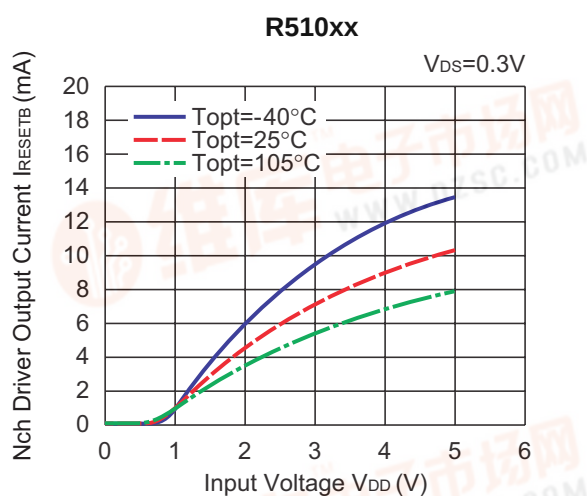
### 3) Detector Threshold Hysteresis vs. Temperature



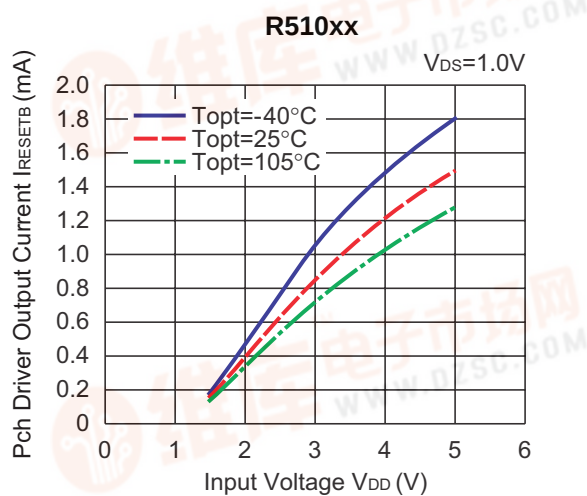
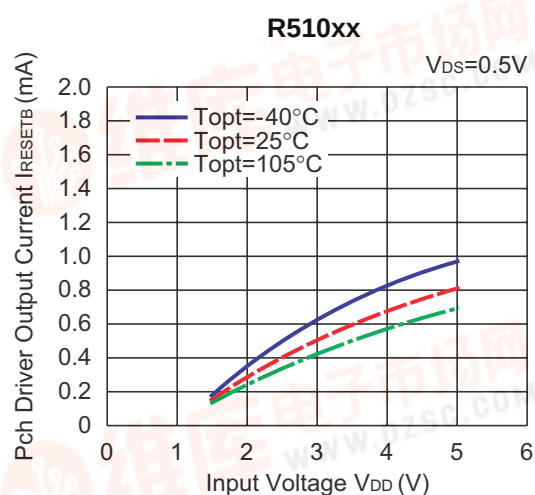
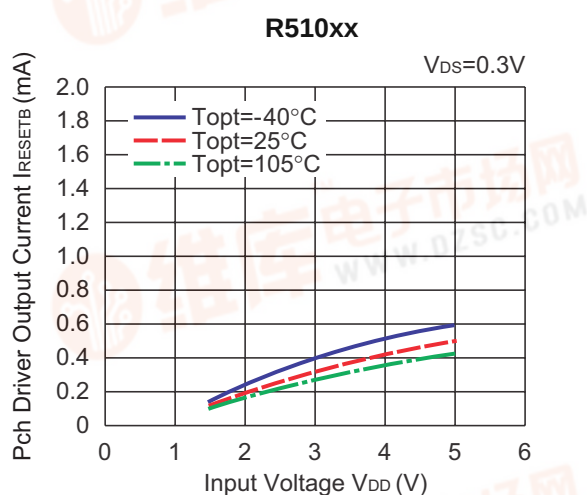
### 4) Nch Driver Output Current vs. Vds



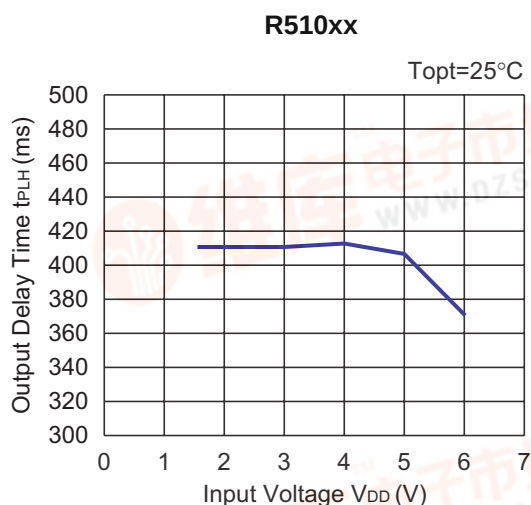
## 5) Nch Driver Output Current vs. Input Voltage



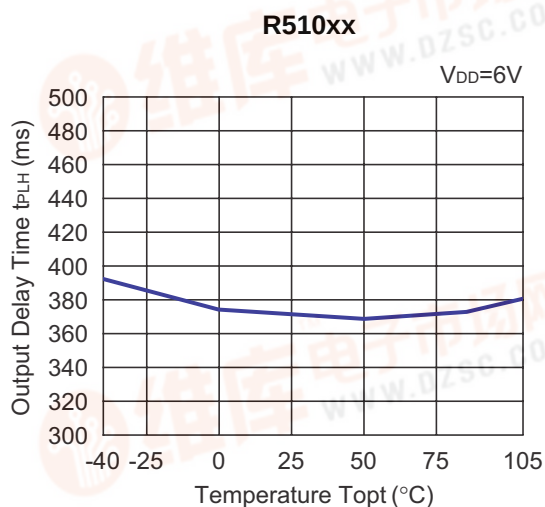
## 6) Pch Driver Output Current vs. Input Voltage



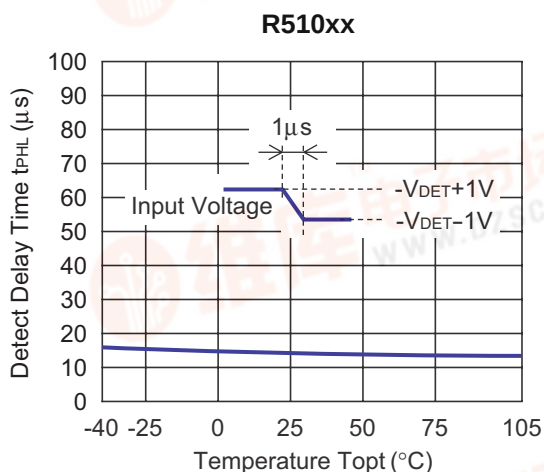
7) Released Delay Time vs. Input Voltage



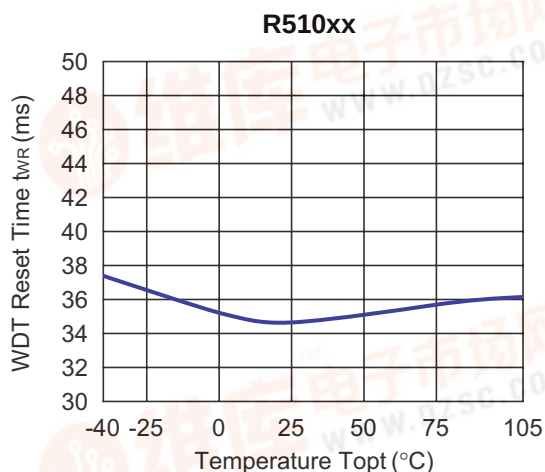
8) Released Delay Time vs. Temperature



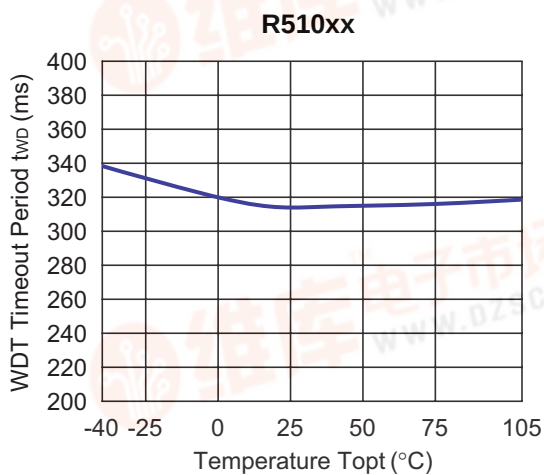
9) Detector Output Delay Time vs. Temperature



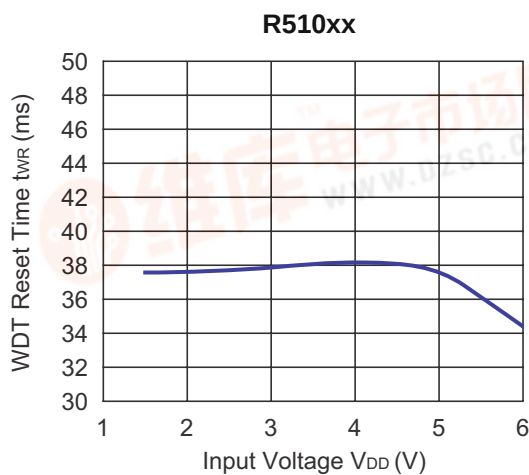
10) WDT Reset Timer vs. Temperature



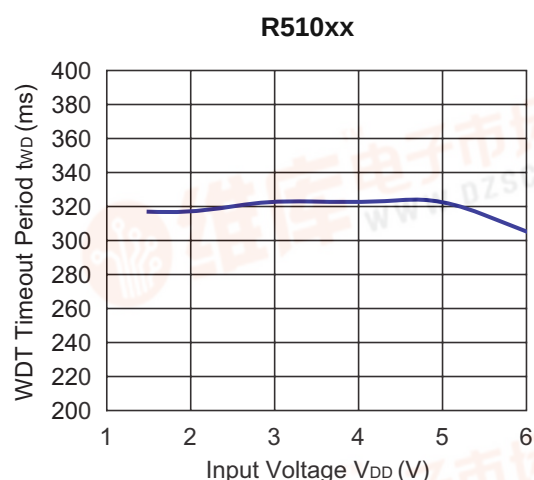
11) WDT Timeout Period vs. Temperature



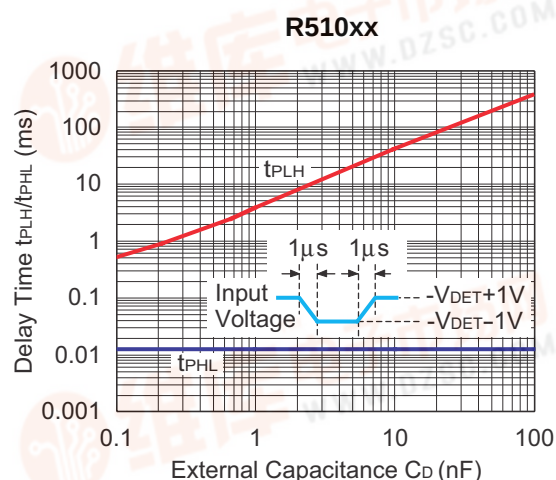
12) WDT Reset Timer vs. Input Voltage



### 13) WDT Timeout Period vs. Input Voltage



### 14) Output Delay Time vs. External Capacitance



## TECHNICAL NOTES

When R510xxx1A (Nch Open Drain Output Type) is used in Figure A or Figure B, if impedance of Voltage Supply pin,  $V_{DD}$  and  $V_{DD}$  of this IC is large, detector threshold level would shift by voltage dropdown caused by the consumption current of the IC itself. Released voltage may also shift and delay time for start-up might be generated by this usage.

When R510xxx1C (CMOS Output Type) is used in Figure A or Figure B, Output level could be unstable by cross conduction current which is generated at detector threshold level or at released voltage level, therefore, do not use this IC with the connection in Figure A or Figure B.

The connection in Figure C may cause the oscillation in both R510xxx1A (Nch Open Drain Output) and R510xxx1C (CMOS Output), therefore do not use R510xx Series with the connection in Figure C.

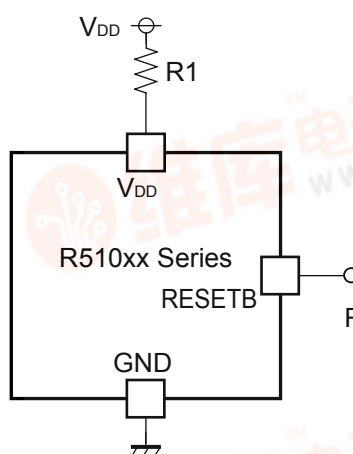


Figure A

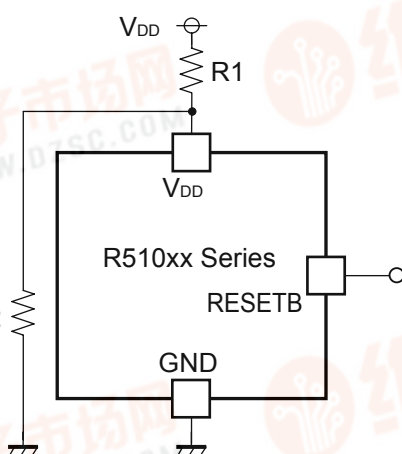


Figure B

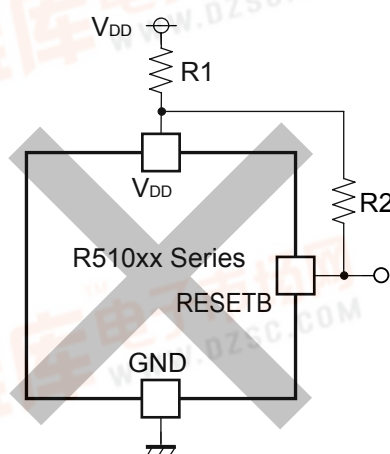


Figure C



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Ricoh completed the organization of the Lead-free production for all of our products. After Apr. 1, 2006, we will ship out the lead free products only. Thus, all products that will be shipped from now on comply with RoHS Directive.

