SIO Input/Output Register Description

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COP400 SERIAL SIO REGISTER

The general operation of the SIO port is treated in the COP400 data sheet. A more detailed look at the internal circuity, as well as software debug, will be presented in this brief.

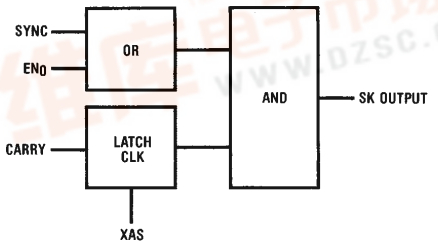
LOGICAL OPERATION

It is important to examine the logical diagram of the SIO and SK circuitry to fully understand the operation of this I/O port. The output at SK is a function of SYNC, EN_0, CARRY, and the XAS instruction.

If CARRY had been set and propagated to the SKL latch by the execution of an XAS instruction, SYNC is enabled to SK and can only be overridden by EN_0. Trouble could arise if the user changes the state of EN_0 without paying close attention to the state of the latch in the SK circuit.

If the latch was set to a logical high and the SIO register enabled as a binary counter, SK is driven high. From this state, if the SIO register is enabled as a serial shift register, SK will output the SYNC pulse immediately, without any intervening XAS instruction.

Logical Diagram of SK Circuit



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SOFTWARE DEBUG OF SERIAL REGISTER FUNCTIONS

In order to understand the method of software debug when dealing with the SIO register, one must first become familiar with the method in which the COPS™ Product Development System (PDS) BREAKPOINT and TRACE operations are carried out. Once these operations are explained, the difficulties which could arise when interrogating the status of the SIO register should become apparent.

SERIAL OUT DURING BREAKPOINT

When the PDS BREAKPOINTs, the COPS user program execution is stopped and execution of a monitor-type program, within the COP device is started. At no time does the COP part "idle". The monitor program loads the development system with the information contained in the COP registers.

Note also that single-step is simply a BREAKPOINT on every instruction.

If the COP chip is BREAKPOINTed while a serial function is in progress, the contents of the SIO register will be destroyed. By the time the monitor program dumps the SIO register to the PDS, the contents of the SIO register will have been written over by clocking in SI. To inspect the SIO register using BREAKPOINT an XAS must be executed prior to BREAKPOINT, therefore the SIO register will be saved in the accumulator.

An even more severe consequence is that the monitor program executes an XAS instruction to get the contents of the SIO register to the PDS. Therefore the SK Latch is dependent on the state of the CARRY prior to the BREAKPOINT. In order to guarantee the integrity of the SIO register one must carefully choose the position of the BREAKPOINT address.

As can be seen, it is impossible to single-step or BREAKPOINT through a serial operation in the SIO register.

SERIAL OUT DURING TRACE

In the TRACE mode, the user's program execution is never stopped. This mode is a real-time description of the program counter and the external event lines, therefore the four external event lines can be used as logic analyzers to monitor the state of any input or output on the COPS device. The external event lines must be tied to the I/O which is to be monitored. The state of these I/O (External Event lines) is displayed along with the TRACE information. The safest way to monitor the real-time state of SO is to use the TRACE function in conjunction with the External Event lines.

BINARY COUNTER DURING BREAKPOINT

Since the COPS chip is executing a Monitor Program during BREAKPOINT the SIO register is still active. In the Binary Counter mode SIO register will decrement on every negative transition of the SI line providing the pulse stays low for

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at least two instruction cycles. However, if the pulse on SI occurs when the monitor is interrogating the SIO register, an erroneous situation may occur.

GENERAL

During a BREAKPOINT operation data is transmitted to the PDS over the SKIP output on the COP402.

Notice that the D register is not contained in the Auto-Print options. The reason for this is that the contents of D cannot be read via COP software. These may be monitored by the External Event lines in the trace mode.

TEMPORARY STORAGE

It is sometimes desirable to temporarily store the value of the accumulator. This can be done by designating a RAM digit and doing an exchange operation. If the user can assure that the SIO register is in the binary counter mode and that SI is at a constant state, the SIO register may be used as a temporary storage location. This is advantageous because the storage and retrieval is accomplished by the single byte XAS instruction and does not require the use of a RAM digit.

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