SONY

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High-speed Buffer Amplifier for CCD Image Sensor

CXA3791EN

Description

The CXA3791EN is a high-speed buffer amplifier IC.
(Applications: CCD image sensor output buffers, Digital still cameras, Camcorders, Other general buffers)

Features

- Power consumption: 22mW (typ.)
  (IDRV = 50μA (180kΩ when V_{CC} = 13V), ISF pin connected to GND, during no signal)
- Push-pull output
- High-speed response: 500V/μs (IDRV = 50μA (180kΩ when V_{CC} = 13V), C_L = 20pF)
- Internal sink current mode for CCD with open source output
  (Settable by external resistance R_{ISF})
- Enables to set the responsibility by changing the drive current by an external resistor

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

(Ta = 25℃)

◆ Supply voltage	V_{CC}	16	V
◆ Supply voltage	IN	GND – 0.3 to V_{CC} + 0.3	V
◆ Storage temperature	Tstg	–65 to +150	℃
◆ Allowable power dissipation	P_D	0.22	W

(when mounted on a two-layer board; 13mm × 13mm, t = 0.63mm)

Recommended Operating Conditions

◆ Supply voltage	V_{CC}	9.0 to 15.5	V
◆ Operating temperature	Ta	–20 to +75	℃

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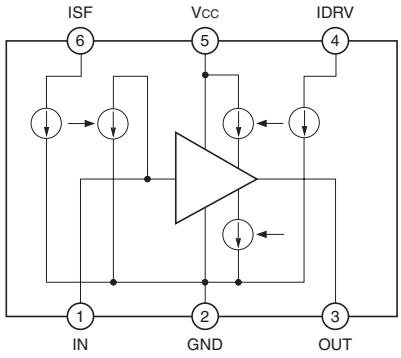
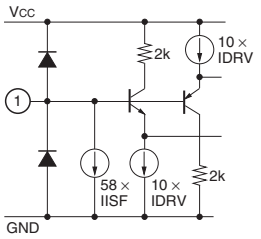
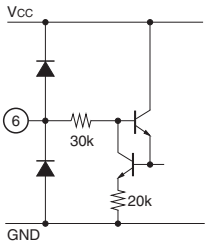
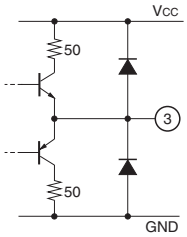
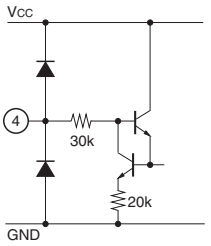
Block Diagram and Pin Configuration

(Top View)



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
2	GND	—	0V	—	GND.
5	Vcc	—	13V	—	Supply voltage input.
1	IN	I	CCD output voltage		Input.
6	ISF	I	—		External resistor connection for setting the sink current for CCD with open source output. Connect an external resistor between this pin and Vcc (Pin 5). Connect this pin to GND (Pin 2) when not using this function. * Set the resistance so that ISF current is 90μA or less.
3	OUT	O	≈IN		Output.
4	IDRV	I	—		External resistor connection for setting the drive current. Connect an external resistor between this pin and Vcc (Pin5). * Set the resistance so that IDRV current is 90μA or less.

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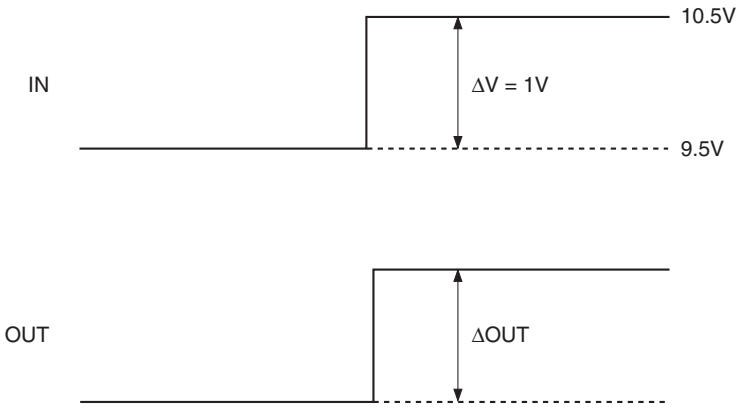
Electrical Characteristics

(Ta = 25°C, V_{CC} = 13V, R_{IDRV} = 180kΩ, ISF pin: connected to GND)

DC Characteristics

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	IN = 10V, R_{IDRV} = 180kΩ	1.4	1.6	1.8	mA
Voltage gain	V_{GAIN}	*1 IN: 10Vdc ΔV = 1V GAIN = ΔOUT/ΔV	—	0.999	—	V/V
I/O offset voltage	V_{OFFSET}	IN = 10V V_{OFFSET} = OUT-IN	–100	—	100	mV
I/O voltage range	V_{RANGE}	R_{IDRV} = 78kΩ R_{IDRV} = 120kΩ R_{IDRV} = 180kΩ R_{IDRV} = 270kΩ	3.3 2.9 2.5 2.1	— — — —	V_{CC} – 2.0 V_{CC} – 1.85 V_{CC} – 1.8 V_{CC} – 1.7	V
Input bias current	I_{BIAS}	IN = 10V, I_{SF} = 0V	–15	–5	6	μA
Sync current	I_{SINK}	IN = 10V, R_{ISF} = 180kΩ	2.6	2.9	3.2	mA

*1 Voltage gain



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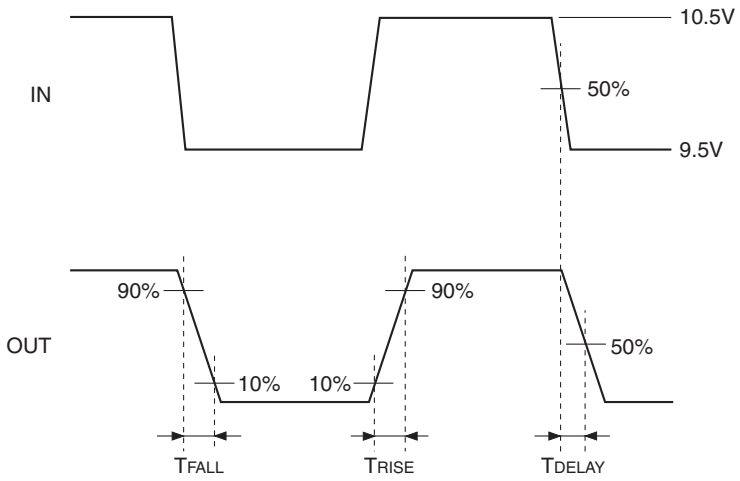
AC Characteristics

(Ta = 25°C, V_{CC} = 13V, IDRV = 50μA (180kΩ when V_{CC} = 13V), ISF pin: connected to GND, R_L = 15Ω, C_L = 20pF)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bandwidth	GBW	IN = 50mVp-p	—	220	—	MHz
Rise time	T_{RISE}	*1 IN = 9.5 to 10.5V 10 to 90%	—	2.5	3.5	ns
Fall time	T_{FALL}	*1 IN = 10.5 to 9.5V 10 to 90%	—	3.0	4.0	ns
I/O delay time	T_{DELAY}	*1 IN = 9.5 to 10.5V @50%	0.9	1.0	2.0	ns

*1 Rise time, fall time and I/O delay time



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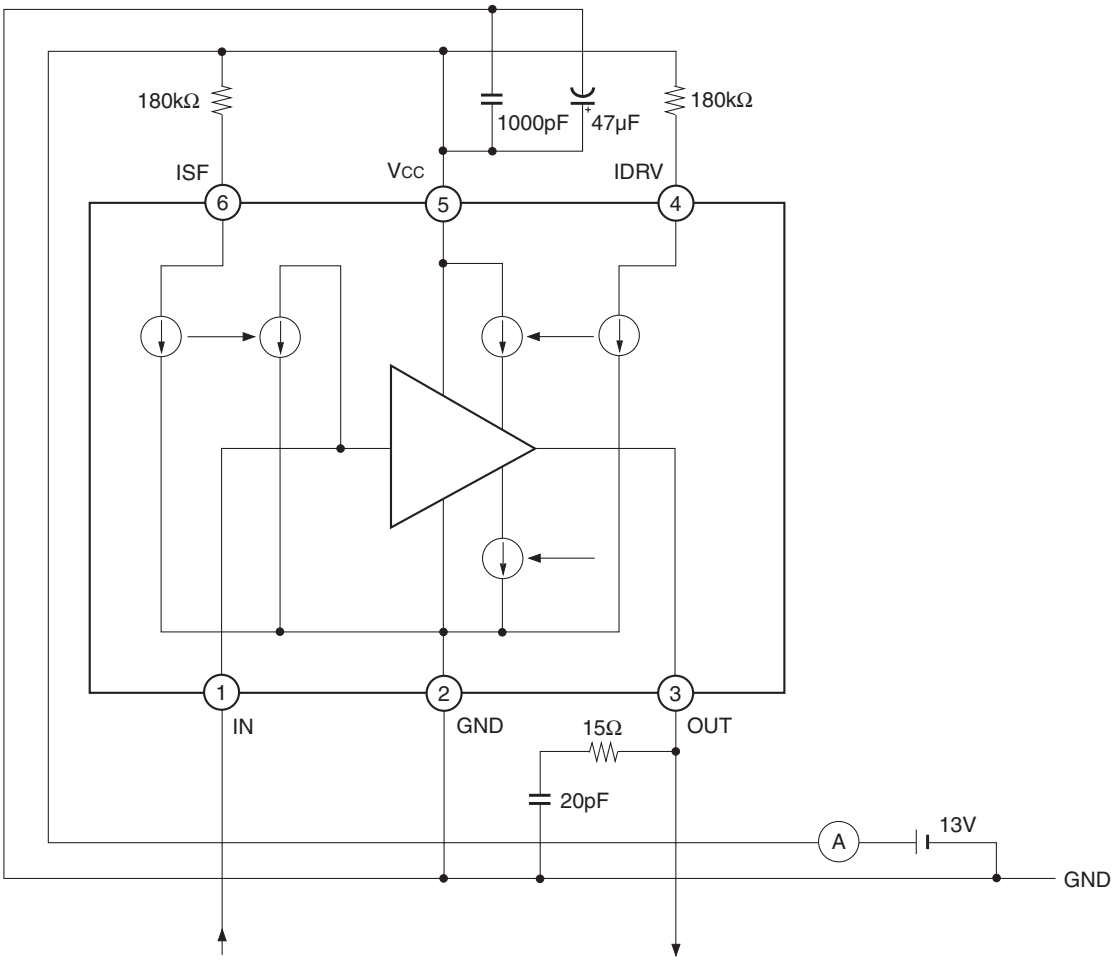
Evaluation Circuit



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Description of Operation

Current Settings

1. Output Drive Current

The small signal output impedance of the OUT pin (Pin 3) can be set by connecting the IDRV pin (Pin 4) to V_{CC} through a resistor. The inflow current to the IDRV pin is multiplied by 10 times inside the IC, and flows as the output stage idling current.
The IDRV pin has an internal 50kΩ resistor, so the inflow current to the IDRV pin can be calculated as follows.

$$I_{IDRV} = (V_{CC} - V_{BE} \times 2)/(R_{IDRV} + 50k\Omega)$$
$$= (13 - 1.46)/(180k\Omega + 50k\Omega)$$
$$= 50.2\mu A$$

Here, V_{CC} = 13V, V_{BE} = 0.73V (typ.), and R_{IDRV} = 180kΩ.
The small signal output impedance at this time can be calculated as follows.

$$R_{OUT} = (26mV/(10 \times I_{IDRV}))/2$$
$$= (26mV/502\mu A)/2$$
$$= 26\Omega$$

2. Sink Current for CCD with open source output

The sink current of the IN pin (Pin 6) can be set by connecting the ISF pin (Pin 1) to V_{CC} through a resistor. This sink current can be used as the CCD output stage source follower drive current. The inflow current to the ISF pin is multiplied by 58 times inside the IC, and flows as the sink current.
The ISF pin has an internal 50kΩ resistor, so the inflow current to the ISF pin can be calculated as follows.

$$I_{ISF} = (V_{CC} - V_{BE} \times 2)/(R_{ISF} + 50k\Omega)$$
$$= (13 - 1.46)/(180k\Omega + 50k\Omega)$$
$$= 50.2\mu A$$

Here, V_{CC} = 13V, V_{BE} = 0.73V (typ.), and R_{ISF} = 180kΩ.
The sink current at this time can be calculated as follows.

$$Isink = 58 \times I_{ISF}$$
$$= 2.9mA$$

Note) This IC operation depends on IDRV and ISF.
Set the external resistance so that IDRV and ISF current are 90μA or less, referring to the table shown below.

[IDRV and ISF vs. external resistor]

Current (μA)	90	68	50	35	26	Unit
When V_{CC} = 15V	100	150	220	330	470	kΩ
When V_{CC} = 13V	78	120	180	270	390	kΩ

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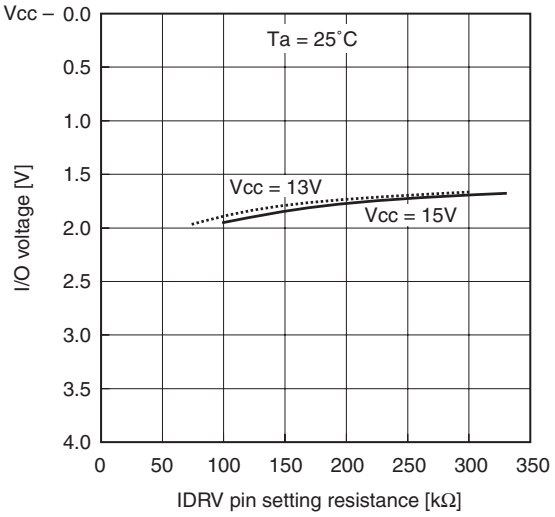
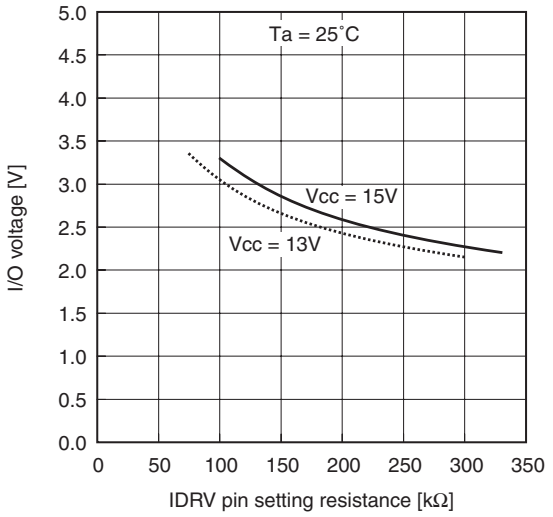
Example of Representative Characteristics

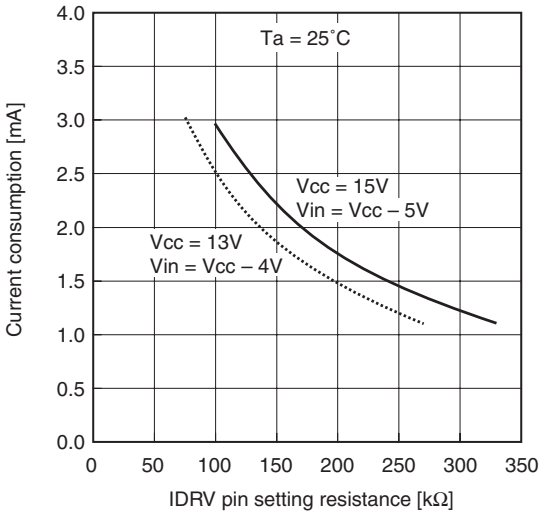
(Upper side) I/O voltage range vs. IDRV pin setting resistance



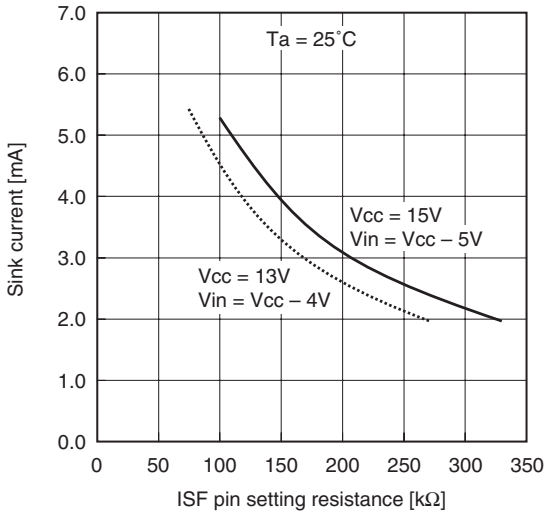
(Lower side) I/O voltage range vs. IDRV pin setting resistance



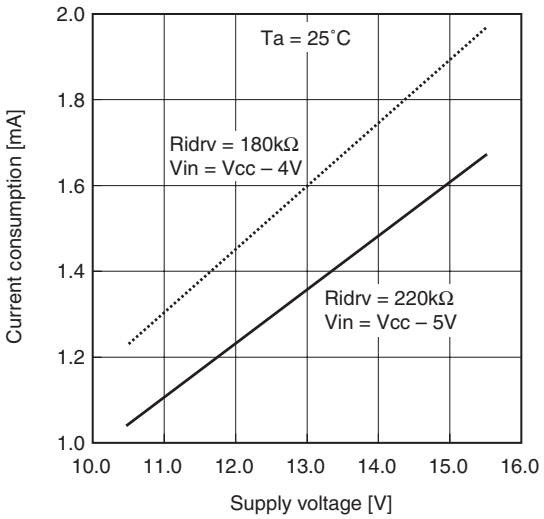
Current consumption vs. IDRV pin setting resistance



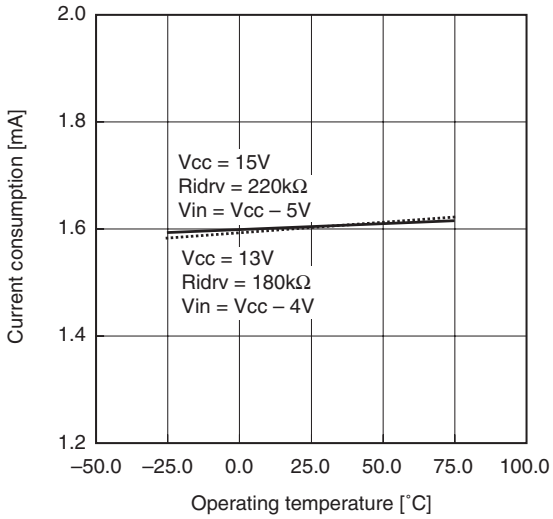
Sink current vs. ISF pin setting resistance



Current consumption vs. Supply voltage



Current consumption vs. Operating temperature



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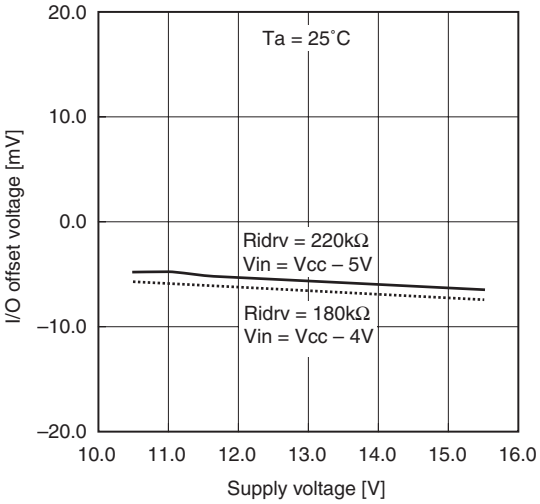
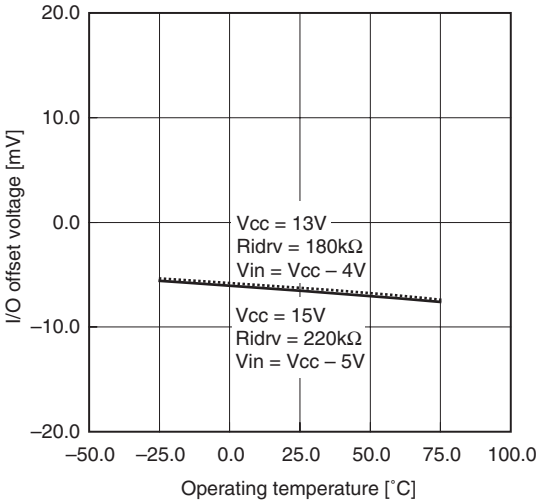
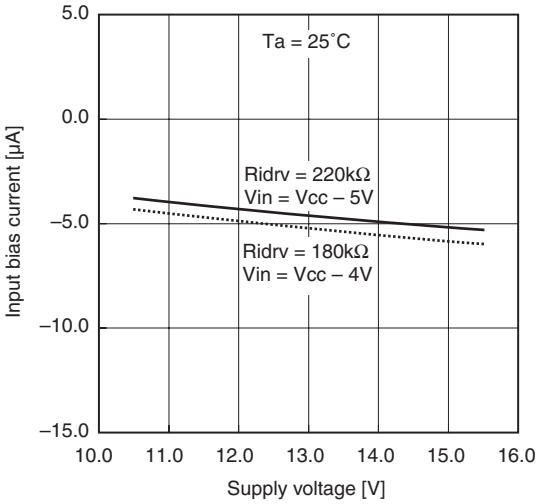
I/O offset voltage vs. Supply voltage



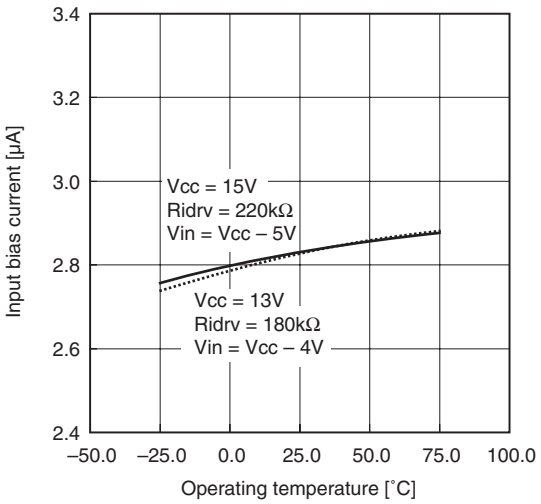
I/O offset voltage vs. Operating temperature



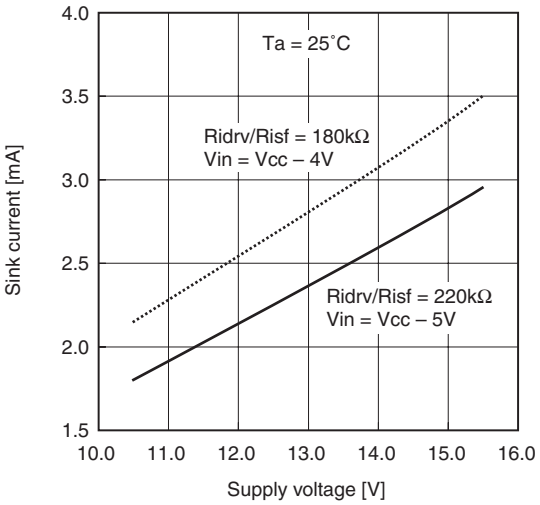
Input bias current vs. Supply voltage



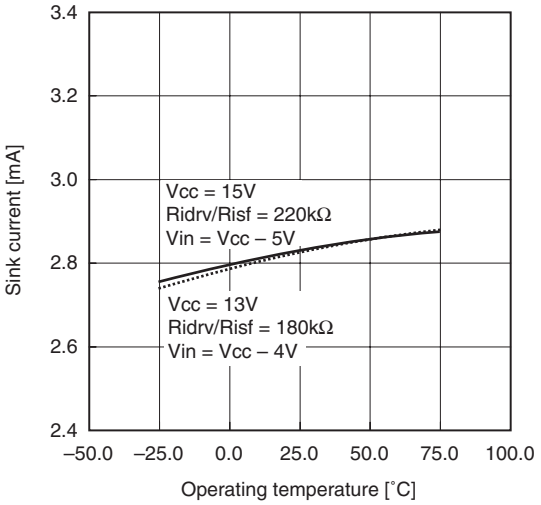
Input bias current vs. Operating temperature



Sink current vs. Supply voltage



Sink current vs. Operating temperature



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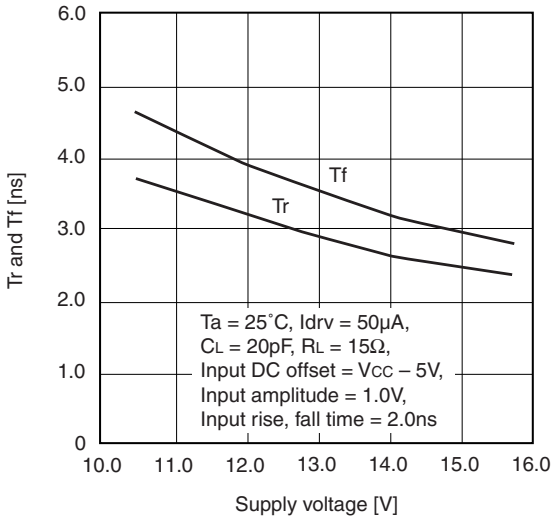
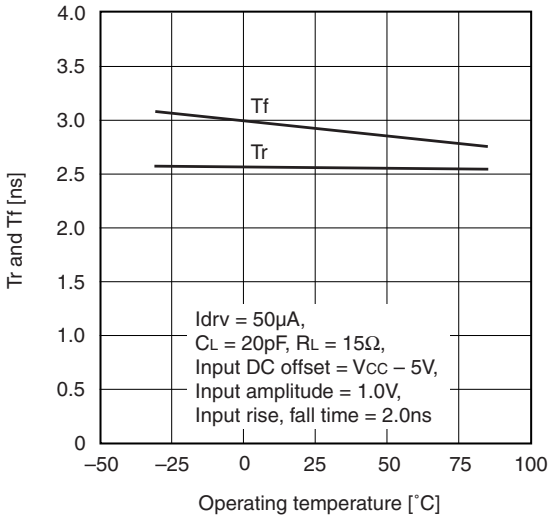
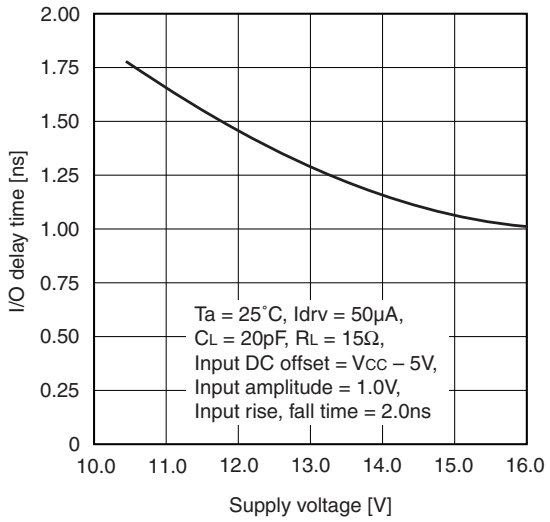
Tr and Tf vs. Supply voltage



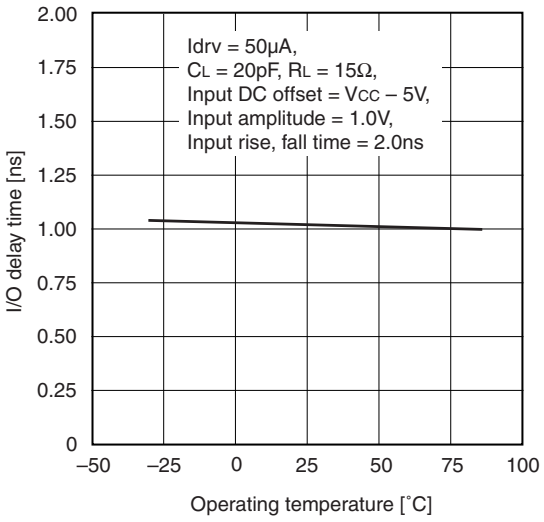
Tr and Tf vs. Operating temperature



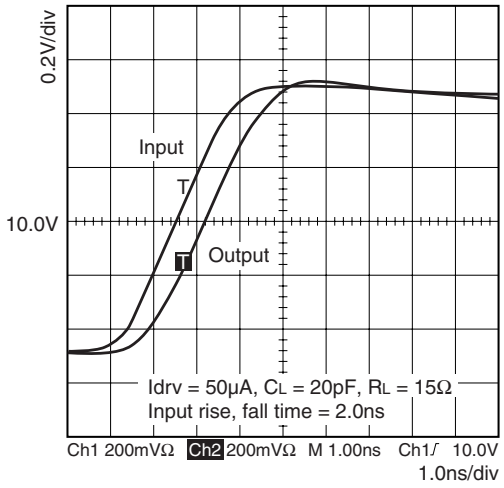
I/O delay time vs. Supply voltage



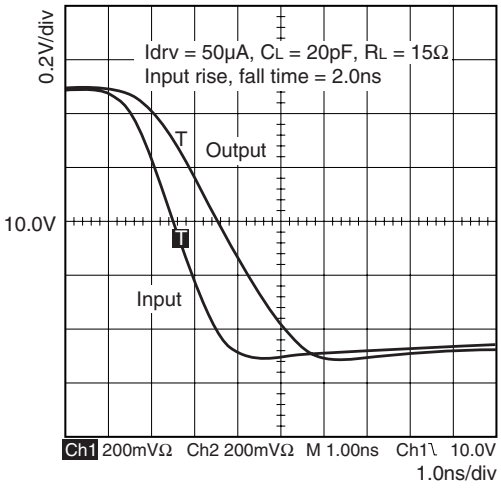
I/O delay time vs. Operating temperature



Positive pulse response



Negative pulse response



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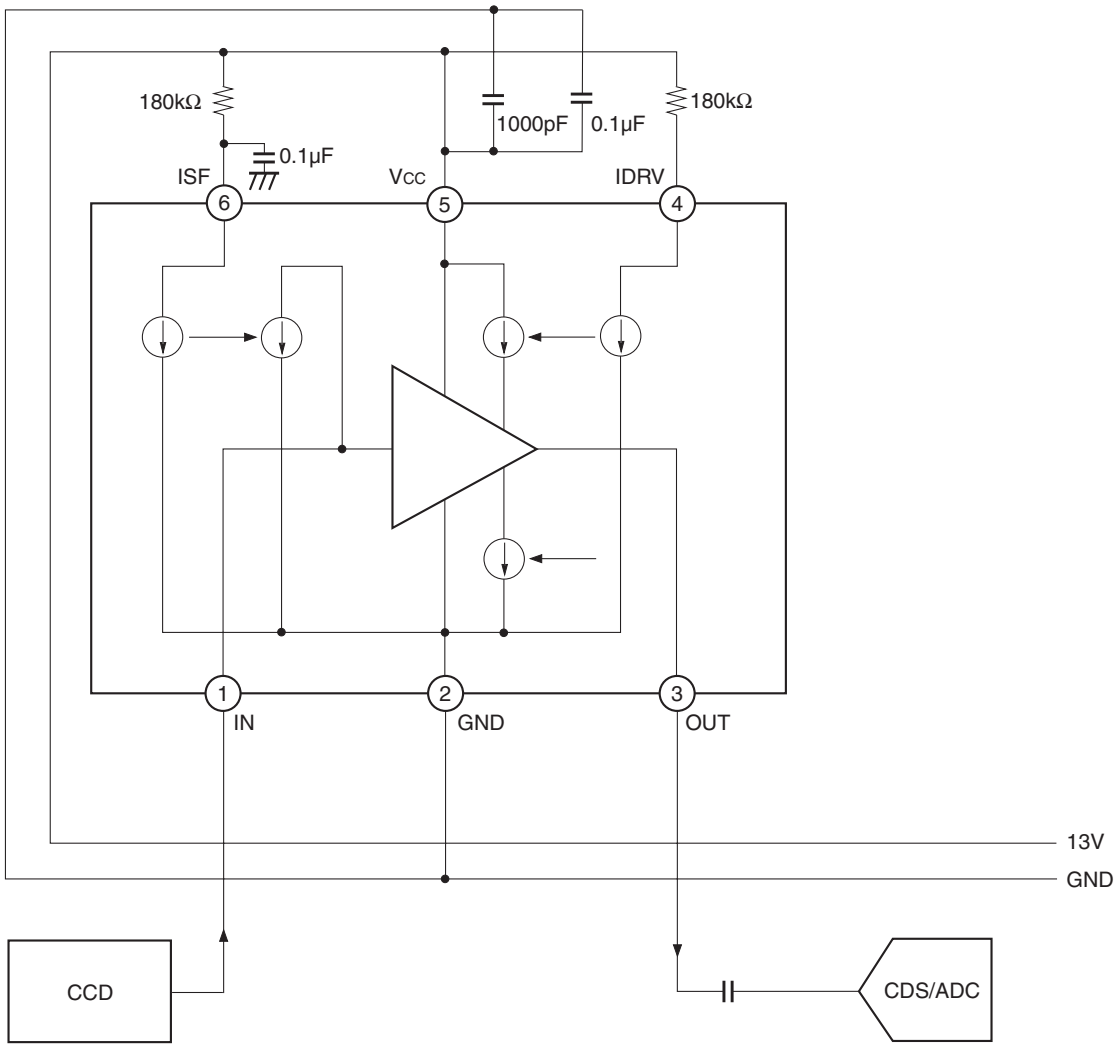
Application Circuit 1 when using CCD with open source output



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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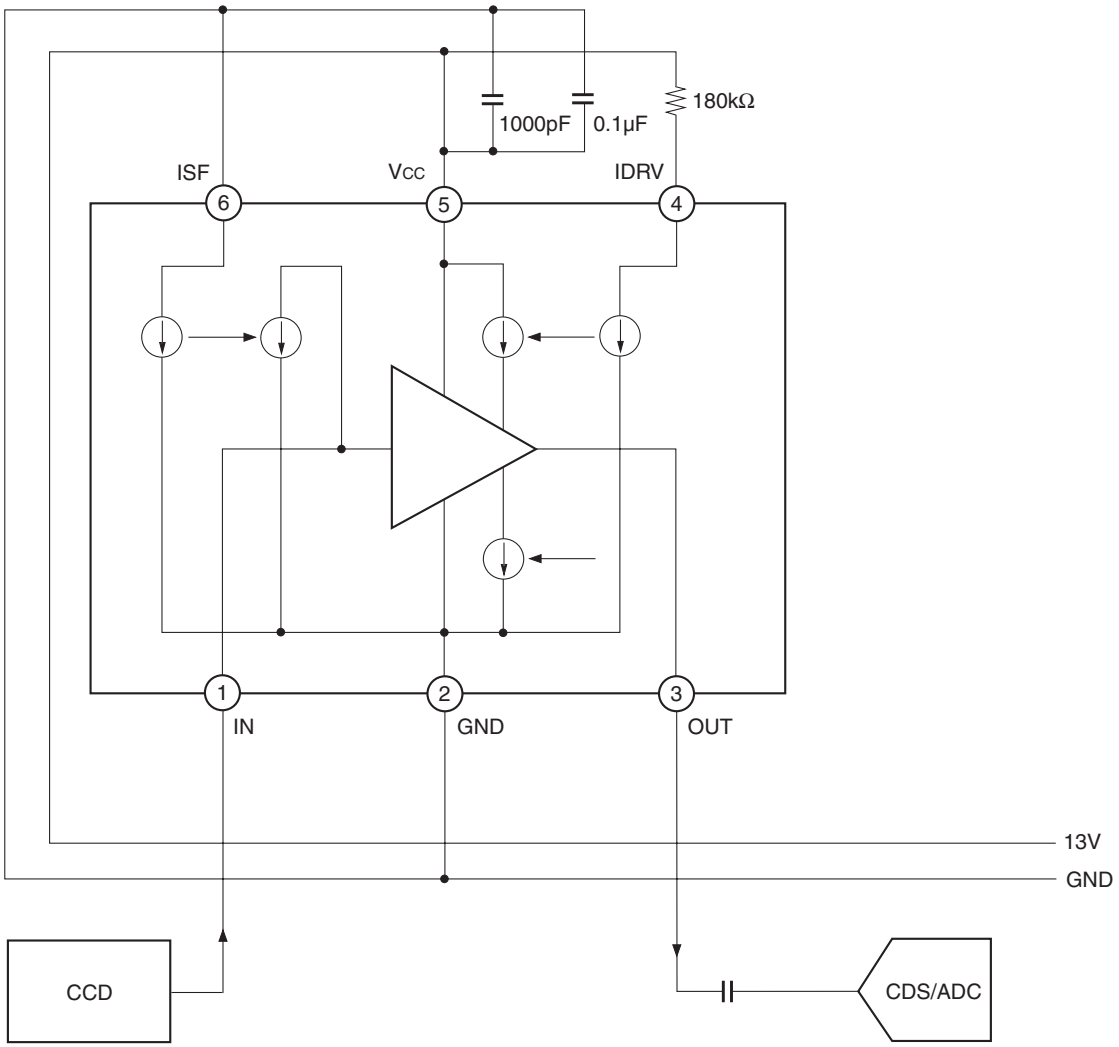
Application Circuit 2 when using CCD with internal current source



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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Notes on Operation

◆ Provide the widest GND pattern possible on the board.

◆ Use a 1000pF (recommended) and a 0.1μF (recommended) ceramic capacitors in parallel for the bypass capacitor connected between the power supply and GND, and connect them as close to the IC pins as possible.

◆ Load capacitance causes the input/output wiring response to worsen and results in noise. Use the shortest wiring layout possible, and shield it with GND.

◆ When the output pin (Pin 3) is shorted to either the power supply or GND, an overcurrent may flow to the output stage elements and damage them.
When the input pin (Pin 1) is shorted to GND, an overcurrent may flow to the internal parasitic elements and damage them.

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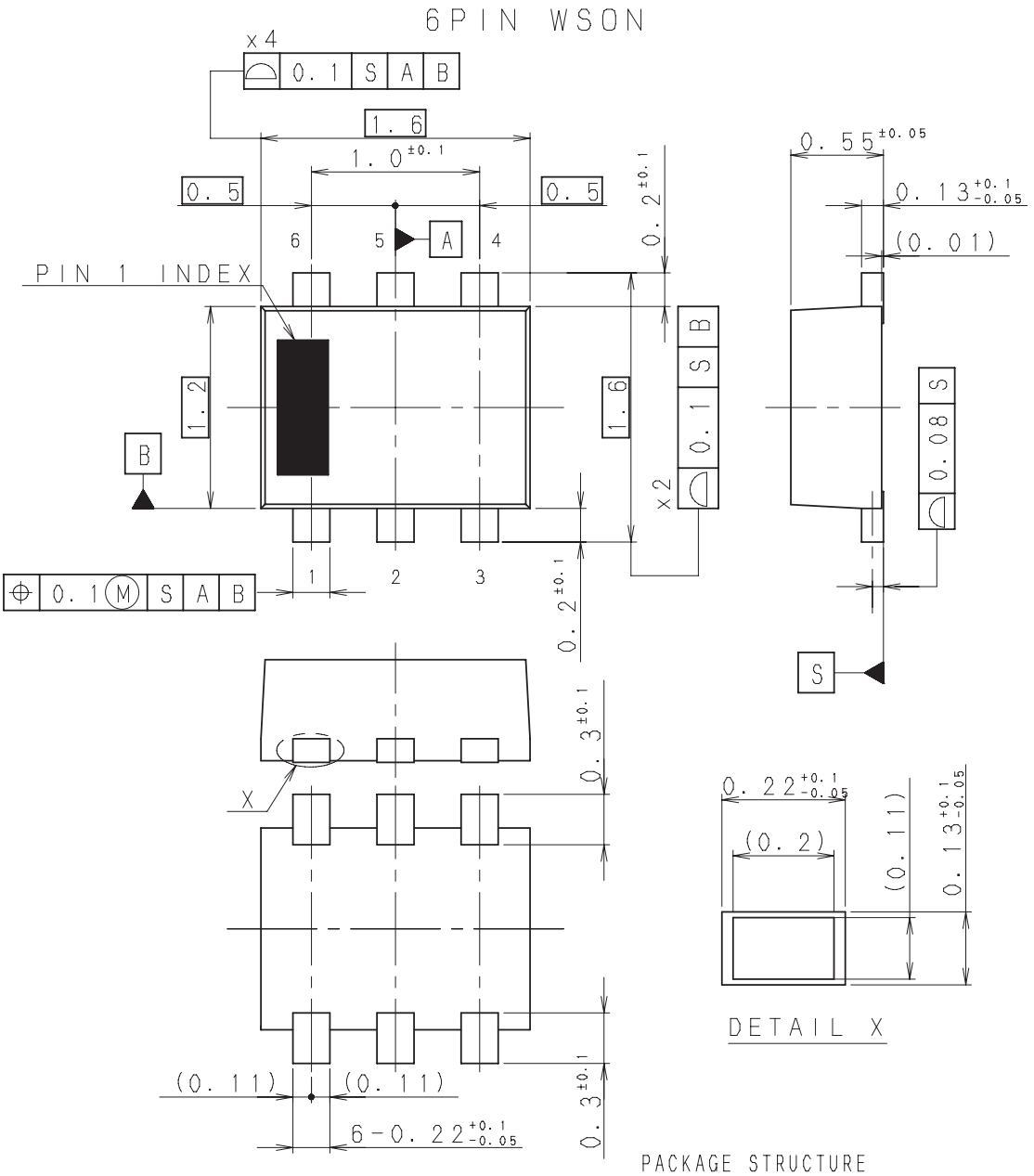
Package Outline

(Unit: mm)



SONY CODE	WSON-6P-052
JEITA CODE	————
JEDEC CODE	————

AP-2000-6SND2 Rev. 0

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	Sn-Bi
LEAD MATERIAL	COPPER
PACKAGE MASS	0.003g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm