19-4938; Rev 0; 9/09

EVALUATION KIT AVAILABLE

MAXIM

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

General Description

The MAX6948B general-purpose input/output (GPIO) peripheral drives a series string of white LEDs (WLEDs), and contains up to five general-purpose input/output (GPIO) ports to drive additional LEDs.

The integrated 2MHz boost converter minimizes the size and cost of external components and supplies 30mA of load current at up to 28V. The converter is stable under all load conditions from 5V up to 28V and includes open-circuit detection to prevent damage to the IC. An I²C-programmable 10-bit pulse-width modulation (PWM) signal enables 1024 levels of WLED intensity.

The five GPIO ports function as logic inputs, open-drain logic outputs, or constant-current sinks in any combination. Ports withstand 5.5V independent of the MAX6948B's supply voltage. Two of the ports drive additional LEDs up to 30mA/port, while the other three ports drive LEDs at up to 10mA/port. The MAX6948B features shutdown and standby modes for low-power dissipation. The constant-current drivers contain programmable PWM outputs and allow staggering to reduce the input peak-current requirements. The I/O ports also feature ramp-up and ramp-down controls.

The MAX6948B features a single input to select from four I²C slave addresses. Programming and functionality for the five GPIO ports is identical to the MAX6946/MAX6947 I/O expanders.

The MAX6948B is available in a 25-bump (2.31mm x 2.31mm) WLP package for cell phones, PDAs, and other portable consumer electronic applications. The MAX6948B operates over the -40°C to +105°C temperature range.

Applications

LED Backlighting for LCDs

Cell Phones

PDAs

Handheld Games

Portable Consumer Electronics

Features

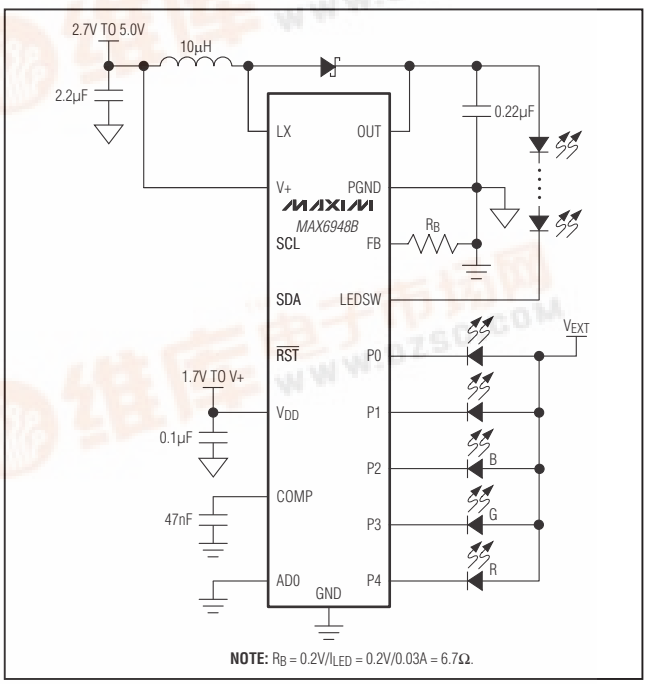
- **28V Step-Up DC-DC Converter with Integrated nMOS Power Switch**
- **Built-In 10-Bit PWM Control for Improved Efficiency**
- **No Discharge Path During PWM Off Period for Increased Battery Life**
- **Fixed 2MHz Switching for Smaller Components Drives up to 6 Series WLEDs**
- **±8kV Human Body Model (HBM) ESD Protection for GPIOs and Boost-Converter Output**
- **Five Open-Drain GPIOs Capable of Constant-Current LED Drive with Individual 8-Bit PWM Intensity Control**
- **2.7V to 5V Power-Supply Operation**
- **400kbps, 5.5V Tolerant I²C Interface**
- **Four I²C Slave Address Choices**
- **$\overline{RST}$ Input Clears Serial Interface and Exits Shutdown (Reset-Run Option)**
- **Small (2.31mm x 2.31mm) WLP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6948BGWA+	-40°C to +105°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



NOTE: $R_B = 0.2V/I_{LED} = 0.2V/0.03A = 6.7\Omega$.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3V to +6V
V_{DD}, COMP to GND ..... -0.3V to (V+ + 0.3V)
PGND to GND ..... -0.3V to +0.3V
LX to PGND (Note 1) ..... -0.3V to +30V
Current into LX (Note 1) 700mA
OUT, LEDSW to PGND (Note 1) ..... -0.3V to +30V
P0–P4 to GND ..... -0.3V to +6V
$\overline{RST}$, SDA, SCL, AD0 to GND ..... -0.3V to (V_{DD} + 0.3V)
FB to PGND (Note 1) ..... -0.3V to +0.3V
I.C. to GND ..... -0.3V to +0.3V
DC Current on P0–P4 ..... 50mA
DC Current on SDA 10mA
Total GND Current 150mA
Total PGND Current 150mA

Continuous Power Dissipation (T_A = +70°C)
25-Bump WLP (derate 10.8mW/°C above +70°C) 866mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
25-Bump WLP ..... 93°C/W
Operating Temperature Range
(T_{MIN} to T_{MAX}) ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
P0–P4, OUT, LEDSW, FB to GND ..... ±8kV
All Other Pins ..... ±2kV
Lead Temperature (soldering, 10s)
25-Bump WLP ..... (Note 3)

Note 1: LX, FB, LEDSW pins have an internal clamp diode to PGND. Applications that forward bias these diodes should take care not to exceed the power dissipation limits of the device.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a single-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Note 3: Refer to the Pb-free solder reflow requirement in J-STD -020, Rev D.1.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V+ = 2.7V to 5.0V, V_{DD} = 1.7V to V+, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage (V+)	V+			2.7	3.3	5.0	V
Operating Supply Voltage (V_{DD})	V_{DD}			1.7	2.5	V+	V
Output Load External Supply Voltage	V_{OUT}	Boost-converter output				28	V
Port External Supply Voltage	V_{EXT}	P0–P4 at high impedance				5.5	V
Port Voltage (P0, P4)	V_{PORT}	Constant-current on				V+	V
Power-On-Reset Voltage	V_{POR}	Voltage rising			1.7		V
Standby Current	I_{STBY}	Standby mode, boost converter off, $\overline{RST}$ = V_{DD}, all digital inputs at V_{DD} or GND	T_A = +25°C		1.5	4	µA
			T_A = T_{MIN} to T_{MAX}			6	
Standby Current in Reset (Interface Active)	I_{RST}	Standby mode, $\overline{RST}$ = GND, f_{SCL} = 400kHz, all other digital inputs at V_{DD} or GND	T_A = +25°C		1.6	4	µA
			T_A = T_{MIN} to T_{MAX}			6	

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V+ = 2.7V to 5.0V, V_{DD} = 1.7V to V+, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change in Supply Current per 30mA Port	ΔI_{DD30}	One port set to 30mA constant current; all other ports are digital inputs at V_{DD} or GND	T_A = +25°C		3	6.2	mA
			T_A = T_{MIN} to T_{MAX}			7	
Change in Supply Current per 10mA Port	ΔI_{DD10}	One port set to 5mA constant current half-current setting; all other ports are digital inputs at V_{DD} or GND	T_A = +25°C		1.3	1.7	mA
			T_A = T_{MIN} to T_{MAX}			2	
GPIO PORTS (P0–P4)							
Input High Voltage	V_{IH1}	Port I/O register value set to 0x01		(0.7 x V_{DD})			V
Input Low Voltage	V_{IL1}	Port I/O register value set to 0x01				(0.3 x V_{DD})	V
Input Leakage Current	I_{IN}				±0.03	±1	µA
Input Capacitance					10		pF
30mA Port Sink Constant Current (P0, P1)	I_{PORT30}	Port I/O register value set to 0x02, V+ = 3.3V, V_{EXT} - V_{LED} = 0.5V to 1.5V (Note 5)	T_A = +25°C	27	30	34	mA
			T_A = T_{MIN} to T_{MAX}	25		35	
10mA Port Sink Constant Current (P2, P3, P4)	I_{PORT10}	5mA half-current setting, port I/O register value set to 0x02, V+ = 3.3V, V_{EXT} - V_{LED} = 0.5V to 1.5V (Note 5)	T_A = +25°C	4.4	5	5.6	mA
			T_A = T_{MIN} to T_{MAX}	3.7		6.3	
Logic Output Low Voltage	V_{OL1}	I_{SINK} = 2mA, port I/O register value set to 0x00			0.17	0.3	V
30mA Port Sink Constant-Current Matching (P0, P1)	ΔI_{PORT30}	Constant current set to 30mA, V+ = 3.3V, T_A = +25°C (Note 6)	V_{PORT} = 1V		±0.7	±5	%
			V_{PORT} = 2.75V			±5	
10mA Port Sink Constant-Current Matching (P2, P3, P4)	ΔI_{PORT10}	Constant current set to 5mA half-current setting, V+ = 3.3V, T_A = +25°C (Note 6)	V_{PORT} = 1V		±2	±5	%
Constant-Current Slew Time		20% current to 80% current, port I/O register value changed from 0x01 to 0x02			2		µs

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V+ = 2.7V to 5.0V, V_{DD} = 1.7V to V+, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST CONVERTER						
Undervoltage Lockout Threshold	V_{UVLO}	V+ rising			2.65	V
		V+ falling	2.3			
Undervoltage Lockout Threshold Hysteresis	V_{HYS}			30		mV
Continuous Output Current	I_{WLED}	100% boost LED PWM, full-current setting, R_B = 6.67Ω, I_{WLED} = V_{FB}/R_B		30		mA
Operating Current		Run bit = 1, boost standby bit = 0, 0% boost LED PWM			2	mA
LX Current Limit		V+ = 3.3V, T_A = +25°C	430	500	570	mA
LX Saturation Voltage		I_{LX} = 200mA		0.1	0.25	V
LX Leakage Current	I_{LXOFF}	0% boost LED PWM, V_{LX} = 10V			8	µA
OUT Leakage Current	I_{OUTOFF}	V_{OUT} = 28V, boost converter in shutdown		16	23	µA
Operating Frequency	f_{BOOST}			2		MHz
Minimum Duty Cycle		Continuous conduction mode		10		%
		Discontinuous conduction mode		0		
Maximum Duty Cycle				95		%
GM Amplifier Transconductance				250		µS
FB Leakage Current	I_{FB}	V_{FB} = 100mV		±0.01	±1	µA
Feedback Output Voltage	V_{FB}	Half-current setting, V+ = 3.3V, T_A = +25°C	94	100	106	mV
		Full-current setting, V+ = 3.3V, T_A = +25°C	190	200	210	
		Half-current setting	90	100	110	
		Full-current setting	175	200	225	
Quick-Start Charge Current	I_{QS}			150		µA
Quick-Start Time		From enable command STOP condition to output regulation, C_{COMP} = 0.047µF (Note 7)		3.5	5	ms
Shutdown Discharge Resistance	R_{COMP}			20		kΩ
Output Current Line Regulation		3.0V < V+ < 5.0V		2		%/V
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Threshold Hysteresis				9		°C
Overvoltage Threshold	V_{OV}	V_{OUT} Rising	28	29	30	V
Overvoltage Threshold Hysteresis	V_{OV_HYS}			4		V
SERIAL INTERFACE (SDA, SCL, AD0, $\overline{RST}$)						
Input High Voltage	V_{IH2}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL2}				0.3 x V_{DD}	V
Input Leakage Current	I_{IN2}			0.03		µA
Output Low Voltage SDA	V_{OL2}	I_{SINK} = 6mA			0.3	V
Input Capacitance	C_{IN2}			10		pF

TIMING CHARACTERISTICS

(*Typical Application Circuit*, V+ = 2.7V to 5.0V, V_{DD} = 1.7V to V+, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Boost-Converter PWM Clock Frequency	f_{INT_BOOST}		98	125	145	kHz
Internal GPIO PWM Clock Frequency	f_{INT_GPIO}		24	31.25	38	kHz
SCL Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 8)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		180			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 7, 9)		20 + 0.1C_b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 7, 9)		20 + 0.1C_b	300	ns
Fall Time of SDA Transmitting	$t_{F, TX}$	(Notes 7, 9)		20 + 0.1C_b	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 7, 10)		50		ns
Serial Bus Timeout	t_{OUT}		20	30	50	ms
Capacitive Load for Each Bus Line	C_b	(Note 7)			400	pF
$\overline{RST}$ Pulse Width	t_W		1			µs

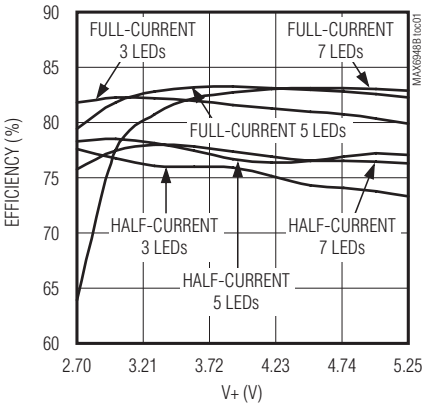
Note 4: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 5: The $\Delta I_{PORT\_}$ specifies current matching between ports of a single part.
Note 6: Current matching is defined as the percent error of any individual port from the average current of the maximum value measured and the minimum value measured. It can be found using the equation $\Delta I_{PORT\_}$ = 100 x (I_{MMAVG} - I_{MEAS})/ I_{MMAVG} where I_{MMAVG} = ($I_{MEASMAX}$ + $I_{MEASMIN}$)/2.
Note 7: Guaranteed by design.
Note 8: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 9: $I_{SINK} \le$ 6mA. C_b = total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 x V_{DD} and 0.7 x V_{DD}.
Note 10: Input filters on the SDA, SCL, and AD0 inputs suppress noise spikes less than 50ns.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

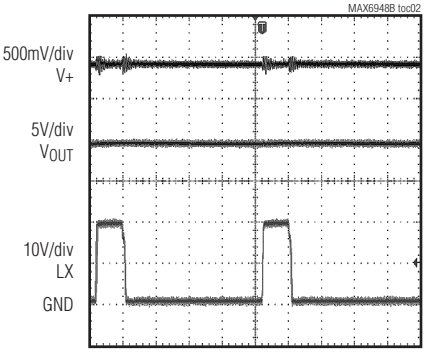
Typical Operating Characteristics

(V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C, unless otherwise noted.)

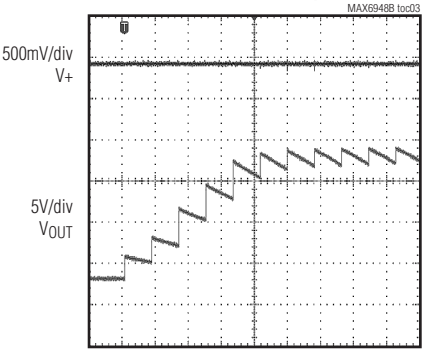
EFFICIENCY vs. V+



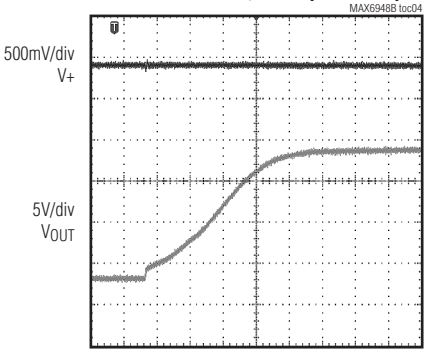
SWITCHING WAVEFORMS



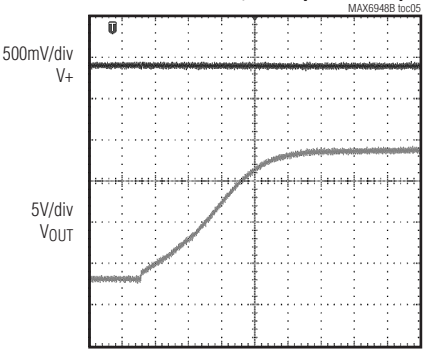
SOFT-START V+, VOUT (10/1024)



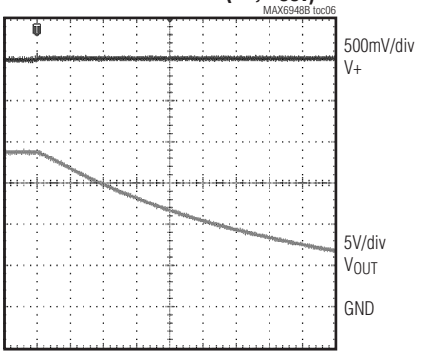
SOFT-START V+, VOUT (512/1024)



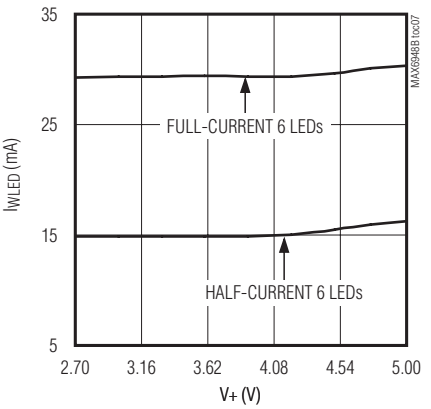
SOFT-START V+, VOUT (1024/1024)



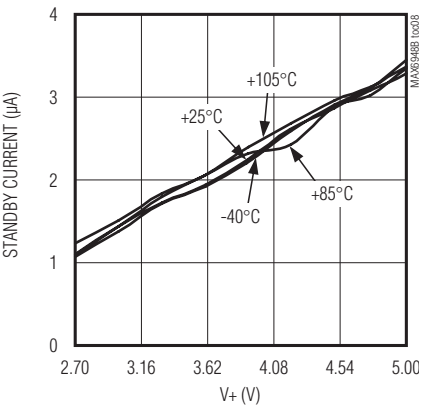
SHUTDOWN RESPONSE (V+, VOUT)



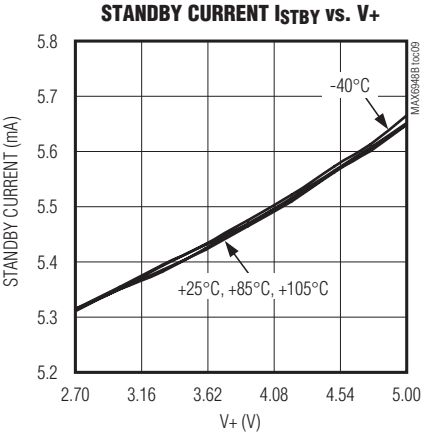
IWLED 30mA OUTPUT CURRENT vs. V+



STANDBY CURRENT ISTBY vs. V+



STANDBY CURRENT ISTBY vs. V+

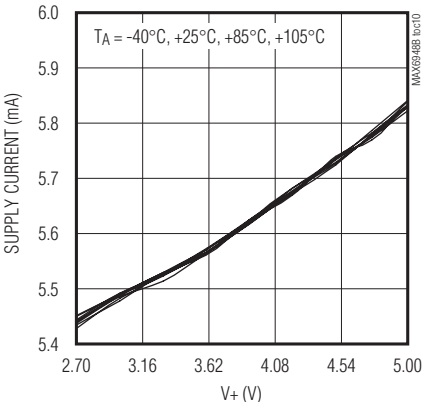


High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

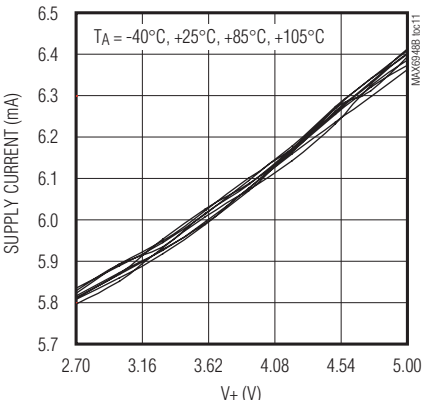
Typical Operating Characteristics (continued)

(V+ = 3.3V, V_{DD} = 2.5V, T_A = +25°C, unless otherwise noted.)

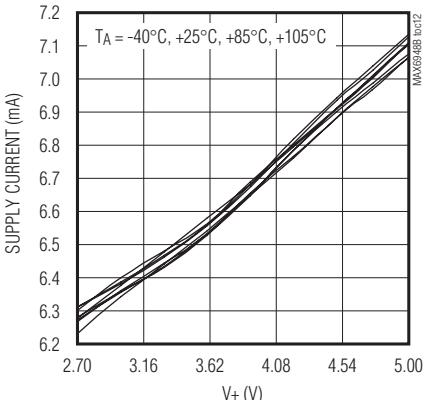
SUPPLY CURRENT vs. V+ (BOOST ON, 10% PWM, FULL CURRENT AND HALF CURRENT)



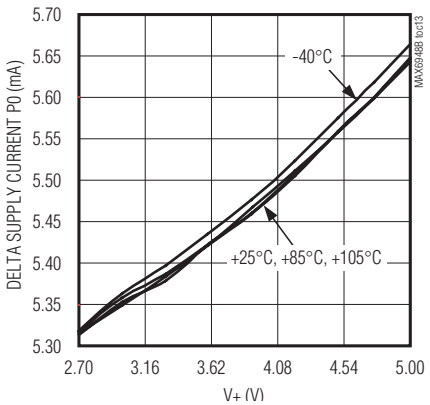
SUPPLY CURRENT vs. V+ (BOOST ON, 50% PWM, FULL CURRENT AND HALF CURRENT)



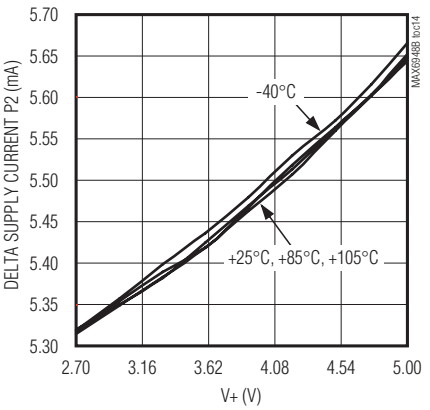
SUPPLY CURRENT vs. V+ (BOOST ON, 10% PWM, FULL CURRENT AND HALF CURRENT)



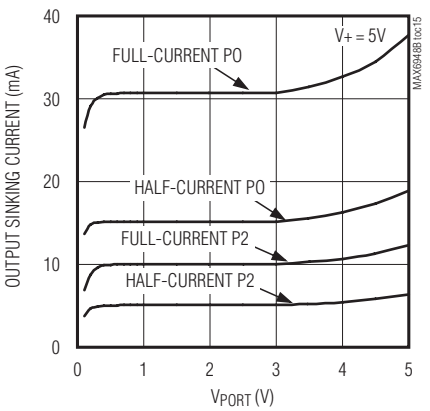
DELTA SUPPLY CURRENT P0 vs. V+ (DIFFERENCE IN CURRENT FROM PORT OFF TO ON)



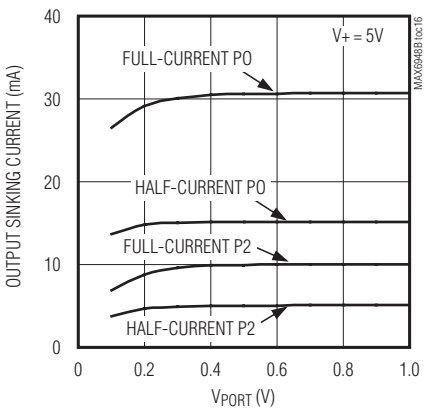
DELTA SUPPLY CURRENT P2 vs. V+ (DIFFERENCE IN CURRENT FROM PORT OFF TO ON)



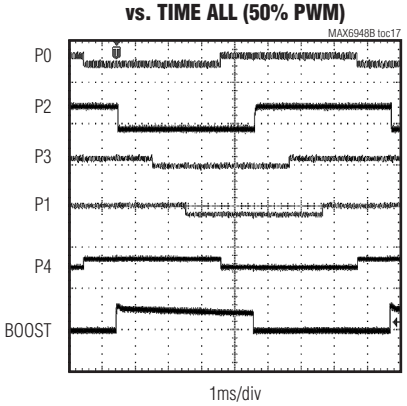
OUTPUT SINKING CURRENT vs. V_{PORT}



OUTPUT SINKING CURRENT vs. V_{PORT}

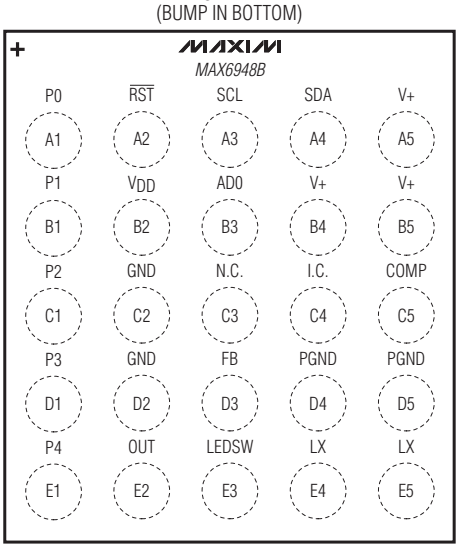


STAGGER PWM PORT WAVEFORMS vs. TIME ALL (50% PWM)



High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Pin Configuration



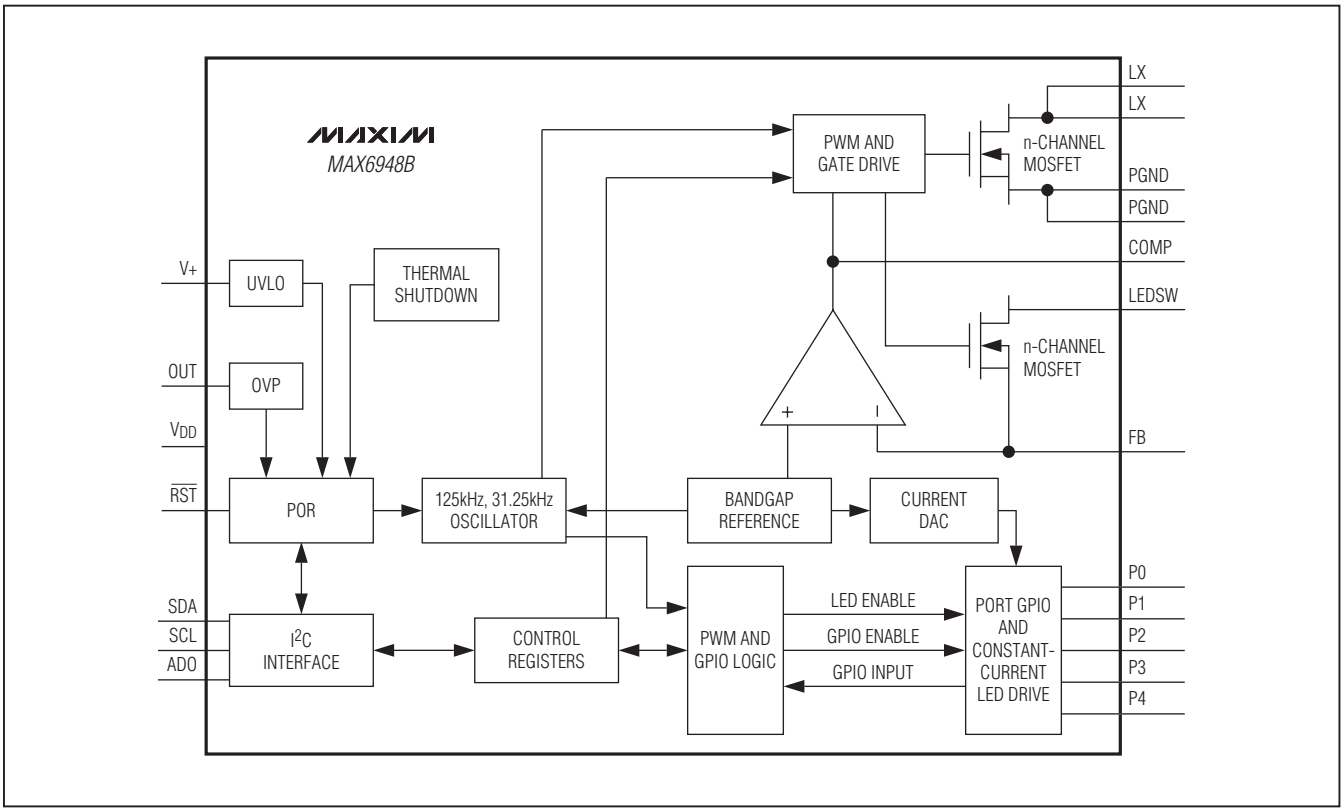
WLP
(2.31mm x 2.31mm)

Pin Description

PIN	NAME	FUNCTION
A1	P0	GPIO Port. Open-drain I/O. P0 can be configured as a 30mA (max) constant sink current output.
A2	$\overline{RST}$	Active-Low Reset Input
A3	SCL	I²C-Compatible, Serial-Clock Input
A4	SDA	I²C-Compatible, Serial-Data I/O
A5, B4, B5	V+	Boost-Converter Supply Voltage and Positive Supply Voltage. Bypass V+ to GND with a 2.2µF or higher value ceramic capacitor.
B1	P1	GPIO Port. Open-drain I/O. P1 can be configured as a 30mA (max) constant sink current output.
B2	V_{DD}	I²C Logic Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or higher value ceramic capacitor.
B3	AD0	Address Input. AD0 selects up to four device slave addresses (Table 13).
C1	P2	GPIO Port. Open-drain I/O. P2 can be configured as a 10mA (max) constant sink current output.
C2, D2	GND	Ground. Connect to PGND.
C3	N.C.	No Connection. Internally not connected.
C4	I.C.	Internally Connected. Connect I.C. to GND for normal operation.
C5	COMP	Compensation Terminal for the Boost Converter. A capacitor from COMP to PGND determines the boost-converter stability.
D1	P3	GPIO Port. Open-drain I/O. P3 can be configured as a 10mA maximum constant sink current output.
D3	FB	Load Current-Sense Voltage Feedback for the Boost Converter. A resistor between FB and PGND sets the maximum load current.
D4, D5	PGND	Power Ground. Connect PGND to GND.
E1	P4	GPIO Port. Open-drain I/O. P4 can be configured as a 10mA (max) constant sink current output.
E2	OUT	Output Voltage Sense Input for Boost Converter
E3	LEDSW	High-Voltage, Constant-Current Input. Connect LEDSW to the cathode-end of the WLED string.
E4, E5	LX	Inductor Switch Node

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Functional Block Diagram



Detailed Description

The MAX6948B general-purpose input/output (GPIO) peripheral with integrated boost converter provides a boost converter capable of driving 6 WLEDs and five I/O ports capable of driving LEDs powered from an alternate power supply such as the Li+ battery. The integrated 2MHz boost converter minimizes the size and cost of external components and supplies 30mA of load current at up to 28V. The feedback input to the error amplifier has a typical set point of 0.1V to minimize power dissipation. External compensation keeps the converter stable under all load conditions from 5V up to 28V. The MAX6948B includes overvoltage and open-circuit detection to prevent damage to the IC.

An I2C-programmable 10-bit PWM signal enables 1024 levels of WLED intensity. During PWM off-time, the internal switch at the LEDSW pin disconnects the series WLEDs. This limits the PWM off-time leakage current to a minimum, limited only by the PWM switch internal to the MAX6948B. Consequently, the boost output voltage remains almost constant during PWM on-/off-time periods. This new approach provides advantages of minimal WLED color change for sharp WLED on and off, and more power efficiency due to minimal leakage.

The five GPIO ports function as logic inputs, open-drain logic outputs, or constant-current sinks in any combination. Ports withstand 5.5V independent of the MAX6948B's supply voltage. Two of the ports drive additional LEDs up to 30mA, while the other three ports drive LEDs at up to 10mA/port. The MAX6948B features shutdown and standby modes for low-power dissipation. The constant-current drivers contain programmable PWM outputs and allow staggering to reduce the input peak current requirements. The I/O ports also feature ramp-up and ramp-down controls.

The MAX6948B features a single input to select from four I2C slave addresses. Programming and functionality for the five GPIO ports is identical to the MAX6946/MAX6947 I/O expanders.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Register Description

The MAX6948B contains 25 internal registers (Table 1). Registers 0x00 to 0x15 control ports P0–P4 and remain compatible with the MAX6946/MAX6947 port expanders.

Register 0x20 and 0x21 set the PWM duty cycle for the integrated boost converter. Register 0x22 conveys the boost-converter status.

Table 1. Register Address Map and Autoincrement Address

ADDRESS CODE (hex)	AUTO-INCREMENT ADDRESS (hex)	READ/ WRITE	REGISTER FUNCTION	DESCRIPTION
0x00	0x01	R/$\overline{W}$	P0	Port P0 I/O control and PWM settings
0x01	0x02	R/$\overline{W}$	P1	Port P1 I/O control and PWM settings
0x02	0x03	R/$\overline{W}$	P2	Port P2 I/O control and PWM settings
0x03	0x04	R/$\overline{W}$	P3	Port P3 I/O control and PWM settings
0x04	0x10	R/$\overline{W}$	P4	Port P4 I/O control and PWM settings
0x05	—	—	Reserved	—
0x06	—	—	Reserved	—
0x07	—	—	Reserved	—
0x08	—	—	Reserved	—
0x09	—	—	Reserved	—
0x0A	0x10	R/$\overline{W}$	Group control (P0–P4)	Write: Simultaneously sets I/O and PWM settings for ports P0–P4 Read: Reads contents of address 0x00
0x0B	0x10	R/$\overline{W}$	Group control (P0, P1)	Write: Simultaneously sets I/O and PWM settings for ports P0, P1 Read: Reads contents of address 0x00
0x0C	0x10	R/$\overline{W}$	Group control (P2, P3, P4)	Write: Simultaneously sets I/O and PWM settings for ports P2, P3, P4 Read: Reads contents of address 0x00
0x0D	0x10	—	Reserved	—
0x0E	0x0E	Read only	Port input	Reads GPIO input values
0x0F	—	—	Reserved	—
0x10	0x11	R/$\overline{W}$	Configuration	Half-/full-boost current, reset options, PWM stagger, start/stop status, reset run, shutdown setting
0x11	0x12	R/$\overline{W}$	Ramp-down	Port ramp-down and hold-off settings
0x12	0x13	R/$\overline{W}$	Ramp-up	Port ramp-up setting
0x13	0x14	R/$\overline{W}$	Output current	Port half-/full-current settings
0x14	—	—	Reserved	—
0x15	0x10	R/$\overline{W}$	Global current	Port maximum current setting
0x20	0x21	R/$\overline{W}$	Boost PWM (MSB)	Boost circuit LED PWM setting (MSB)
0x21	—	R/$\overline{W}$	Boost PWM (LSB)	Boost circuit LED PWM setting (LSB)
0x22	—	R/$\overline{W}$	Boost status	Boost circuit status and standby setting

Configuration Register Format (0x10)

Use the configuration register to select PWM phasing between outputs, monitor fade status, enable hardware startup from shutdown, and select shutdown or run mode (Table 2).

Initial Power-Up

On power-up, all control registers are set to power-up values and the MAX6948B is in shutdown mode (Table 3).

Table 2. Configuration Register Format (0x10)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	Half-/full-boost current	1	Half-boost current set by R_{FB}	1
		0	Full-boost current set by R_{FB}	
D6	Reset/POR option	0	$\overline{RST}$ does not change register data	0
		1	$\overline{RST}$ resets registers to POR values	
D5	PWM stagger	0	PWM outputs are in phase	0
		1	PWM outputs are staggered	
D4	Hold-off status	0	Device is not in hold-off	Read only
		1	Device is in hold-off	
D3	Ramp-down (fade-off) status	0	Device is not in fade-off	Read only
		1	Device is in fade-off	
D2	Ramp-up status	0	Device is not in ramp-up	Read only
		1	Device is in ramp-up	
D1	Reset-run enable	0	Reset run disabled	0
		1	Reset run enabled	
D0	Run	0	Shutdown mode	0
		1	Run mode	

Table 3. Power-On Reset (POR) Values

ADDRESS CODE (hex)	READ/ WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	POR DESCRIPTION
0x00	R/$\overline{W}$	0xFF	P0	Port P0 high impedance
0x01	R/$\overline{W}$	0xFF	P1	Port P1 high impedance
0x02	R/$\overline{W}$	0xFF	P2	Port P2 high impedance
0x03	R/$\overline{W}$	0xFF	P3	Port P3 high impedance
0x04	R/$\overline{W}$	0xFF	P4	Port P4 high impedance
0x10	R/$\overline{W}$	0x00	Configuration	Shutdown mode (reset run disabled)
0x11	R/$\overline{W}$	0x00	Ramp-down	Port ramp-down and hold-off disabled
0x12	R/$\overline{W}$	0x00	Ramp-up	Port ramp-up disabled
0x13	R/$\overline{W}$	0x03	Output current	P0, P1 at full current; P2, P3, P4 at half current
0x15	R/$\overline{W}$	0x07	Global current	Maximum output current
0x20	R/$\overline{W}$	0x00	Boost PWM (MSB)	Zero PWM duty cycle
0x21	R/$\overline{W}$	0x00	Boost PWM (LSB)	Zero PWM duty cycle
0x22	R/$\overline{W}$	0x01	Boost status	Boost circuit in standby mode

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Boost Converter

Boost-Converter Output PWM

The MAX6948B boost converter has 10-bit PWM operation using an internal 125kHz clock. This yields a PWM period of 1024/125k = 8.192ms. PWM operation allows the user to adjust the LED intensity and lower the average current by enabling and disabling the boost converter at a selectable rate. This rate is set using the boost-converter output PWM registers (Tables 4, 5). The duty cycle ranges from 0/1024 (no intensity or off) to 1023/1024 (full intensity). Eight of the 10 bits, which include the MSB, are in a single register (0x20) to allow a single I²C write to set the majority of the intensity level and minimize visible flicker during intensity changes. The LSB register (0x21) allows for very fine adjustments in LED intensity.

Boost-Converter Status Register

The MAX6948B checks the boost converter and indicates its status in the boost-converter status register (Table 6). Faults indicated in this register include thermal shutdown, overvoltage, and current limit. The boost converter goes into standby mode whenever the boost standby bit (D0) = 1.

Table 4. Boost-Converter Output PWM (MSB) Register Format (0x20)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	Bit 9	—	Boost-converter output PWM bit 9 (MSB)	0
D6	Bit 8	—	Boost-converter output PWM bit 8	0
D5	Bit 7	—	Boost-converter output PWM bit 7	0
D4	Bit 6	—	Boost-converter output PWM bit 6	0
D3	Bit 5	—	Boost-converter output PWM bit 5	0
D2	Bit 4	—	Boost-converter output PWM bit 4	0
D1	Bit 3	—	Boost-converter output PWM bit 3	0
D0	Bit 2	—	Boost-converter output PWM bit 2	0

X = Don't care.

Table 5. Boost-Converter Output PWM (LSB) Register Format (0x21)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7–D2	Reserved	000000	—	000000
D1	Bit 1	—	Boost-converter output PWM bit 1	0
D0	Bit 0	—	Boost-converter output PWM bit 0 (LSB)	0

Table 6. Boost-Converter Status Register Format (0x22)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7, D6, D5	Reserved	000	—	000
D4	Schottky open	0	Schottky diode present	Read only
		1	Schottky diode open	
D3	Current limit	0	Normal output current	Read only
		1	Converter output current exceeded the current limit	
D2	Thermal shutdown	0	Normal operation	Read only
		1	Device temperature has exceeded thermal shutdown threshold	
D1	Overvoltage	0	Normal operation	Read only
		1	V_{OUT} exceeded overvoltage limit	
D0	Boost standby	0	Boost converter operating according to PWM register and configuration register	1
		1	Boost converter in standby mode	

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Boost-Converter Shutdown/Standby Modes

The boost converter shuts down when D0 of the configuration register (0x10) = 0, or when D0 of the boost-converter status register (0x22) = 1. If both the boost PWM output registers' (0x20, 0x21) values are zero, the boost converter remains in a low-current state (standby).

Undervoltage Lockout (UVLO)

Undervoltage lockout (UVLO) disables the boost converter when V+ is below 2.4V (max). This resets bit D0 of the configuration register and puts the part into shutdown mode (0x10).

Quick Start

The MAX6948B quick starts by charging C_{COMP} with a current source. During this time, the internal MOSFET is switching at the minimum duty cycle. Once V_{COMP} rises above 0.2V, the duty cycle increases until the output voltage reaches the desired regulation level. In shutdown mode, COMP is pulled to GND with a 20kΩ internal resistor.

Overvoltage Protection

If the voltage on the output terminal rises above 28.5V (min), the converter is put into standby mode. This protects the converter from excessive voltage in the event of an open-circuit condition. To detect if the boost converter has exceeded the overvoltage limit, read bit D1 of the boost-converter status register (0x22). Once the output voltage has dropped 4V below the overvoltage threshold, the read-only bit (D1) goes to zero. The boost converter leaves standby mode and normal operation resumes. Reading the register causes the bit to reset. If the fault is still active, the bit will be set again.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX6948B. When the junction temperature exceeds 151°C (typ), the boost converter and ports P0–P4 turn off, allowing the part to cool. The thermal shutdown bit (D2) of the boost configuration and status register (0x22) is set high. Bit D0 of the boost-converter status register (0x22) = 1, bit D0 of the configuration register (0x10) = 0 (reset), and the device is in shutdown mode. The MAX6948B turns on and begins to quick-start after the junction temperature cools by 10°C. Reading this register causes the bit to reset. If the fault is still active, the bit will be set again.

Current Limit

The MAX6948B current-limit function monitors the inductor current when the internal switch on the LX node is on. The device compares the inductor current to a fixed threshold. When the current exceeds the threshold, bit D3 of the boost-converter status register asserts and the switch shuts off for that cycle. Reading this register causes the bit to reset. If the fault is still active, the bit will be set again.

Boost-Converter Current Settings

The boost current, through the serial output LEDs, can be set to half or full scale by setting the FB pin voltage. The FB voltage is set through bit D7 of the configuration register (0x10) (Table 2). The FB voltage settings are 100mV or 200mV for half- or full-current mode operation, respectively.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

I/O Ports (P0–P4)

The MAX6948B contains five I/O ports (P0–P4). Configure the five I/O ports as logic inputs, open-drain logic outputs, or constant-current sinks in any combination. Table 7 provides a detailed description of the individual port configuration registers. Use registers 0x00 to 0x04 to individually assign each port (see the *PWM Intensity Control and Phasing* section). Use registers 0x0A, 0x0B, and 0x0C to assign the same port setting to multiple ports (Table 1). When powered off, the I/O ports remain in high impedance.

Figure 1 shows the I/O port structure of the MAX6948B. I/O ports P0–P4 default to high impedance on power-up, to prevent connected ports from drawing current. Ports used as inputs do not load their source signals.

Table 7. Port Registers Format (0x00 to 0x04, 0x0A, 0x0B, and 0x0C)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Port is logic-low. Port is still active in shutdown mode.	0	0	0	0	0	0	0	0
Port is logic-high. Set this mode when using GPIO as an input. Port is still active when in shutdown mode.	0	0	0	0	0	0	0	1
Port is a static constant-current sink. Port is high impedance when in shutdown mode.	0	0	0	0	0	0	1	0
Port is a constant-current sink with a 3/256 duty cycle. Port is high impedance when in shutdown mode.	0	0	0	0	0	0	1	1
Port is a constant-current sink with a 4/256 duty cycle. Port is high impedance when in shutdown mode.	0	0	0	0	0	1	0	0
Port is a constant-current sink with a 5/256 duty cycle. Port is high impedance when in shutdown mode.	0	0	0	0	0	1	0	1
• • •								
Port is a constant-current sink with a 254/256 duty cycle. Port is high impedance when in shutdown mode.	1	1	1	1	1	1	1	0
Power-up default setting (port is high impedance)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

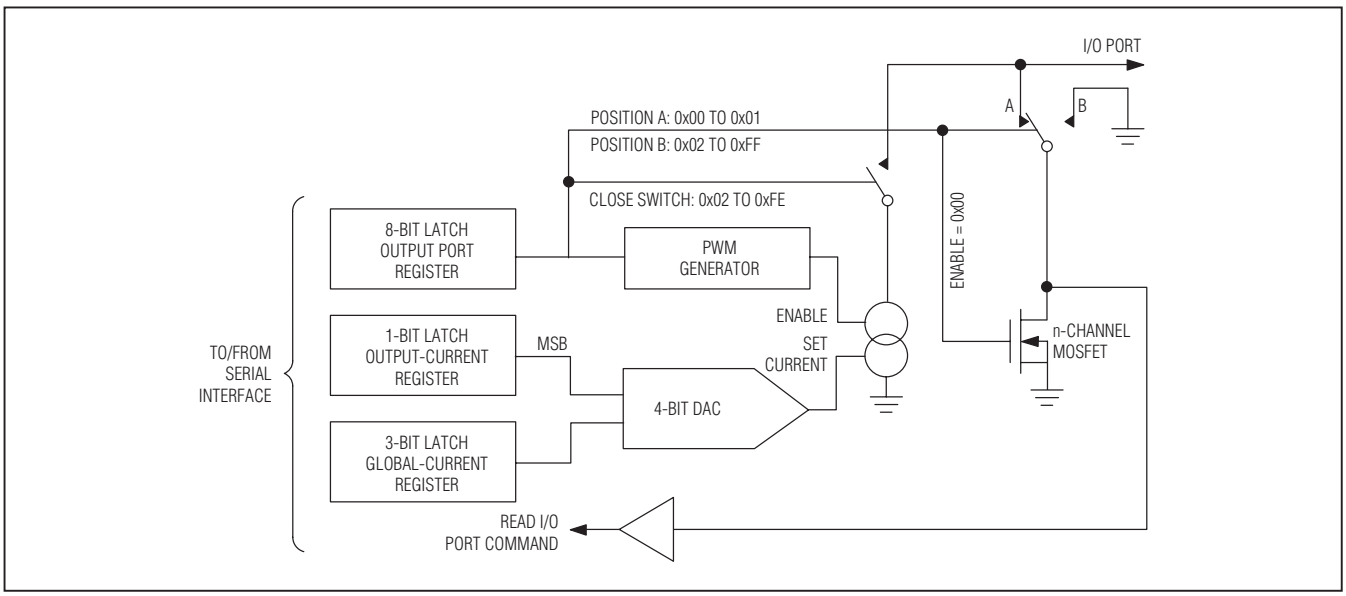


Figure 1. Simplified Schematic of I/O Ports

Ports Configured as Outputs

The global-current register sets the full (maximum) constant-current sink amount for I/O ports configured as an output (Table 8). Power-up sets the global current to its maximum value.

Set each output port's individual constant-current sink to either half scale or full scale of the global current. Use the output-current registers to set the individual currents (Table 9). By default, P0 and P1 start up set to full current, while P2, P3, and P4 are set to half current.

Set each output current individually to best suit the maximum operating current of an LED load, or adjust as needed to double the effective intensity control range of each output. The maximum individual current selection is 15mA (half) or 30mA (full) for ports P0 and P1, and 5mA (half) or 10mA (full) for ports P2, P3, and P4.

Table 8. Global-Current Register Format (0x15)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED					GLOBAL CURRENT		
3.75mA full-current value (P0, P1) 1.25mA full-current value (P2, P3, P4)	X	X	X	X	X	0	0	0
7.5mA full-current value (P0, P1) 2.5mA full-current value (P2, P3, P4)	X	X	X	X	X	0	0	1
11.25mA full-current value (P0, P1) 3.75mA full-current value (P2, P3, P4)	X	X	X	X	X	0	1	0
15mA full-current value (P0, P1) 5mA full-current value (P2, P3, P4)	X	X	X	X	X	0	1	1
18.75mA full-current value (P0, P1) 6.25mA full-current value (P2, P3, P4)	X	X	X	X	X	1	0	0
22.5mA full-current value (P0, P1) 7.5mA full-current value (P2, P3, P4)	X	X	X	X	X	1	0	1
26.25mA full-current value (P0, P1) 8.75mA full-current value (P2, P3, P4)	X	X	X	X	X	1	1	0
30mA full-current value (P0, P1) 10mA full-current value (P2, P3, P4)	X	X	X	X	X	1	1	1
Power-up default	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

X = Don't care.

Table 9. Output-Current Register Format (0x13)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7, D6, D5	Reserved	0	—	0
D4	P4	0	Port P4 is set to half current	0
		1	Port P4 is set to full current	
D3	P3	0	Port P3 is set to half current	0
		1	Port P3 is set to full current	
D2	P2	0	Port P2 is set to half current	0
		1	Port P2 is set to full current	
D1	P1	0	Port P1 is set to half current	1
		1	Port P1 is set to full current	
D0	P0	0	Port P0 is set to half current	1
		1	Port P0 is set to full current	

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

PWM Intensity Control and Phasing

The MAX6948B uses an internal 31.25kHz oscillator to generate PWM timing for LED intensity control. A PWM period comprises 256 cycles of the nominal 31.25kHz PWM clock (Figure 2). Each port can have an individual PWM duty cycle between 3/256 and 254/256. See Table 7 for port register settings.

Configure PWM timing by setting the stagger bit in the configuration register (Table 2), either with output staggering or without. Set PWM stagger = 0 to cause all outputs using PWM to switch at the same time using the timing shown in Figure 2. All outputs, therefore, draw load current at the exact same time for the same PWM setting. This means that if, for example, all outputs are set to 0x80 (128/256 duty cycle), the current draw would be zero (all loads off) for half the time, and full (all loads on) for the other half.

Set PWM stagger = 1 to stagger the PWM timing of the five port outputs and the integrated boost-converter output, distributing the port output switching points across the PWM period (Figure 3). Staggering reduces the di/dt output-switching transient on the supply and reduces the peak/mean current requirement.

Change the PWM stagger-setting bit during shutdown. Changing the stagger bit during normal operation can cause a transient flicker in any PWM-controlled LED because of the fundamental PWM timing changes.

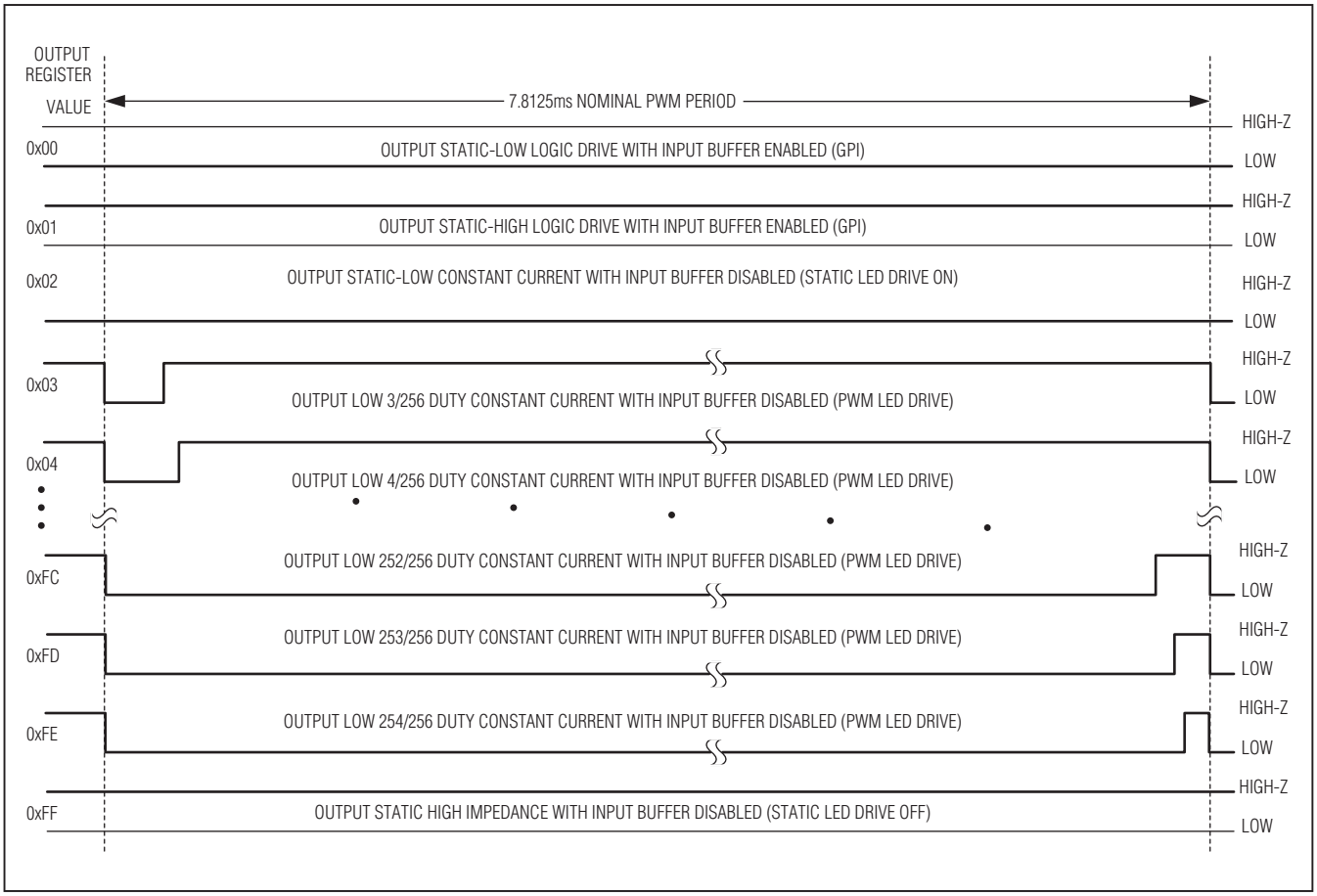


Figure 2. Static and PWM Constant-Current Waveforms

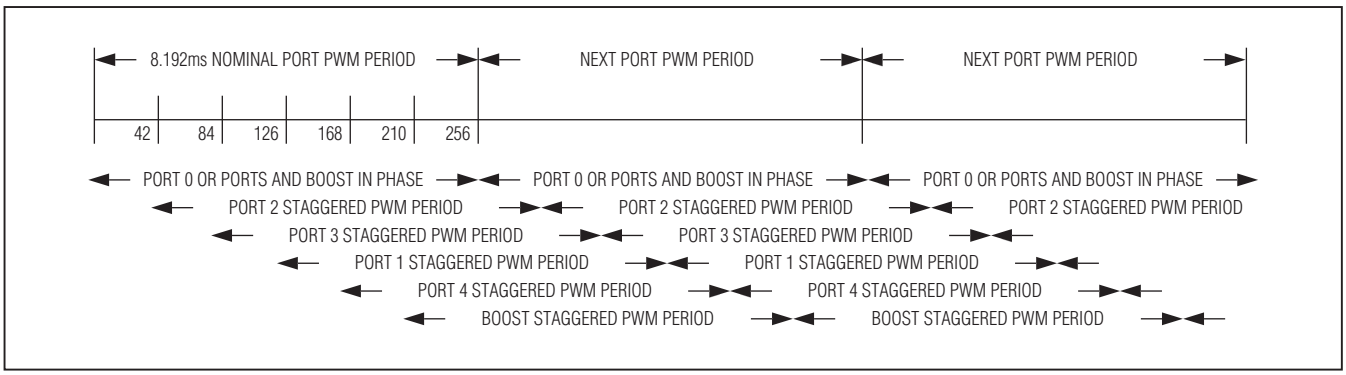


Figure 3. Staggered Port and Boost PWM Waveform

Table 10. Input Ports Register Format (0x0E, Read Only)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION
D7, D6, D5	Reserved	0	—
D4	P4	0	Port P4 is logic input low, or is not set as an input
		1	Port P4 is logic input high
D3	P3	0	Port P3 is logic input low, or is not set as an input
		1	Port P3 is logic input high
D2	P2	0	Port P2 is logic input low, or is not set as an input
		1	Port P2 is logic input high
D1	P1	0	Port P1 is logic input low, or is not set as an input
		1	Port P1 is logic input high
D0	P0	0	Port P0 is logic input low, or is not set as an input
		1	Port P0 is logic input high

Ports Configured as Inputs

Configure a port as a logic input by writing 0x01 to the port's output register (Table 7). Reading an input port register returns the logic levels from the I/O ports configured as a logic input (Table 10). The input port register returns logic 0 in the appropriate bit position for a port not configured as a logic input. The input ports' registers are read only. The MAX6948B ignores writes to the input ports register.

Standby Mode and Operating Current

Configuring all the ports as logic inputs or outputs (all output registers set to value 0x00 or 0x01) or high impedance (output register set to value 0xFF) puts the device into standby mode. Put the MAX6948B into standby mode for lowest supply current consumption.

Setting a port as a constant-current output increases the operating current (output register set to a value between 0x02 and 0xFE), even if a load is not applied to the port. The MAX6948B enables an internal current mirror to provide the accurate constant-current sink. Enabling the internal current mirror increases the device's supply current. Each output contains a gated mirror, which activates only when required.

In PWM mode, the current mirror turns on only for the duration of the output's on-time. This means that the operating current varies as constant-current outputs are turned on and off through the serial interface, as well as by the PWM intensity control.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Shutdown Mode

In shutdown mode, all ports configured as constant-current outputs (output register set to a value between 0x02 and 0xFE) switch off and become high impedance. Shutdown does not affect ports configured as logic inputs or outputs (output registers set to value 0x00 or 0x01) (Table 7). This means that any ports used for GPIOs are still operational in shutdown mode.

Put the MAX6948B into shutdown mode by setting the run bit (D0) = 0 in the configuration register (0x10) (Table 2). Exit shutdown by setting the run bit high through the serial interface or by using the reset-run option (see the *Reset-Run Option* section). Configure and control the MAX6948B normally through the serial interface in shutdown mode. All registers are accessible in shutdown mode. Entering and/or exiting shutdown mode does not change any register values.

Changing a port from static logic-low (0x00) or static logic-high (0x01) to a constant-current value (0x02 to 0xFE) in shutdown mode turns that output off (logic-high or high impedance) like any other constant-current outputs in shutdown. The new constant-current output starts just like any other constant-current outputs when exiting shutdown.

Changing a port from a constant-current value (0x02 to 0xFE) to static logic-low (0x00) or static logic-high (0x01) in shutdown causes that output to set to the value as a GPIO output. The new GPIO output is unaffected just like any other GPIO output when exiting shutdown.

Ramp-Up and Ramp-Down Controls

The MAX6948B provides controls that allow the output currents to ramp down into shutdown (ramp-down) and ramp up again out of shutdown (ramp-down) (Figures 4, 5). Ramp-down comprises a programmable hold-off delay that maintains the outputs at full current for a time before the programmed ramp-down time. After the hold-off delay, the output currents ramp down.

The ramp-down register sets the hold-off and ramp-down times and allows disabling of hold-off and ramp-down (zero delay), if desired (Table 11). The ramp-up register sets the ramp-up time and allows disabling of ramp-up (zero delay), if desired (Table 12). The configuration register contains three status bits that identify the condition of the MAX6948B, hold-off, ramp-down, or ramp-up (Table 2). The configuration register also enables or disables ramp-up. One write command to the configuration register puts the device into shutdown (using hold-off and ramp-down settings in the ramp-down register) and one read command to the configuration register determines whether the reset run is enabled for restart, and whether the MAX6948B is currently in ramp-up or ramp-down mode. Reset run needs to be used with ramp-up for it to work properly.

Ramp-up and ramp-down use the PWM clock for timing. The internal oscillator always runs during a fade sequence, even if none of the ports uses PWM.

The ramp-up and ramp-down circuit operates a 3-bit DAC. The DAC adjusts the internal current reference used to set the constant-current outputs in a similar manner to the global-current register (Table 8). The MAX6948B scales the master-current reference to have all output constant-current and PWM settings adjust at the same ratio with respect to each other. This means the LEDs always fade at the same rate even if with different intensity settings. The boost circuit does not use the 3-bit DAC. During ramp-down, the boost circuit remains at its programmed output until it shuts off completely at the end of the ramp-down period. The boost circuit turns on completely at the beginning of the ramp-up sequence.

The maximum port output current set by the global-current register (Table 8) also sets the point during ramp-down that the current starts falling, and the point during ramp-up that the current stops rising. Figure 7 shows the ramp waveforms that occur with different global-current register settings.

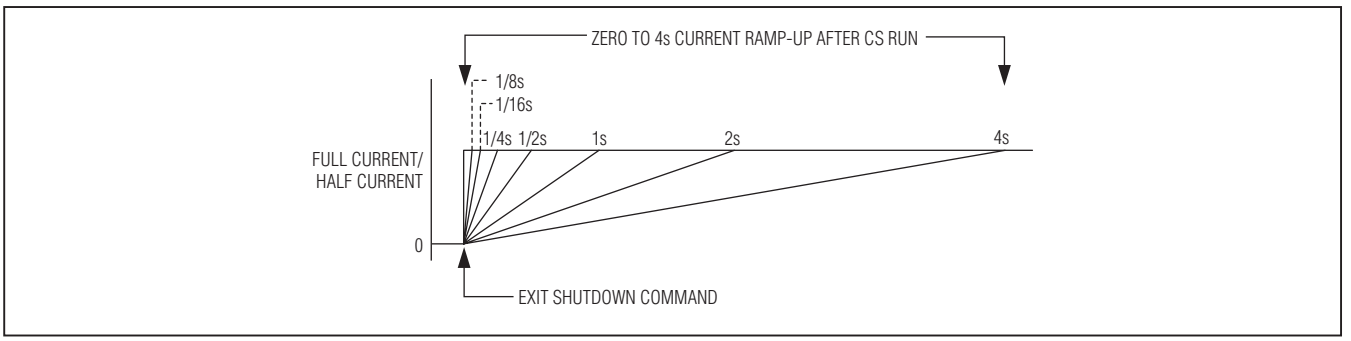


Figure 4. Ramp-Up Behavior

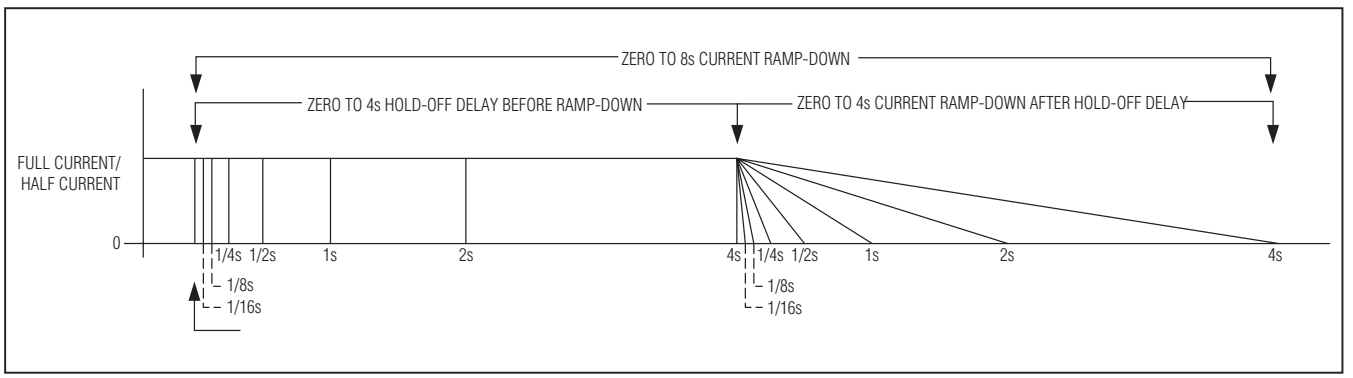


Figure 5. Hold-Off and Ramp-Down Behavior

Table 11. Port Ramp-Down Register Format (0x11)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED		HOLD-OFF			RAMP-DOWN		
Immediately shuts down after hold-off delay	X	X	X	X	X	0	0	0
0.0655s ramp-down from full current after hold-off delay	X	X	X	X	X	0	0	1
0.131s ramp-down from full current after hold-off delay	X	X	X	X	X	0	1	0
0.262s ramp-down from full current after hold-off delay	X	X	X	X	X	0	1	1
0.524s ramp-down from full current after hold-off delay	X	X	X	X	X	1	0	0
1.049s ramp-down from full current after hold-off delay	X	X	X	X	X	1	0	1
2.097s ramp-down from full current after hold-off delay	X	X	X	X	X	1	1	0

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Table 11. Port Ramp-Down Register Format (0x11) (continued)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED		HOLD-OFF			RAMP-DOWN		
4.164s ramp-down from full current after ramp-down delay	X	X	X	X	X	1	1	1
Zero ramp-down delay before fade-off	X	X	0	0	0	X	X	X
0.0655s ramp-down delay before fade-off	X	X	0	0	1	X	X	X
0.131s ramp-down delay before fade-off	X	X	0	1	0	X	X	X
0.262s ramp-down delay before fade-off	X	X	0	1	1	X	X	X
0.524s ramp-down delay before fade-off	X	X	1	0	0	X	X	X
1.049s ramp-down delay before fade-off	X	X	1	0	1	X	X	X
2.097s ramp-down delay before fade-off	X	X	1	1	0	X	X	X
4.164s ramp-down delay before fade-off	X	X	1	1	1	X	X	X
Power-up default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

X = Don't care.

Table 12. Port Ramp-Up Register Format (0x12)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED					RAMP-UP		
Immediately starts up	X	X	X	X	X	0	0	0
0.0655s ramp-up to full current	X	X	X	X	X	0	0	1
0.131s ramp-up to full current	X	X	X	X	X	0	1	0
0.262s ramp-up to full current	X	X	X	X	X	0	1	1
0.524s ramp-up to full current	X	X	X	X	X	1	0	0
1.049s ramp-up to full current	X	X	X	X	X	1	0	1
2.097s ramp-up to full current	X	X	X	X	X	1	1	0
4.164s ramp-up to full current	X	X	X	X	X	1	1	1
Power-up default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

X = Don't care.

$\overline{RST}$ Input

The active-low $\overline{RST}$ input operates as a reset that voids any current I²C transaction involving the MAX6948B, forcing the device into the I²C STOP condition. Use the D6 bit in the configuration register (Table 2) to configure $\overline{RST}$ to reset all the internal registers to the power-on-reset state (Table 3). The $\overline{RST}$ input is overvoltage tolerant to 5.5V.

The MAX6948B ignores all I²C bus activity while $\overline{RST}$ remains low. The device uses this feature to minimize supply current in power-critical applications by effectively disconnecting the MAX6948B from the bus during idle periods. $\overline{RST}$ also operates as a bus multiplexer, allowing multiple devices to use the same I²C slave address. Drive only one MAX6948B $\overline{RST}$ input high at any time to use $\overline{RST}$ as a bus multiplexer.

The MAX6948B features a reset-run option. Taking the $\overline{RST}$ input high brings the driver out of shutdown in addition to its normal function of enabling the device's I²C interface.

Reset-Run Option

The MAX6948B features a reset-run option enabling $\overline{RST}$ to bring the driver out of shutdown, in addition to its normal function of enabling the MAX6948B's I²C interface. This provides an alternative method of bringing the driver out of shutdown to writing to the configuration register through the serial interface. The reset-run timing uses the internal PWM clock.

After enabling the reset-run option, the MAX6948B uses the rising edge on $\overline{RST}$, followed by no I²C interface activity to the MAX6948B for 128 to 129 periods of the GPIO PWM clock (32kHz typ) to trigger the reset-run option. If this timeout period elapses without the MAX6948B acknowledging an I²C transaction, the device sets the run bit (D0) in the configuration register and brings itself out of shutdown, activating any programmed ramp-up. If $\overline{RST}$ pulses high for less than this timeout period to trigger a reset run, the MAX6948B ignores the pulse and continues to wait for a suitable trigger.

Cancel the reset-run trigger by transmitting an I²C communication to the MAX6948B before the timeout period elapses. The trigger cancels when the MAX6948B acknowledges the I²C transaction and requires sending at least the MAX6948B's I²C slave address. The minimum timeout period is equal to 4ms. The minimum I²C clock speed that guarantees a successful start bit and 8 data bits (9 bits total) within the minimum timeout period is 9/4ms equal to 2.25kHz. Canceling the reset-run trigger clears the reset-run bit (D1) in the configuration register, disabling reset run. The run bit (D0) in the configuration register remains cleared and the driver remains in shutdown.

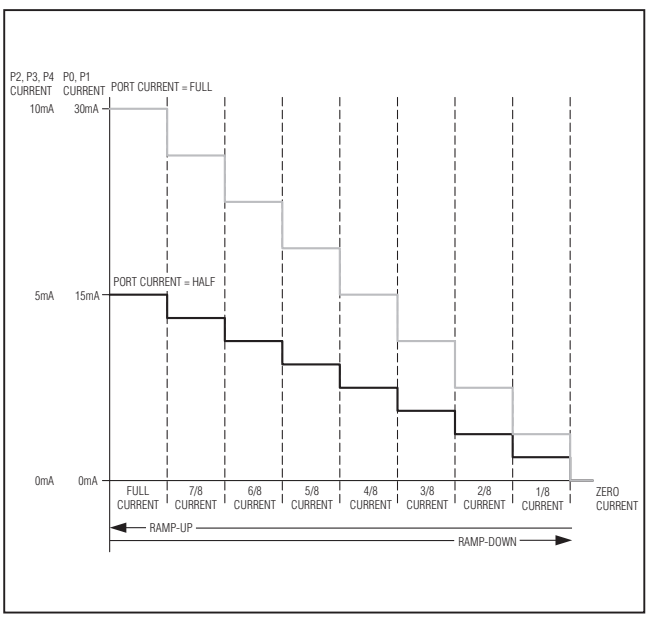


Figure 6. Output Fade DAC (Global Current = 0x07)

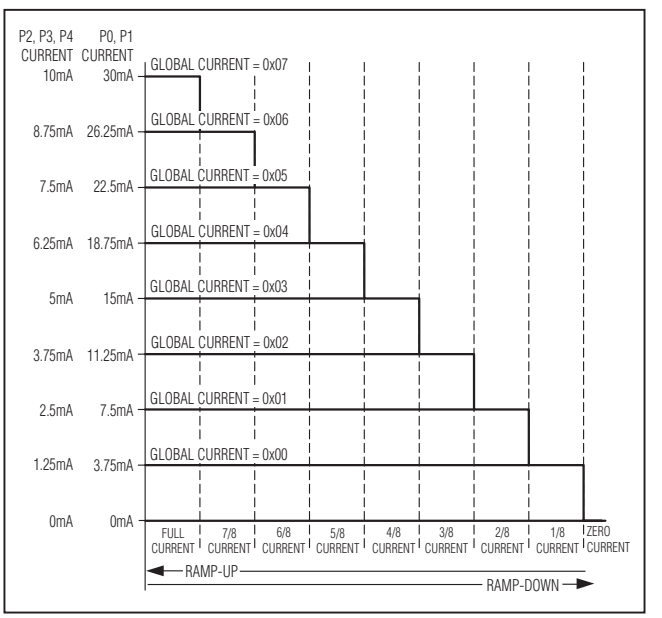


Figure 7. Global Current Modifies Ramp-Down Behavior

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Serial Interface

Figure 8 shows the 2-wire serial-interface timing details.

Serial Addressing

The MAX6948B operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6948B and generates the SCL clock that synchronizes the data transfer.

The MAX6948B's SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The MAX6948B's SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 9) sent by a master, followed by the MAX6948B 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 10). The data on SDA must remain stable while SCL is high.

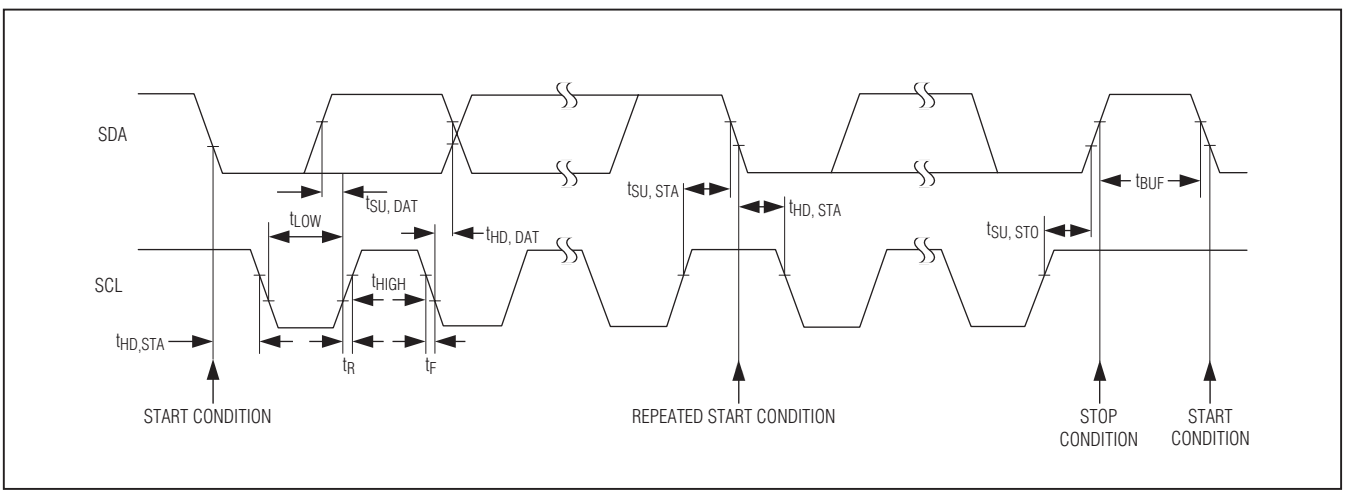

Figure 8. 2-Wire Serial-Interface Timing Details

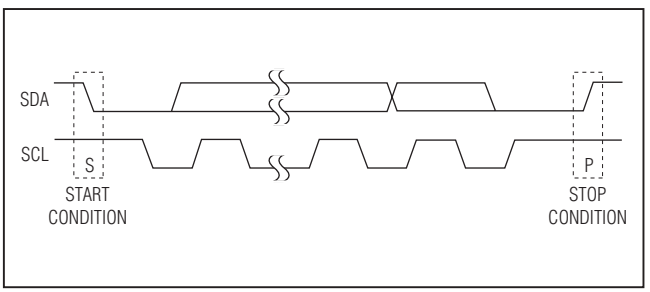

Figure 9. START and STOP Conditions

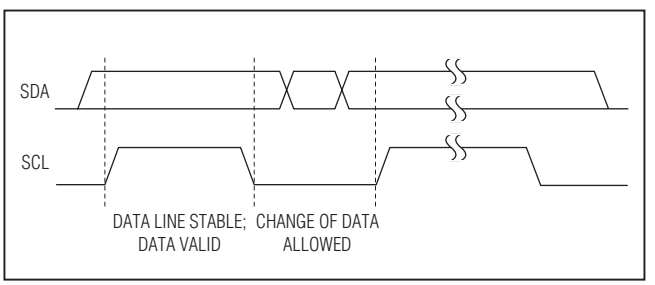

Figure 10. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 11), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, and therefore the SDA line is stable-low during the high period of the clock pulse. When the master is transmitting to the MAX6948B, the MAX6948B generates the acknowledge bit because the MAX6948B is the recipient. When the MAX6948B is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

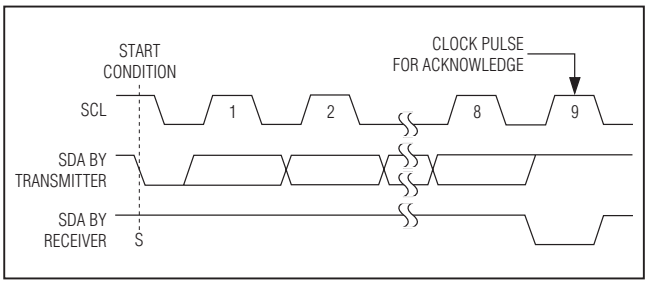

Figure 11. Acknowledge

Slave Addresses

The MAX6948B has a 7-bit long slave address (Figure 12). The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

Five bits (A6, A5, A4, A2, and A1), of the MAX6948B slave address are always 1, 0, 0, 0, and 0, respectively. Slave address bits A7 and A3 correspond, by the matrix in Table 13, to the states of the device address input AD0, and A0 corresponds to the R/$\overline{W}$ bit. The AD0 input can be connected to any of four signals: GND, V_{DD}, SDA, or SCL, giving four possible slave-address pairs, allowing up to four MAX6948B devices to share the bus. Because SDA and SCL are dynamic signals, care must be taken to ensure that AD0 transitions no sooner than the signals on SDA and SCL.

The MAX6948B monitors the bus continuously, waiting for a START condition followed by its slave address. When the MAX6948B recognizes its slave address, it acknowledges and is then ready for continued communication.

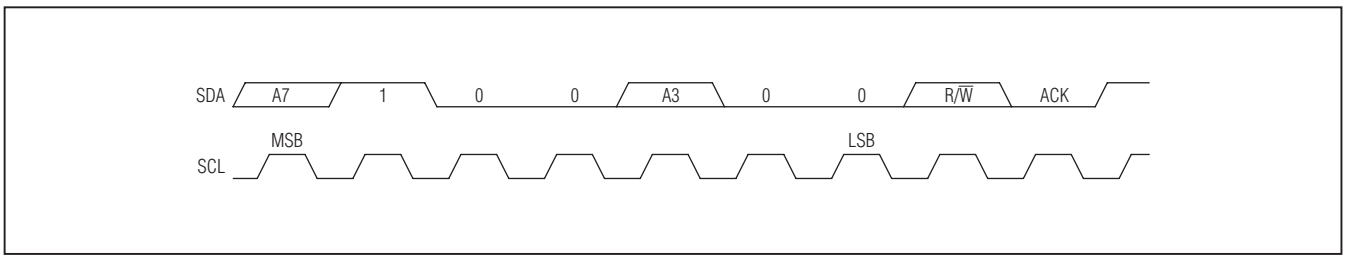

Figure 12. Slave Address

Table 13. MAX6948B Slave Address Map

PIN AD0	DEVICE ADDRESS							
	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	0	0	0	0	0	R/$\overline{W}$
V_{DD}	0	1	0	0	1	0	0	R/$\overline{W}$
SCL	1	1	0	0	0	0	0	R/$\overline{W}$
SDA	1	1	0	0	1	0	0	R/$\overline{W}$

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Message Format for Writing the LED Driver

A write to the MAX6948B comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX6948B is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the MAX6948B takes no further action (Figure 13) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6948B selected by the command byte (Figure 14).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6948B internal registers because the command-byte address generally autoincrements (Table 1).

Message Format for Reading

The MAX6948B is read using the MAX6948B's internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 1). Thus, a read is initiated by first configuring the MAX6948B's command byte by performing a write (Figure 13). The master can now read n consecutive bytes from the MAX6948B, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command-byte address is generally autoincremented after the write (Figure 15, Table 1).

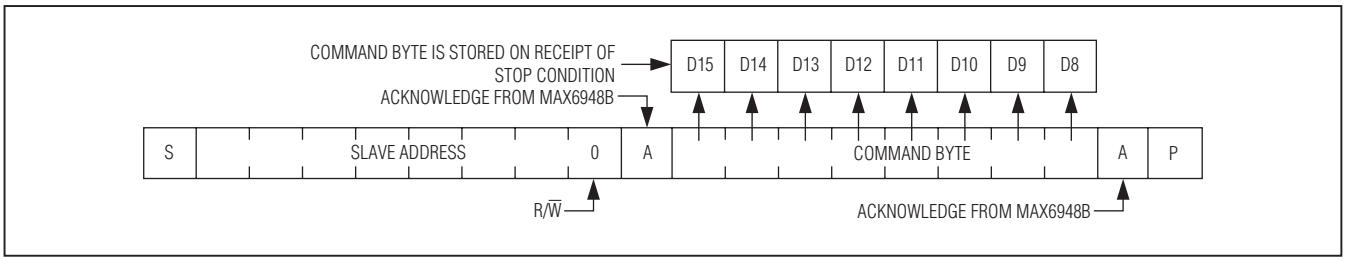

Figure 13. Command Byte Received

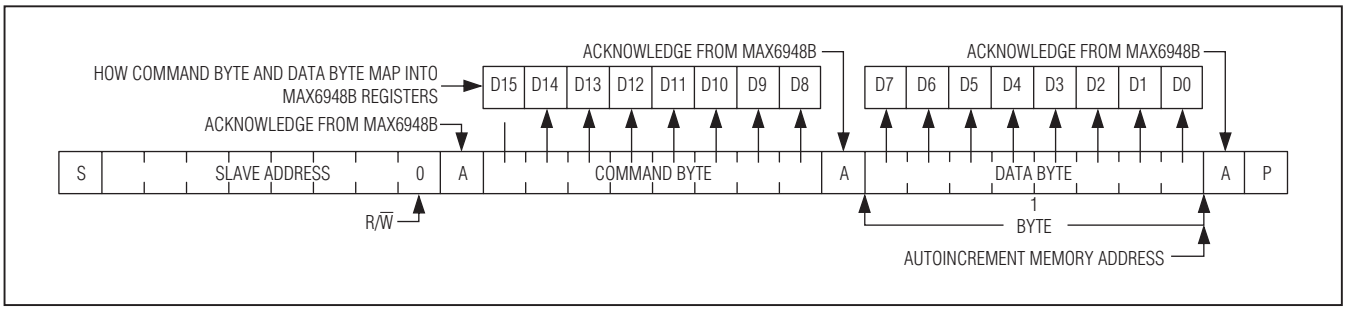

Figure 14. Command and Single Data Byte Received

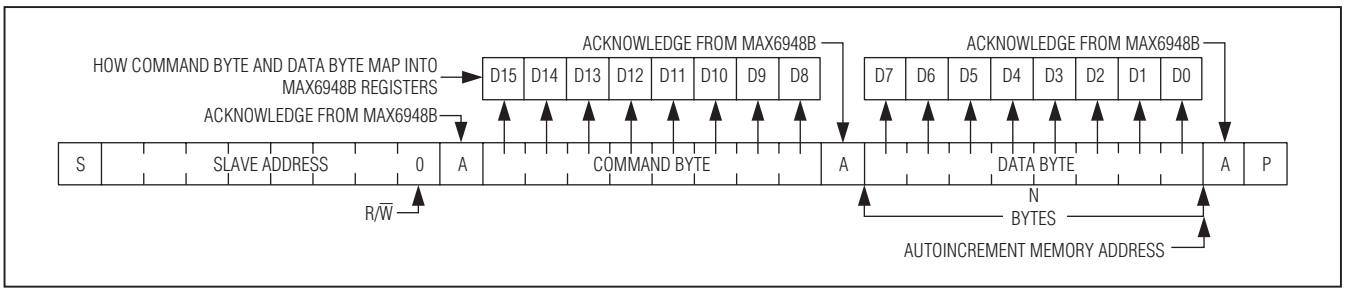

Figure 15. N Data Bytes Received

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Operation with Multiple Masters

When the MAX6948B is operated on a 2-wire interface with multiple masters, a master reading the MAX6948B uses a repeated start between the write that sets the MAX6948B's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX6948B's address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX6948B's address pointer, master 1's read can be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the MAX6948B to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX6948B generally increments after each data byte is written or read (Table 1). Autoincrement only works when doing a burst read or write.

Applications Information

Inductor Selection

The MAX6948B is optimized for a 10µH inductor, although larger or smaller inductors can be used. Using a smaller inductor results in discontinuous-current-mode operation over a larger range of output power, whereas use of a larger inductor results in continuous conduction for most of the operating range.

To prevent core saturation, ensure that the inductor's saturation current rating exceeds the peak inductor current for the application. For larger inductor values and continuous conduction operation, calculate the worst-case peak inductor current with the following formula:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MAX)}} + \frac{V_{IN(MIN)} \times 0.5\mu s}{2 \times L}$$

Otherwise, for small values of L in discontinuous conduction operation, I_{PEAK} is 860mA (typ). Table 14 provides a list of recommended inductors.

Capacitor Selection

The typical input capacitor value is 2.2µF and the typical output capacitor is 0.22µF. Higher value capacitors can reduce input and output ripple, but at the expense of size and higher cost. For best operation, use ceramic X5R or X7R dielectric capacitors. Generally, ceramic capacitors with smaller case sizes have poorer DC bias characteristics than larger case sizes for a certain capacitance value. Select the capacitor that yields the best trade-off between case size and DC bias characteristics.

Diode Selection

The high switching frequency of the MAX6948B demands a high-speed rectification diode for optimum efficiency. A Schottky diode is recommended due to its fast recovery time and low forward-voltage drop. Ensure that the diode's average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse-breakdown voltage must exceed V_{OUT}.

Compensation Network Selection

The step-up converter uses an external compensation network from COMP to GND to ensure stability. For 5 or 6 WLEDs, choose $C_{COMP} = C_{OUT}/10$ for optimal transient response.

Port Input and I²C Interface Logic Voltages

The MAX6948B I²C supply (V_{DD}) accepts voltages from 1.7V up to the boost-converter input (V+). V_{DD} determines the I²C interface (SDA, SCL), I²C slave-address select input (AD0), and reset input ($\overline{RST}$) logic voltages. The five I/O ports P0–P4 are overvoltage protected to 5.5V independent of V_{DD} or V+. This allows the MAX6948B to operate from one supply voltage, such as 3.3V, while driving some of the five I/Os as inputs from a different logic level, such as 5V.

Table 14. Recommended Inductors

VENDOR PART NUMBER	L (µH)	DCR (mΩ)	I_{SAT} (A)	CASE SIZE (mm)
TOKO 1069AS-220M	22	570	0.47	3 x 3 x 1.8
TOKO 1098AS-100M	10	290	0.75	2.8 x 3 x 1.2

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Driving LEDs into Brownout

The MAX6948B correctly regulates the constant-current outputs, provided there is a minimum voltage drop across the port output. This port output voltage is the difference between the load (typically LED) supply and the load voltage drop (LED forward voltage). If the LED supply drops so that the minimum port output voltage is not maintained, the driver output stages brownout and the load current falls. The minimum port voltage is approximately 0.25V at 15mA sink current and approximately 0.3V at 30mA sink current (ports P0, P1) and 0.39V at 5mA sink current and approximately 0.4V at 10mA sink current (ports P2, P3, P4).

Operating the LEDs directly from a battery supply can cause brownouts. For example, the LED supply voltage is a single rechargeable lithium-ion battery with a maximum terminal voltage of 4.2V on charge, 3.4V to 3.7V most of the time, and down to 3V when discharged. In this scenario, the LED supply falls significantly below the brownout point when the battery is at end-of-life voltage (3V).

Figure 16 shows the typical current sink by a King Bright AA3020ARWC/A white LED as the LED supply voltage is varied from 2.5V to 5.5V. The LED currents shown are for ports programmed for 10mA and 30mA constant current, swept over a 2.5V to 5.5V LED supply voltage range. It can be seen that the LED forward voltage falls with current, allowing the LED current to fall gracefully, not abruptly, in brownout. In practice, the LED current drops to 11mA to 12.5mA at a 3V LED supply voltage; this is acceptable performance at end-of-life in many backlight applications.

Output-Level Translation

The open-drain output architecture allows the ports to level translate the outputs to higher or lower voltages than the MAX6948B supply (V_{DD}). Use an external pullup resistor on any output to convert the high-impedance, logic-high condition to a positive voltage level. Connect the resistor to any voltage up to 5.5V. When using a pullup on a constant-current output, select the resistor value to sink no more than a few hundred µA in logic-low condition. This ensures that the current-sink output saturates close to GND. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to improve noise immunity in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Using Stagger with Fewer Ports

The stagger option, when selected, applies to all ports configured as constant-current outputs. The PWM cycles are separated to six evenly spaced start positions (Figure 3). Optimize phasing when using some of the ports as constant-current outputs by allocating the ports with the most appropriate start positions. In general, choose the ports that spread the PWM start positions as evenly as possible. This optimally spreads out the current demand from the ports' load supply.

Generating a Shutdown/Run Output

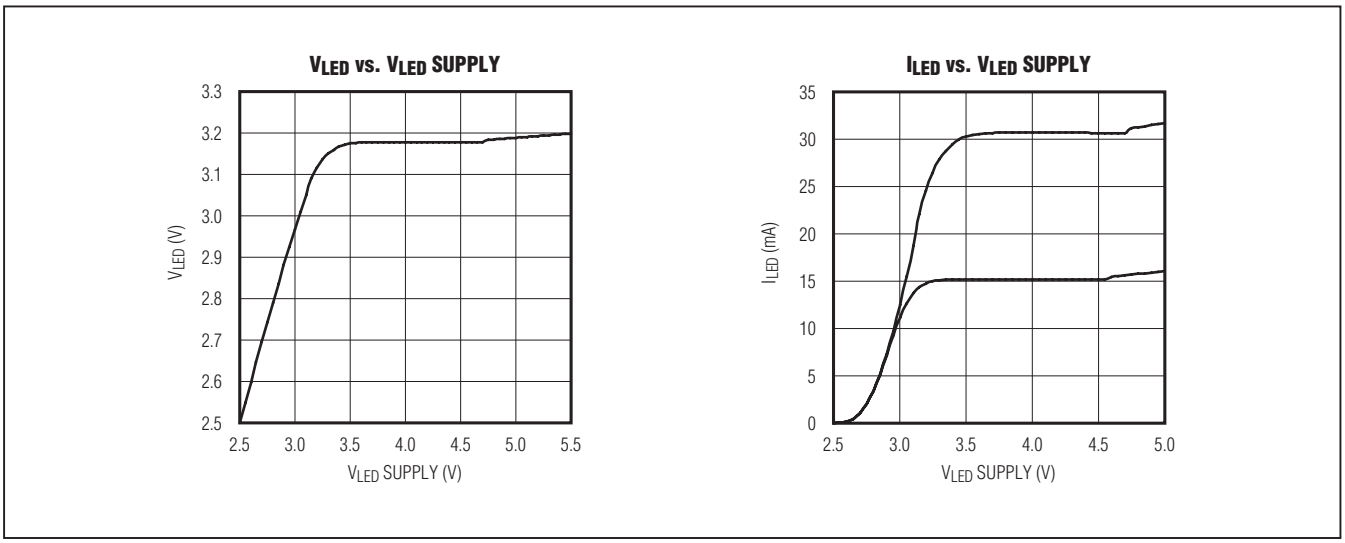

Figure 16. LED Brownout

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

The MAX6948B can use an I/O port to automatically generate a shutdown/run output. The shutdown/run output is active-low when the MAX6948B is in run mode, hold-off, ramp-down, or ramp-up, and goes high automatically when the device finally enters shutdown after ramp-down. Programming the port's output register to value 0x02 puts the output into static constant-current mode (Table 7). Program the port's output current to half current (Table 9) to minimize operating current. Connect a 220kΩ pullup resistor to this port.

In run mode, the output port goes low, approaching 0V, as the port's static constant current saturates trying to sink a higher current than the 220kΩ pullup resistor can source.

In shutdown mode, the output goes high impedance together with any other constant-current outputs. This output remains low during ramp-up and ramp-down sequences because the current drawn by the 220kΩ pullup resistor is much smaller than the available output constant current, even at the lowest fade-current step.

Driving Load Currents Higher than 30mA

The MAX6948B can drive loads needing more than 30mA, like high-current white LEDs, by paralleling outputs. For example, consider a white LED that requires 90mA. Drive this LED using the ports P0–P4 connected in parallel (shorted together). Configure all of the five ports for full current (2 x 30mA + 3 x 10mA) to meet the 90mA requirement. Control the five ports simultaneously with one write access using register 0x0C (Table 1). Note that because the output ports are current limiting, they do not need to switch simultaneously to ensure safe current sharing.

Power-Supply Considerations

V+ operates with a 2.7V to 5.5V power-supply voltage. Bypass V+ to GND with a 2.2µF or higher ceramic capacitor as close as possible to the device. V_{DD} operates with a 1.7V to V+ power-supply voltage. Bypass V_{DD} to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device.

PCB Layout Considerations

Due to fast switching waveforms and high-current paths, careful PCB layout is required. Minimize trace lengths between the IC and the inductor, the diode, the input capacitor, and the output capacitor. Minimize trace lengths between the input and output capacitors and the MAX6948B GND terminal, and place input and output capacitor grounds as close together as possible. Use separate power-ground and analog-ground copper areas, and connect them together at the output-capacitor ground. Keep traces short, direct, and wide. Keep noisy traces, such as the LX node trace, away from sensitive analog circuitry. For improved thermal performance, maximize copper area of the LX and PGND traces. Refer to the MAX6948B EV kit data sheet for an example layout.

High-Efficiency PWM LED Driver with Boost Converter and Five Constant-Current GPIO Ports

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
25 WLP	B9-7 W252D2+1	**21-0453**