

2-Mbit (128K x 16) Static RAM

Features

- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive-A: -40°C to 85°C
 - Automotive-E: -40°C to 125°C
- **High speed: 55 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in standard Pb-free 44-pin TSOP Type II, Pb-free and non Pb-free 48-ball FBGA packages**

Functional Description^[1]

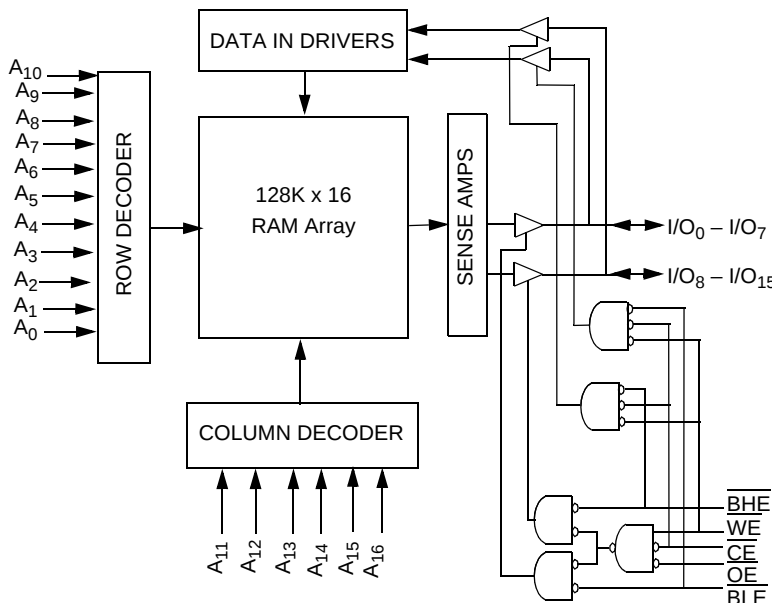
The CY62136VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ($\overline{CE}$ LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



PinConfigurations^[3]

TSOP II (Forward)
Top View

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	$\overline{OE}$
A ₀	5	40	BHE
$\overline{CE}$	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₆	18	27	A ₈
A ₁₅	19	26	A ₉
A ₁₄	20	25	A ₁₀
A ₁₃	21	24	A ₁₁
A ₁₂	22	23	NC

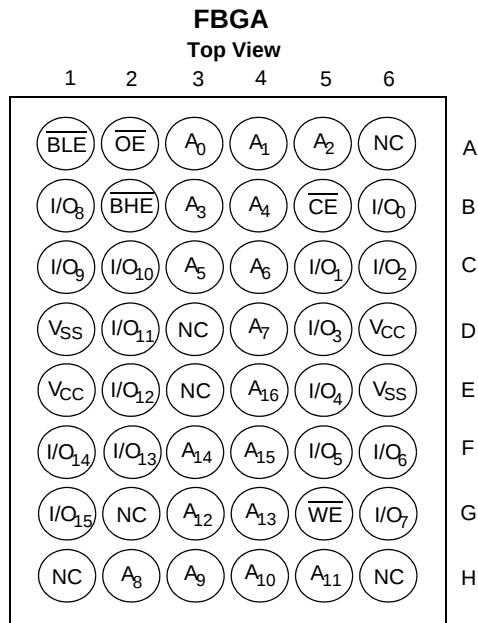
Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	V _{CC} Range (V)			Speed	Ranges	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
	Min	Typ. ^[2]	Max			Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62136VNLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				55	Automotive-A	7	20	1	15
				70	Industrial	7	15	1	15
				70	Automotive-A	7	15	1	15
				70	Automotive-E	7	20	1	20

Pin Configurations^[3]



Notes:

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.
3. NC pins are not connected on the die.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs

in High-Z State^[4] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[4] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature [T_A] ^[5]	V_{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7V$, $I_{OH} = -1.0$ mA	2.4			2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7V$, $I_{OL} = 2.1$ mA			0.4			0.4	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 3.6V$	2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V
V_{IL}	Input LOW Voltage	$V_{CC} = 2.7V$	-0.5		0.8	-0.5		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	Ind'I	-1	+1	-1		+1	μA
			Auto-A	-1	+1	-1		+1	μA
			Auto-E			-10		+10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	Ind'I	-1	+1	-1		+1	μA
			Auto-A	-1	+1	-1		+1	μA
			Auto-E			-10		+10	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ $V_{CC} = 3.6V$, $I_{OUT} = 0$ mA, CMOS Levels	Ind'I	7	20	7	15		mA
			Auto-A	7	20	7	15		
			Auto-E			7	20		
		$f = 1$ MHz	Ind'I	1	2	1	2		mA
			Auto-A	1	2	1	2		
			Auto-E			1	2		
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = f_{MAX}$	Ind'I		100			100	μA
			Auto-A		100			100	μA
			Auto-E					100	μA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	Ind'I	1	15	1	15		μA
			Auto-A	1	15	1	15		
			Auto-E			1	20		

Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

4. $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.

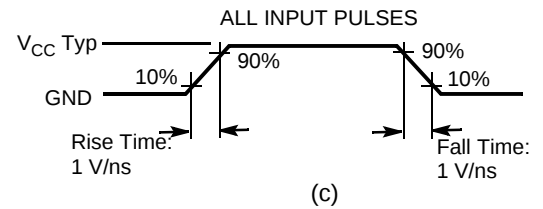
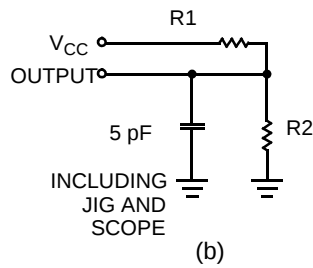
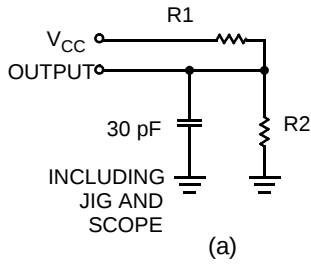
5. T_A is the "Instant-On" case temperature.

6. Tested initially and after any design or process changes that may affect these parameters.

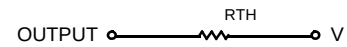
Thermal Resistance^[6]

Parameter	Description	Test Conditions	TSOPII	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		22	16	°C/W

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

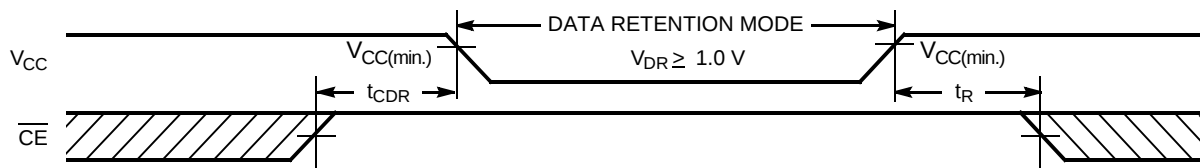


Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[9]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$,		0.5	7.5	μA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		70			ns

Data Retention Waveform



Note:

7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ ≥ 100 ms or stable at $V_{CC(min)}$ ≥ 100 ms.
8. No input may exceed $V_{CC} + 0.3V$

Switching Characteristics Over the Operating Range^[9]

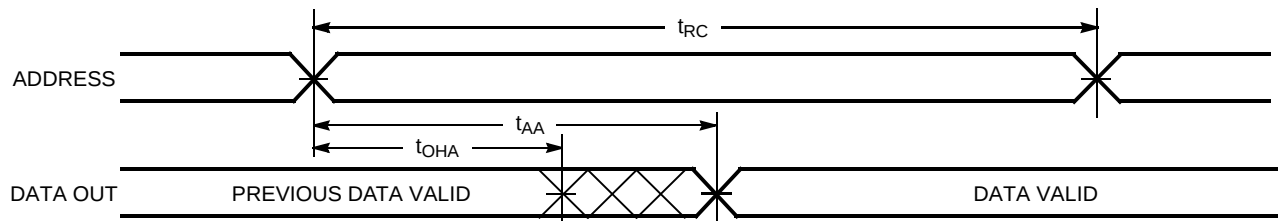
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[10]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[10, 11]		25		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low-Z ^[10]	10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High-Z ^[10, 11]		25		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
t _{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		25		35	ns
t _{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z ^[10, 11]	5		5		ns
t _{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z ^[12]		25		25	ns
Write Cycle ^[12, 13]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t _{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	50		60		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[10, 11]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[10]	5		10		ns

Notes:

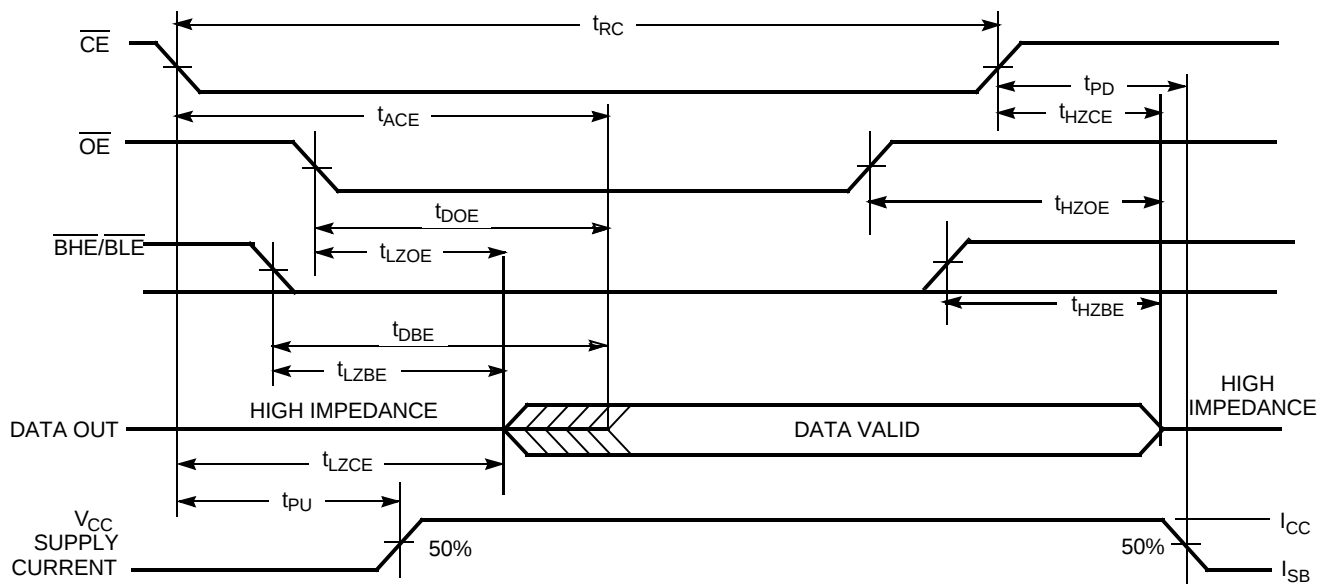
9. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Read Cycle No. 1^[14, 15]



Read Cycle No. 2^[15, 16]

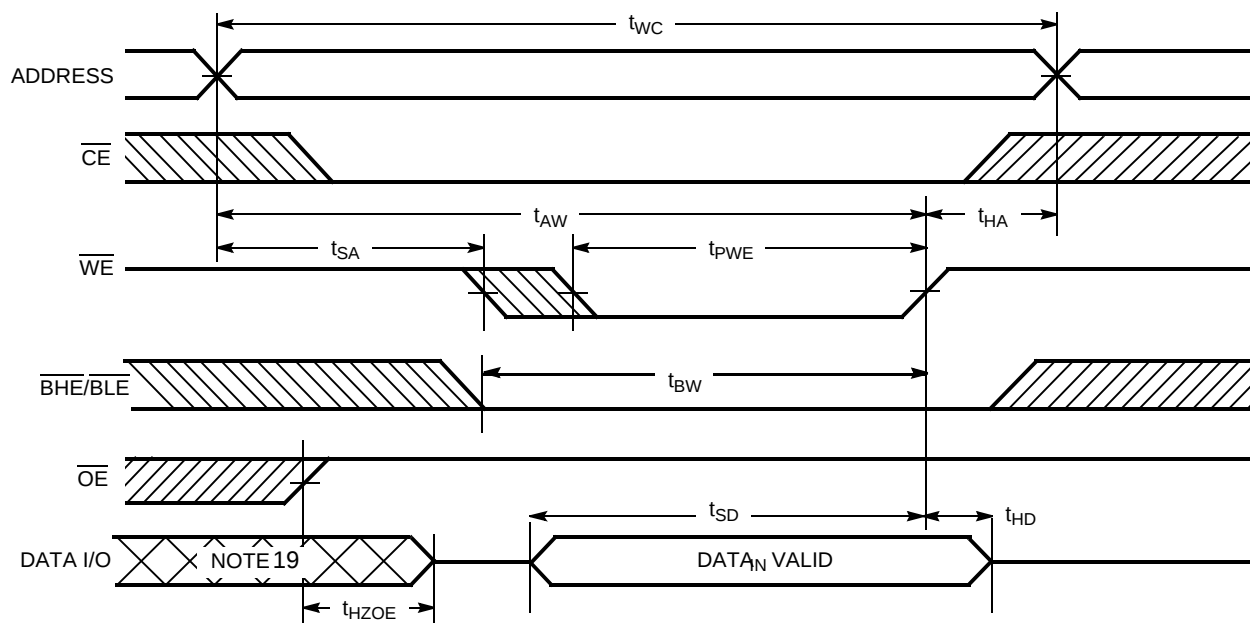


Notes:

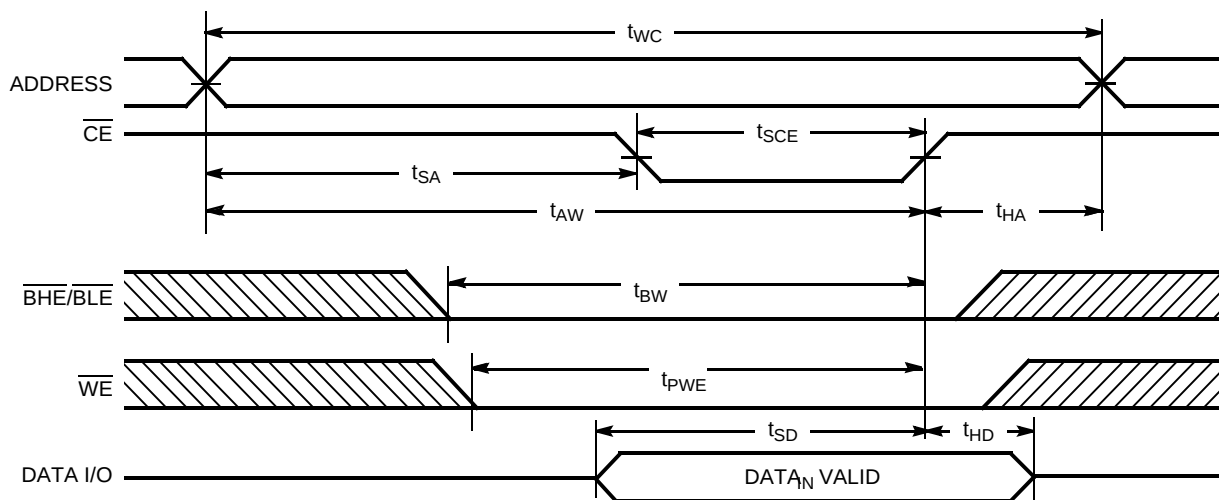
14. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)^[12, 17, 18]



Write Cycle No. 2 (CE Controlled)^[12, 17, 18]

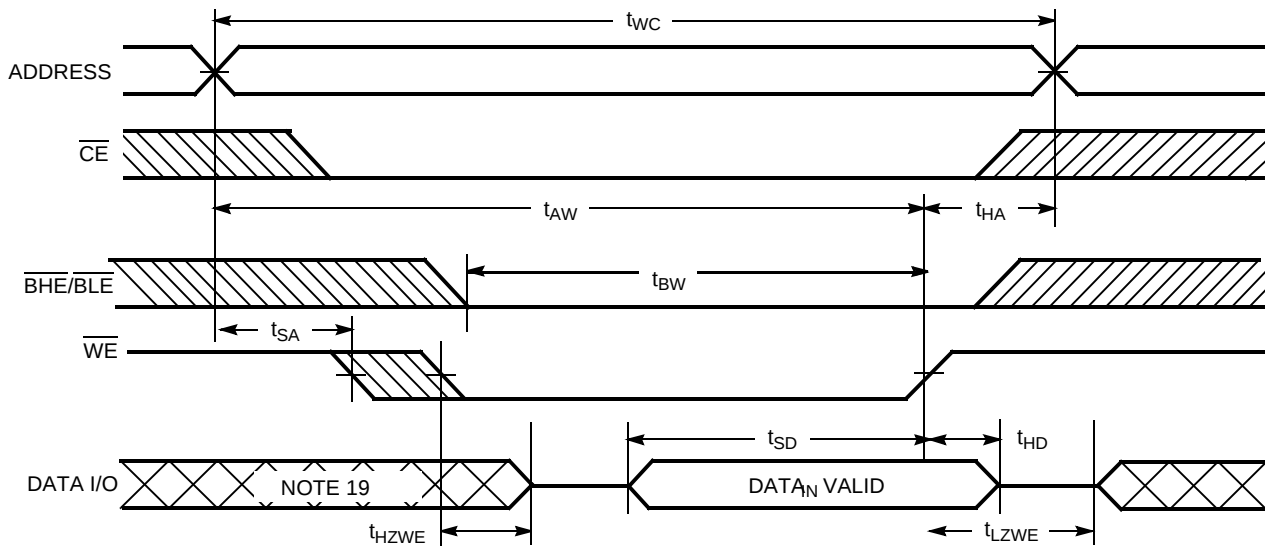


Notes:

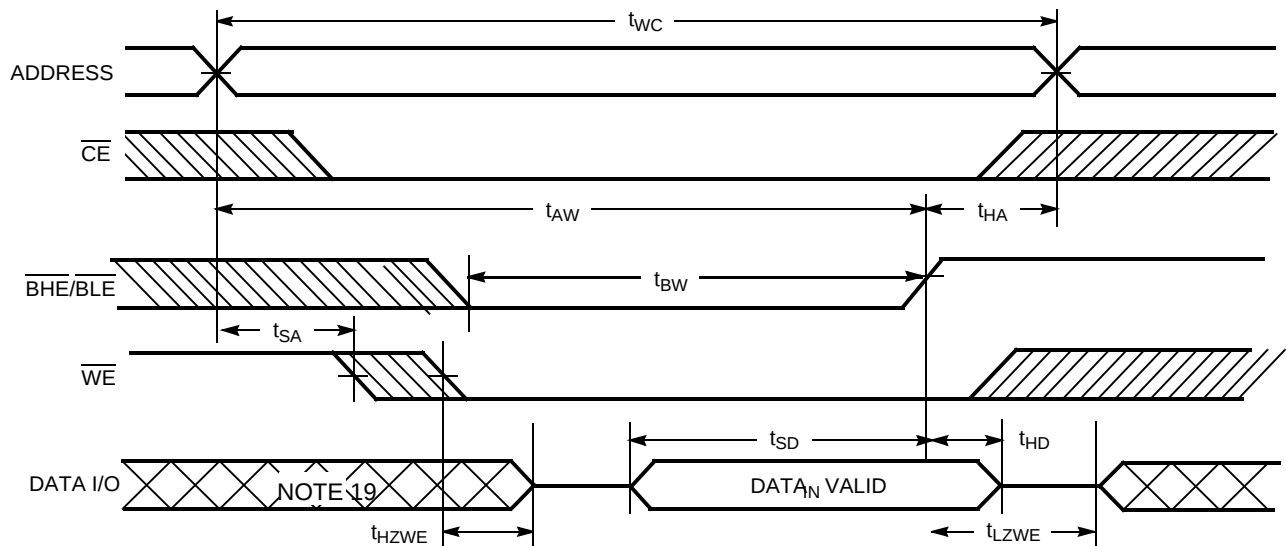
17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
18. If $\overline{CE}$ goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

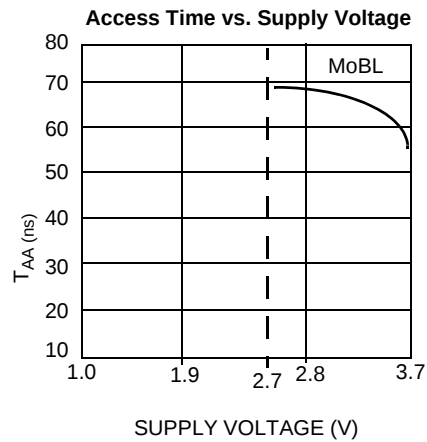
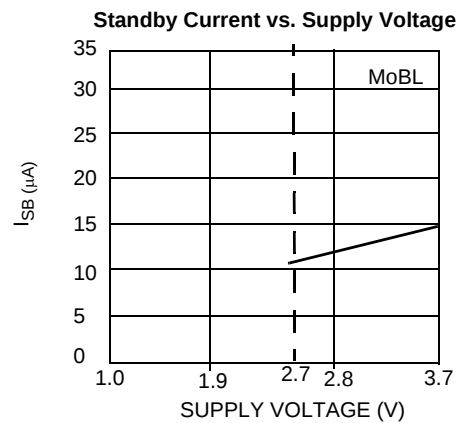
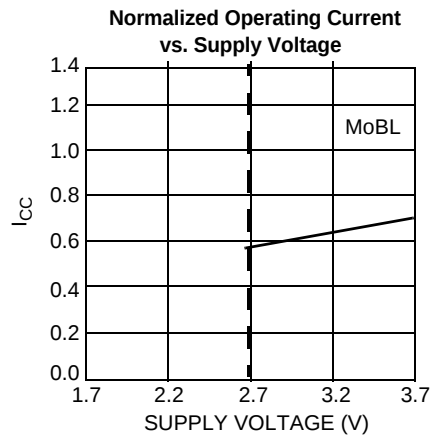
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[13, 18]



Write Cycle No. 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)^[19]



Typical DC and AC Characteristics



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High-Z	Read	Active (I_{CC})
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High-Z	Write	Active (I_{CC})

Ordering Information

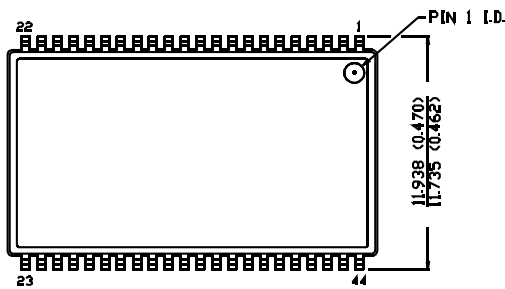
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62136VNLL-55ZXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial
	CY62136VNLL-55BAI	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA	
	CY62136VNLL-55ZSXA	51-85087	44-pin TSOP II (Pb-Free)	Automotive-A
70	CY62136VNLL-70ZXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial
	CY62136VNLL-70BAI	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA	
	CY62136VNLL-70BAXA	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA (Pb-Free)	Automotive-A
	CY62136VNLL-70ZSXA	51-85087	44-pin TSOP II (Pb-Free)	
	CY62136VNLL-70ZSXE	51-85087	44-pin TSOP II (Pb-Free)	Automotive-E

Please contact your local Cypress sales representative for availability of these parts

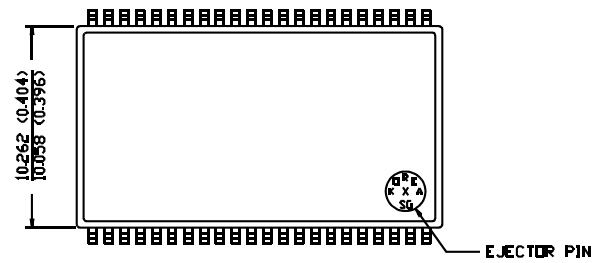
Package Diagrams

44-pin TSOP II (51-85087)

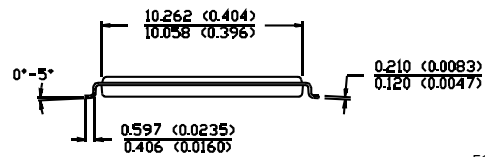
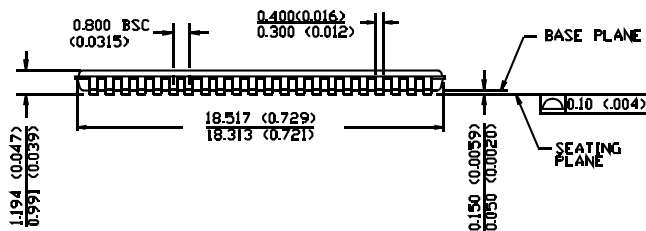
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



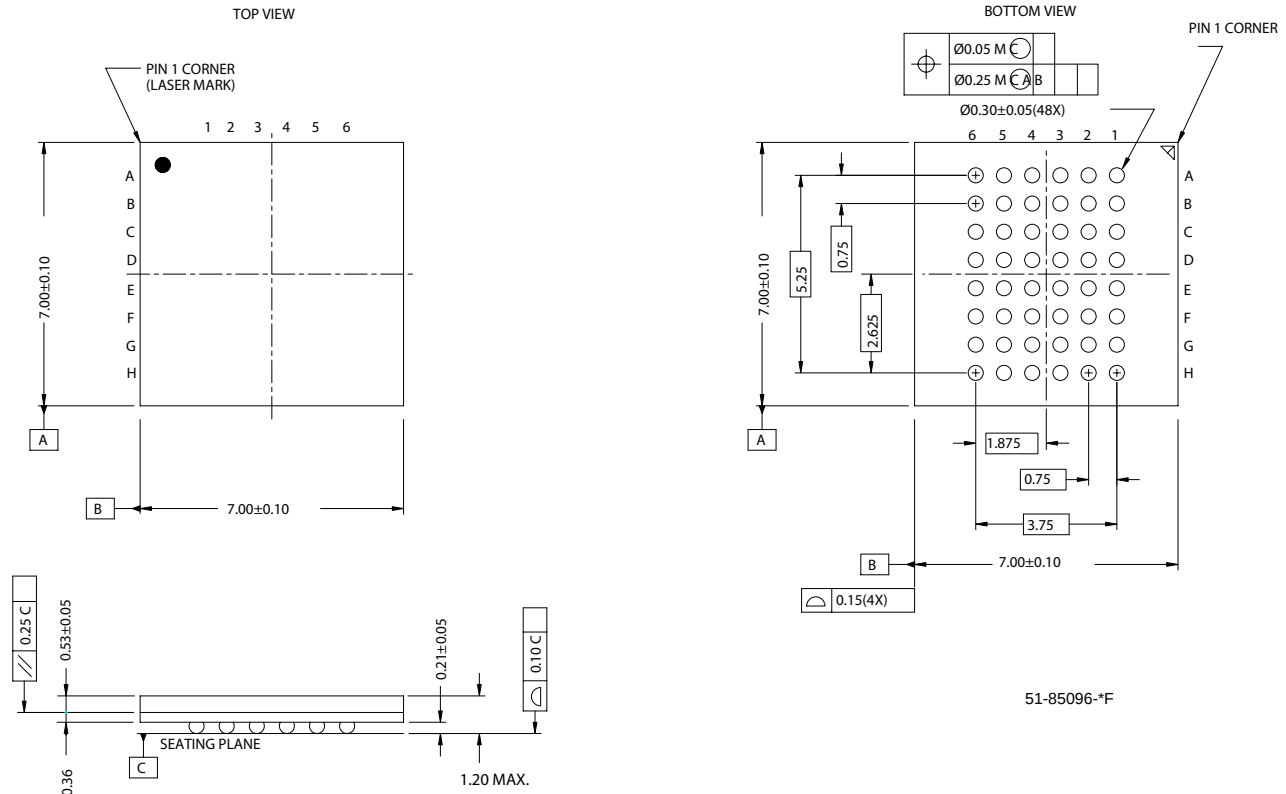
BOTTOM VIEW



51-85087-*A

Package Diagrams (continued)

48-Ball (7.00 mm x 7.00 mm) FBGA (51-85096)



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Document History Page

Document Title: CY62136VN MoBL [®] 2-Mbit (128K x 16) Static RAM Document Number: 001-06510				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426503	See ECN	RXU	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table