

August 1986 Revised March 2000

# DM74LS251 3-STATE 1-of-8 Line Data Selector/Multiplexer

## **General Description**

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled 3-STATE output. The strobe must be at a low logic level to enable these devices. The 3-STATE outputs permit direct connection to a common bus. When the strobe input is HIGH, both outputs are in a highimpedance state in which both the upper and lower transistors of each totem-pole output are OFF, and the output neither drives nor loads the bus significantly. When the strobe is LOW, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

#### **Features**

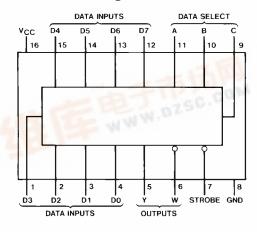
- 3-STATE version of DM74LS151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Maximum number of common outputs: 129
- Typical propagation delay time (D to Y): 17 ns
- Typical power dissipation: 35 mW

## **Ordering Code:**

Order Number	Package Number	Package Description
DM74LS251M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS251N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0,300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## **Connection Diagram**



### **Function Table**

	Inputs			Outputs		
	Select		Strobe	v	w	
С	В	Α	S		**	
X	X	X	Н	Z	Z	
L	L	L	L	D0	D0	
L	L	Н	L	D1	D1	
L	Н	L	L	D2	D2	
L	Н	Н	L	D3	D3	
Н	L	L	L	D4	D4	
Н	L	Н	L	D5	D5	
Н	Н	L	L	D6	D6	
Н	Н	Н	L	D7	D7	

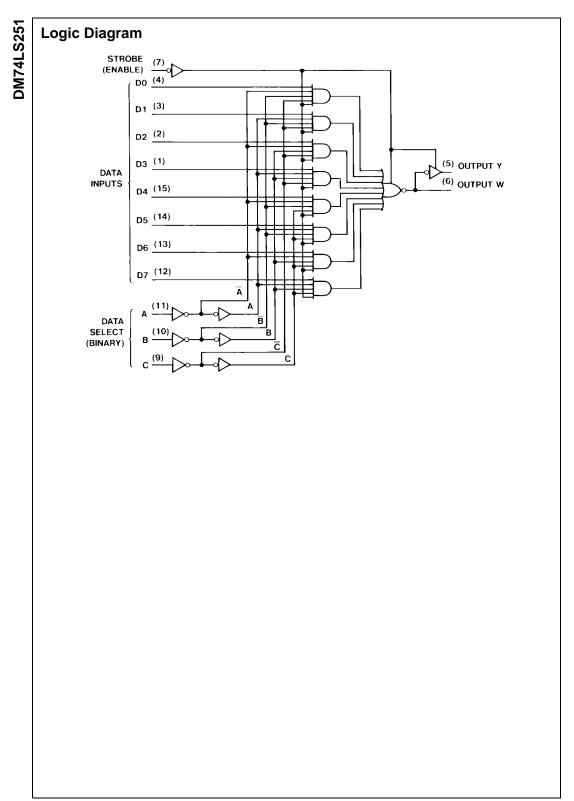
- H = HIGH Logic Leve
- L = LOW Logic Level
- X = Don't Care
- Z = High Impedance (OFF)
  D0, D1...D7 = The level of the respective D input

© 2000 Fairchild Semiconductor Corporation

www.fairchildsemi.com

WWW.DZS





## **Absolute Maximum Ratings**(Note 1)

7V Supply Voltage 7V Input Voltage Operating Free Air Temperature Range 0°C to +70°C  $-65^{\circ}C$  to  $+150^{\circ}C$ 

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## **Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
Гон	HIGH Level Output Current			-2.6	mA
I <sub>OL</sub>	LOW Level Output Current			24	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

#### **Electrical Characteristics**

Storage Temperature Range

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	HIGH Level	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	2.4	3.1		V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$	2.4	3.1		v
V <sub>OL</sub>	LOW Level	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max		0.25	0.5	0.5 V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		0.35	0.5	
		$I_{OL} = 12 \text{ mA}, V_{CC} = \text{Min}$		0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V			0.1	mA
I <sub>IH</sub>	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
I <sub>IL</sub>	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
I <sub>OZH</sub>	Off-State Output Current with	$V_{CC} = Max, V_O = 2.7V$			20	^
	HIGH Level Output Voltage Applied	$V_{IH} = Min, V_{IL} = Max$			20	μА
I <sub>OZL</sub>	Off-State Output Current with	$V_{CC} = Max, V_O = 0.4V$		-20	μА	
	LOW Level Output Voltage Applied	$V_{IH} = Min, V_{IL} = Max$			-20	μА
Ios	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	-20		-100	mA
I <sub>CC1</sub>	Supply Current	V <sub>CC</sub> = Max (Note 4)		6.1	10	mA
I <sub>CC2</sub>	Supply Current	V <sub>CC</sub> = Max (Note 5)		7.1	12	mA

Note 2: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

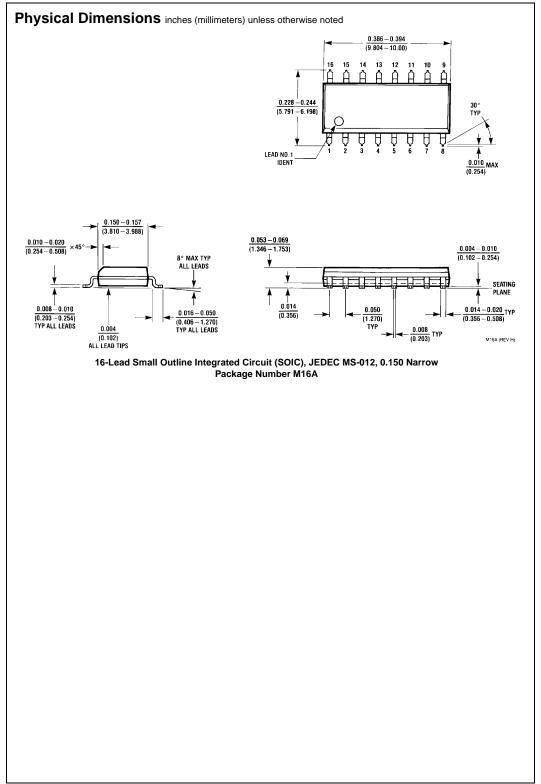
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

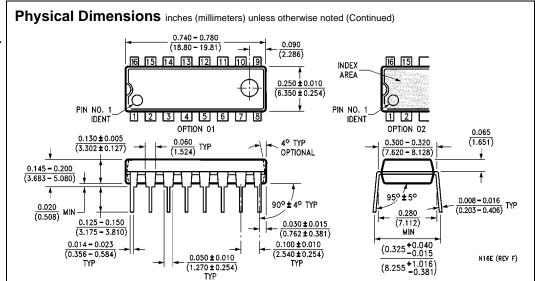
Note 4:  $I_{CC1}$  is measured with the outputs open, STROBE grounded, and all other inputs at 4.5V.

Note 5:  $I_{CC2}$  is measured with the outputs open and all inputs at 4.5V.

	5V and T <sub>A</sub> = 25°C	From (Input)	$R_L = 667\Omega$				Т
Symbol	Parameter	to (Output)	C <sub>L</sub> =	45 pF	C <sub>L</sub> =	C <sub>1</sub> = 150 pF	
			Min	Max	Min	Max	†
t <sub>PLH</sub>	Propagation Delay Time	A, B, C		45		53	
	LOW-to-HIGH Level Output	(4 Levels) to Y		45		53	
t <sub>PHL</sub>	Propagation Delay Time	A, B, C		45		53	
	HIGH-to-LOW Level Output	(4 Levels) to Y		45		53	
t <sub>PLH</sub>	Propagation Delay Time	A, B, C		22			n
	LOW-to-HIGH Level Output	(3 Levels) to W		33		38	
t <sub>PHL</sub>	Propagation Delay Time	A, B, C		33		42	n
	HIGH-to-LOW Level Output	(3 Levels) to W					
t <sub>PLH</sub>	Propagation Delay Time	D to V		00		0.5	1
	LOW-to-HIGH Level Output	D to Y		28		35	n
t <sub>PHL</sub>	Propagation Delay Time	D to V		28		38	ns
	HIGH-to-LOW Level Output	D to Y					
t <sub>PLH</sub>	Propagation Delay Time	D. W.	15			25	n
	LOW-to-HIGH Level Output	D to W		15			
t <sub>PHL</sub>	Propagation Delay Time	D 1- 10/		45		0.5	1
	HIGH-to-LOW Level Output	D to W		15		25	
t <sub>PZH</sub>	Output Enable Time to	Strobe to Y	4	45		60	n
	HIGH Level Output	Strobe to 1		40			
t <sub>PZL</sub>	Output Enable Time to	Otrob - to V		40		E4	n
	LOW Level Output	Strobe to Y		40		51	
t <sub>PHZ</sub>	Output Disable Time from	Strobe to Y		45			
	HIGH Level Output (Note 6)	Strope to 1		45			
t <sub>PLZ</sub>	Output Disable Time from	Strobe to Y		25			
	LOW Level Output (Note 6)	Strobe to 1		25			
t <sub>PZH</sub>	Output Enable Time to	Otrolio 4- 10/		07		40	
	HIGH Level Output	Strobe to W		27		40	
t <sub>PZL</sub>	Output Enable Time to	Otrob - 4- 10/		40		47	1
1 <u>4</u> L	LOW Level Output	Strobe to W		40		47	
t <sub>PHZ</sub>	Output Disable Time from	Otrob a ta M'				<u> </u>	1
THE	HIGH Level Output (Note 6)	Strobe to W		55			
t <sub>PLZ</sub>	Output Disable Time from					<u> </u>	†
	LOW Level Output (Note 6)	Strobe to W		25			1

**Note 6:** C<sub>L</sub> = 5 pF





16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com