

查询"CS9LTSK"供应商

## CS9L/CSPL SERIES: ULTRA HF CLOCK OSCILLATOR, PECL, +3.3 VDC or +2.5VDC

**DESCRIPTION:** A crystal controlled, high frequency, highly stable oscillator, adhering to Positive Emitter Coupled Logic (PECL) Standards and fundamental crystal or analog multiplication technologies. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

### APPLICATIONS AND FEATURES:

- Infiniband; Fiber Channel; SATA; 10GbE; Network Processors; SOHO Routing; Switches;
- Common Frequencies: 150 MHz; 156.25 MHz; 155.52 MHz; 161.1328 MHz; 212.5MHz; 312.5MHz
- +3.3 VDC or +2.5VDC PECL
- Frequency Range from 150.000 to 700 MHz
- Analog multiplication
- Miniature Ceramic SMD Package Available on Tape and Reel
- Lead Free and ROHS Compliant

### ■ ABSOLUTE MAXIMUM RATINGS:

| PARAMETER                   | SYMBOL | VALUE             | UNIT |
|-----------------------------|--------|-------------------|------|
| Operating temperature range | Ta     | -40...+85         | °C   |
| Storage temperature range   | T(stg) | -55...+90         | °C   |
| Supply voltage              | Vcc    | +4.6              | VDC  |
| Maximum Input Voltage       | Vi     | Vss-0.5...Vcc+0.5 | VDC  |
| Maximum Output Voltage      | Vo     | Vss-0.5...Vcc+0.5 | VDC  |

### ■ ELECTRICAL PARAMETERS:

| PARAMETER                   | SYMBOL     | TEST CONDITIONS <sup>1</sup>                                          | VALUE                                                                                                | UNIT                                                     |
|-----------------------------|------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| Nominal Frequency           | fo         |                                                                       | 150.000 ~ 700.00**                                                                                   | MHz                                                      |
| Supply Voltage              | Vcc        |                                                                       | +3.3 or +2.5 ±5%                                                                                     | VDC                                                      |
| Supply Current              | Is         |                                                                       | 80.0 MAX                                                                                             | mA                                                       |
| Output Logic Type           |            |                                                                       | PECL                                                                                                 |                                                          |
| Load                        |            | Connected between each output and Vcc – 2.0 VDC                       | 50                                                                                                   | Ω                                                        |
| Output Voltage Levels       | Voh<br>Vol | min<br>max                                                            | Vcc-1.025<br>Vcc-1.620                                                                               | VDC<br>VDC                                               |
| Duty Cycle                  | DC         | Measured at 50% of Vcc                                                | 40/60 to 60/40 or 45/55 to 55/45                                                                     | %                                                        |
| Rise / Fall Time            | tr / tf    | Measured at 20/80% and 80/20% Vcc Levels                              | 0.7 TYP 1.0 MAX <sup>2</sup>                                                                         | ns                                                       |
| Jitter                      | J          | Integrated Phase tji RMS, Fj = 12 kHz...20 MHz <sup>5</sup>           | 0.3 TYP**                                                                                            | ps                                                       |
|                             |            | Integrated Phase RMS tii offset frequency 50KHz to 80MHz <sup>5</sup> | 0.5 TYP**                                                                                            | ps                                                       |
|                             |            | Deterministic period Jitter Dj using wavecrest analyzer <sup>4</sup>  | Fo<320MHz. 1 TYP **<br>Fo>320MHz. 8 TYP **                                                           | ps                                                       |
|                             |            | Random period Jitter Rj using wavecrest analyzer <sup>4</sup>         | Fo<320MHz. 2.5 TYP **<br>Fo>320MHz. 2.5 TYP**                                                        | ps                                                       |
|                             |            | Acumm. Peak to Peak Jitter Tp-p using wavecrest analyzer <sup>4</sup> | Fo<320MHz. 25 TYP**<br>Fo>320MHz. 27 TYP**                                                           | ps                                                       |
|                             |            |                                                                       |                                                                                                      |                                                          |
| Phase Noise                 | E(Δf)      | typ. @212.5MHz <sup>6</sup>                                           | Δf=10 Hz -65<br>Δf=100 Hz -95<br>Δf=1 KHz -125<br>Δf=10 KHz -140<br>Δf=100 KHz -145<br>Δf≥1M Hz -148 | dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| Sub Harmonics               | f_sub      | Load, nom, Supply nom                                                 | Fo<320MHz. -50<br>Fo>320MHz. -35                                                                     | dBc                                                      |
| Overall Frequency Stability | Δf/fc      | Op. Temp., Aging, Load, Supply and Cal. Variations                    | ±20, ±25, ±50, or ±100 MAX <sup>3</sup>                                                              | ppm                                                      |
| Pin 1 Output Enabled        | En         | High Voltage or No Connect                                            | 0.7•Vcc MIN                                                                                          | VDC                                                      |
| Pin 1 Output Disabled       | Dis        | Ground                                                                | 0.3•Vcc MAX                                                                                          | VDC                                                      |



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1 Test Conditions Unless Stated Otherwise: Nominal Vcc, Nominal Load, +25 ±3°C

\*2 Frequency Dependent

\*3 Not All Stabilities Available With All Temperature Ranges—Please Consult Factory For Availability

\*4 Measured with Wavcrest SIA-3000A 1,000,000 Hits no filtering

\*5 Calculated from Agilent 5500 phase noise measurements

\*6 Measured with Agilent 5500

## ■ PART NUMBERING SYSTEM:

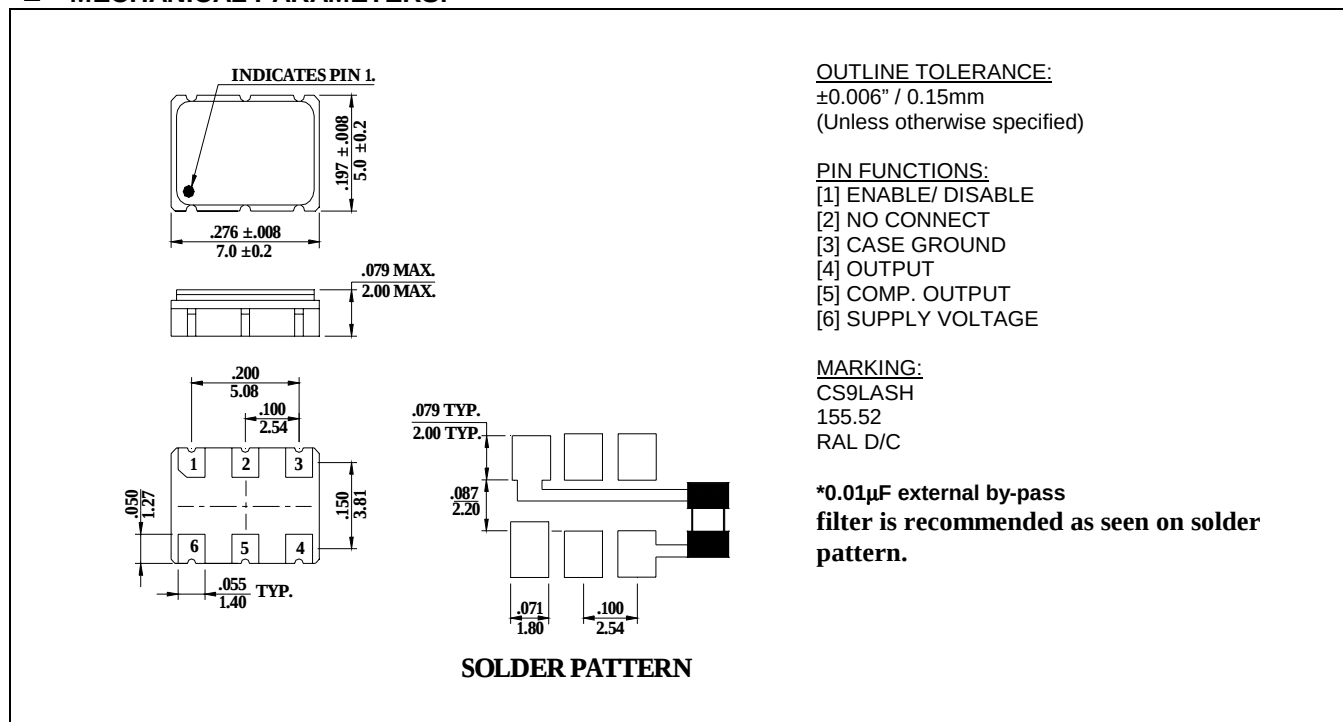
| SERIES                                                                                           | SYMMETRY                                 | TEMPERATURE RANGE (°C)                                     | FREQUENCY STABILITY (Overall)                             | FREQUENCY (MHz)   |
|--------------------------------------------------------------------------------------------------|------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------|-------------------|
| CS9L: UHF +3.3Vdc Clock with PECL Comp. Output<br>CSPL: UHF +2.5Vdc Clock with PECL Comp. Output | A: 40/60 to 60/40%<br>T: 45/55 to 55/45% | R: 0...+50<br>S: 0...+70<br>U: -20...+70<br>V: -40...+85** | K: ±20 ppm**<br>L: ±25 ppm**<br>H: ±50 ppm<br>J: ±100 ppm | 150.000...700.000 |

## EXAMPLE: CS9LASH-155.520

Clock Oscillator, 7x5mm Package, +3.3 VDC Supply Voltage, PECL Output, Standard Symmetry, 0...+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

\*\*Above 300MHz extended temp range and ±25ppm stability may not be available, jitter may vary upon spec requirements. Please consult the factory for any custom requirements.

## ■ MECHANICAL PARAMETERS:



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## ■ REFLOW PROFILE:

