19-0356; Rev 1; 8/92

MAXIM

CMOS, µP-Compatible 8-Bit A/D Converter

1.0 SCOPE

1.1 This specification covers the detail requirements for an 8-bit, monolithic, CMOS multiplying analog-to-digital converter, which is processed in accordance with MIL-STD-883 and is fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MX7574S(X)/883B
-2	MX7574T(X)883/B

1.3 Package

(X)	Package	Description
Q	Q-18	18-Pin Dual-In-Line Package (CERDIP)
E	E-20	20-Pin Ceramic Leadless Chip Carrier (LCC)
D	D-18	18-Pin Side-Brazed Ceramic Package (Ceramic SB)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
Clock Input Voltage to DGND ..... -0.3V, V_{DD}
Digital Input to DGND ..... -0.3V, V_{DD}
Digital Output Voltage to DGND ..... -0.3V, V_{DD}
VREF ..... -20V, +20V
V_{BOFS} ..... -20V, +20V
V_{AIN} ..... -20V, +20V
Power Dissipation (T_A = +70°C, T_j = +150°C)
  18-Pin CERDIP (derate 10.53mW/°C above +70°C) 789mW
  20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
  18-Pin Ceramic SB (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

1.5 Thermal Resistance

Θ_{JC} = 40°C/W for D-18
Θ_{JC} =45°C/W for Q-18
Θ_{JC} =55°C/W for E-20
Θ_{JA} = 90°C/W for D-18
Θ_{JA} =95°C/W for Q-18
Θ_{JA} =110°C/W for E-20

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution	RES	Guaranteed, but not tested	-1, -2		8		Bits
Relative Accuracy	RA	500kHz external clock frequency	-1	1, 2, 3	-0.75	0.75	LSB
			-2	1, 2, 3, 4	-0.5	0.5	
Differential Nonlinearity	DNL	500kHz external clock frequency	-1	1, 2, 3	-0.875	0.875	LSB
			-2	1, 2, 3, 4	-0.75	0.75	
Gain Error	AE	Gain error is measured after calibrating offset error, 500kHz external clock frequency	-1	1	-5	5	LSB
				2, 3	-6.5	6.5	
			-2	1	-3	3	
				2, 3	-4.5	4.5	
Offset Error	V_{OS}	500kHz external clock frequency	-1	1	-60	60	mV
				2, 3	-80	80	
			-2	1	-30	30	
				2, 3	-50	50	
Resistance Mismatch Between B_{OFS} and AIN	RM		-1, -2	1, 2, 3	-1.5	1.5	%
Input Resistance	R_{IN}	At VREF	-1, -2	1, 2, 3	5	15	kΩ
		At B_{OFS}			10	30	
		At AIN			10	30	
Digital Input High Level	V_{IH}	$\overline{RD}$, $\overline{CS}$	-1, -2	1, 2, 3	3		V
Digital Input Low Level	V_{IL}		-1, -2	1, 2, 3		0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	-1, -2	1	-1	1	µA
				2, 3	-10	10	
Digital Input Capacitance	C_{IN}		-1, -2	4		7	pF
Clock Input High	V_{IH}		-1, -2	1, 2, 3	3		V
Clock Input Low	V_{IL}		-1, -2	1, 2, 3		0.4	V
Clock Input High Current	I_{IH}		-1, -2	1, 2, 3	-2	2	mA
Clock Input Low Current	I_{IL}		-1, -2	1	-1	1	µA
				2, 3	-10	10	

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Digital Output High Level	V_{OH}	I_{SOURCE} = 40µA	-1, -2	1, 2, 3	4		V
Digital Output Low Level	V_{OL}	I_{SINK} = 1.6mA	-1, -2	1		0.4	V
				2, 3		0.8	
Floating State Leakage Current (D7-D0)	I_{LKG}	V_{OUT} = 0V or V_{DD}	-1, -2	1	-1	1	µA
				2, 3	-10	10	
Floating State Output Capacitance (D7-D0)	C_{OUT}		-1, -2	4		7	pF
Supply Current	I_{DD}	AIN = 0V, $\overline{BUSY}$ and $\overline{RD}$ = High	-1, -2	1, 2, 3		5	mA
$\overline{CS}$ Pulse Width	t_{CS}		-1, -2	9	150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		-1, -2	9	0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	t_{CBPD}	$\overline{BUSY}$ load = 20pF	-1, -2	9		180	ns
		$\overline{BUSY}$ load = 100pF				200	
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		-1, -2	9	0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		-1, -2	9	0		ns
Data-Valid Access Time	t_{RAD}	D7-D0, load = 100pF	-1, -2	9		400	ns
Data-Valid Hold Time	t_{RHD}		-1, -2	9		180	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHS}		-1, -2	9		500	ns
Reset Time Requirement	t_{RESET}		-1, -2	9	3		µs
$\overline{RD}$ to $\overline{BUSY}$	t_{WBPD}	BUSY load = 20pF	-1, -2	9		2	µs
Conversion Time	$t_{CONVERT}$	2MHz external clock	-1, -2	9		15	µs

Note 1: V_{DD} -= +5V, VREF = -10V, unipolar configuration, R_{CLK} = 180kΩ, C_{CLK} = 100p,F unless otherwise noted.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883.
Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.

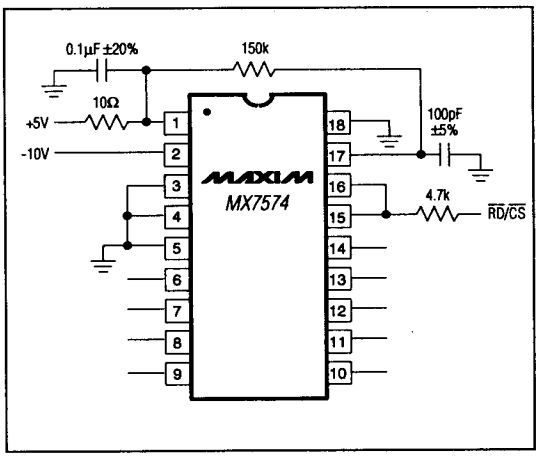
3.4 Groups C and D Inspections:
a. End-point electrical parameters shall be as specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

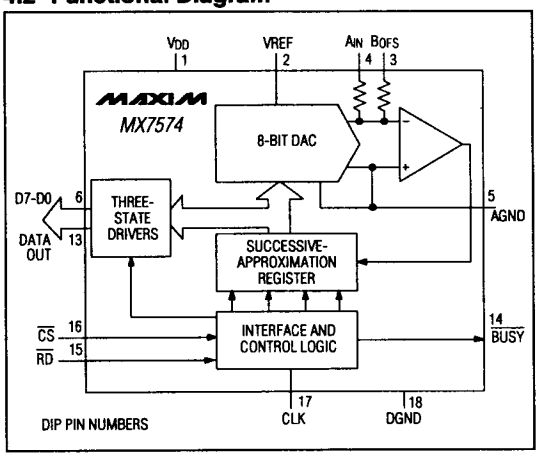
MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
**Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

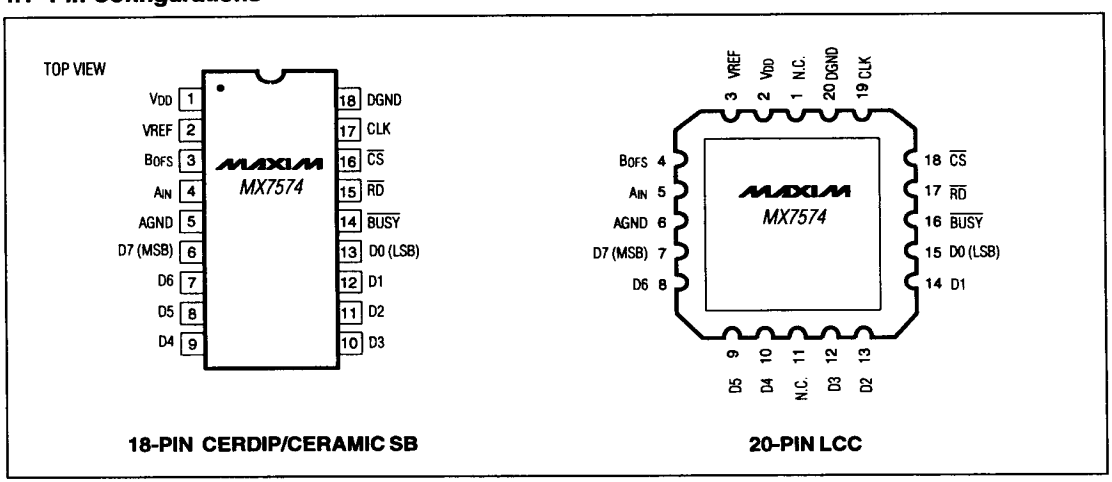
4.0 Life Test/Burn-In Circuit



4.2 Functional Diagram



4.1 Pin Configurations



7