National Semiconductor

54F/74F273
Octal D Flip-Flop

General Description

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'F377 for clock enable version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE® version
- Guaranteed 4000V minimum ESD protection

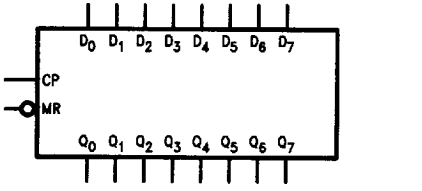
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F273PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F273DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F273SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F273SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F273FM (Note 2)	W20A	20-Lead Cerpack
	54F273LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



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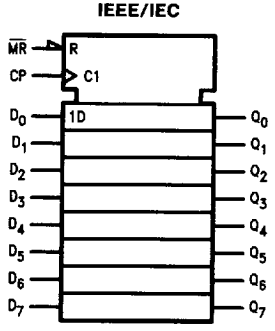

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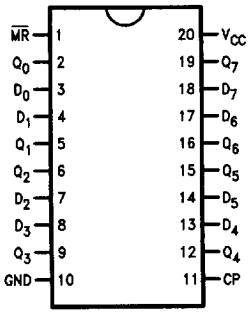
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



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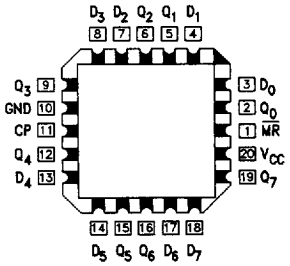
Pin Assignment
for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

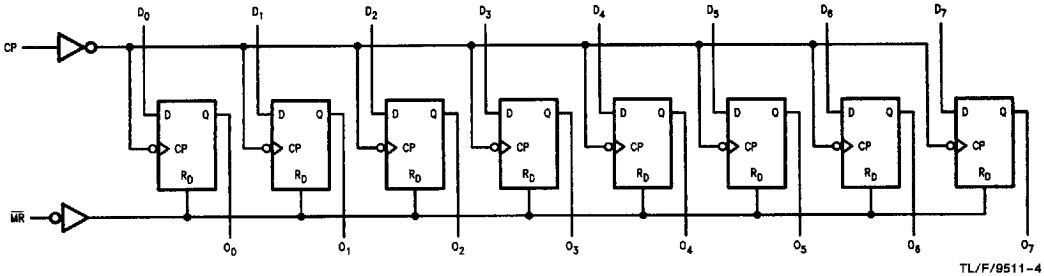
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$	Master Reset (Active LOW)	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
Q_0–Q_7	Data Outputs	50/33.3	−1 mA/20 mA

Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	h	H
Load '0'	H	⌐	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
⌐ = LOW-to-HIGH clock transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	Mil 10% V_{CC} 5% V_{CC}	2.5 2.5 2.7			V	Min	I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	Mil 10% V_{CC} 5% V_{CC}			0.5 0.5 0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All other pins grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All other pins grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH} I_{CCL}	Power Supply Current				44 56	mA	Max	CP = ⌐ D_n = $\overline{MR}$ = HIGH

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F $T_A, V_{CC} =$ Mil, $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	160			95		130		MHz	2–1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3.0 4.0		7.0 9.00	2.5 3.0	9.5 11.0	2.5 3.5	7.5 9.0	ns	2–4
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	4.5		9.5	3.0	11.0	4.0	10.0	ns	2–4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	3.0 3.5		3.5 4.0		3.0 3.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0.5 1.0		1.0 1.0		0.5 1.0			
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	6.0		4.0		6.0		ns	2–4
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	6.0 6.0		5.0 5.0		6.0 6.0		ns	2–4
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.0		4.5		3.5		ns	2–4