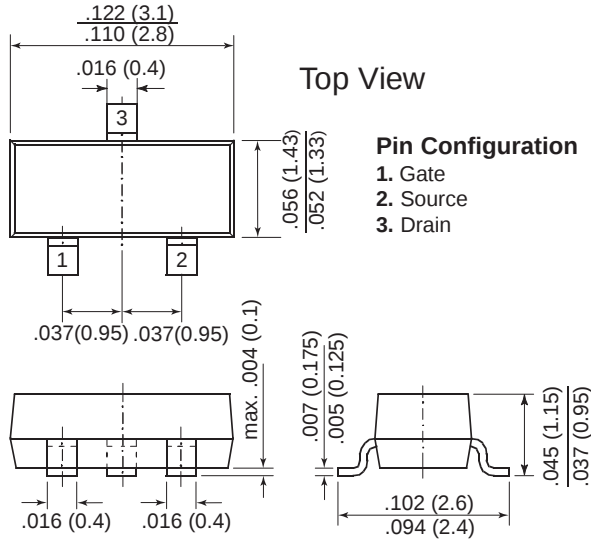


DMOS Transistors (N-Channel)

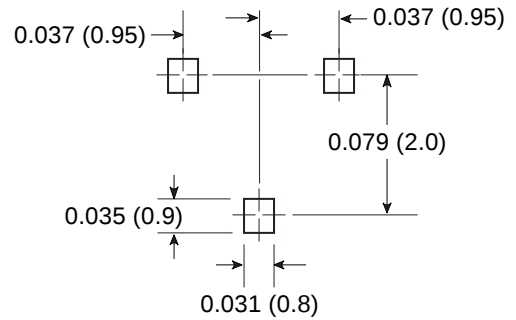


TO-263AB (SOT-23)



Dimensions in inches and (millimeters)

Mounting Pad Layout



Features

- High input impedance
- High-speed switching
- No minority carrier storage time
- CMOS logic compatible input
- No thermal runaway
- No secondary breakdown

Mechanical Data

Case: SOT-23 Plastic Package

Weight: approx. 0.008g

Packaging Codes/Options:

E8/10K per 13" reel (8mm tape), 30K/box

E9/3K per 7" reel (8mm tape), 30K/box

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DSS}	60	V
Drain-Gate Voltage	V _{DGS}	60	V
Gate-Source-Voltage (pulsed)	V _{GS}	±20	V
Drain Current (continuous)	I _D	250	mA
Power Dissipation at T _C = 50°C	P _{tot}	0.310 ⁽¹⁾	W
Thermal Resistance Junction to Substrate Backside	R _{θSB}	320 ⁽¹⁾	°C/W
Thermal Resistance Junction to Ambient Air	R _{θJA}	450 ⁽¹⁾	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature Range	T _S	-55 to +150	°C

Note:

(1) Ceramic Substrate 0.7mm; 2.5cm² area.

DMOS Transistors (N-Channel)

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 100\mu A, V_{GS} = 0$	60	90	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 1mA$	—	2	2.5	
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = 15V, V_{DS} = 0V$	—	—	10	nA
Drain Cutoff Current	I_{DSS}	$V_{DS} = 25V, V_{GS} = 0V$	—	—	0.5	μA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 500mA$	—	5	7.5	Ω
Forward Transconductance	g_m	$V_{DS} = 10V, I_D = 200mA, f = 1MHz$	—	200	—	mS
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0, f = 1MHz$	—	60	—	pF
Turn-On Time	t_{on}	$V_{GS} = 10V, V_{DS} = 10V$ $R_D = 100\Omega$	—	5	—	ns
Turn-Off Time	t_{off}		—	25	—	ns

Note:

(1) Device on fiberglass substrate, see layout

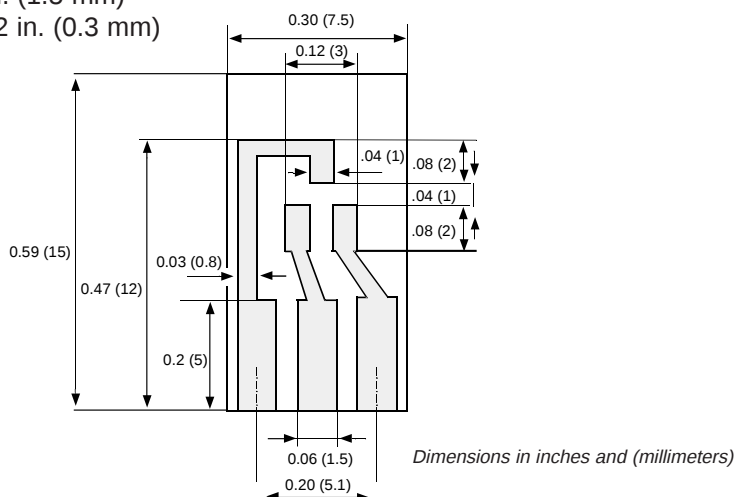
Inverse Diode

Parameter	Symbol	Test Condition	Value	Unit
Max. Forward Current (continuous)	I _F	T _{amb} = 25°C	0.3	A
Forward Voltage Drop (typ.)	V _F	V _{GS} = 0V, I _F = 0.3A T _J = 25°C	0.85	V

Layout for R_{thJA} test

Thickness: Fiberglass 0.059 in. (1.5 mm)

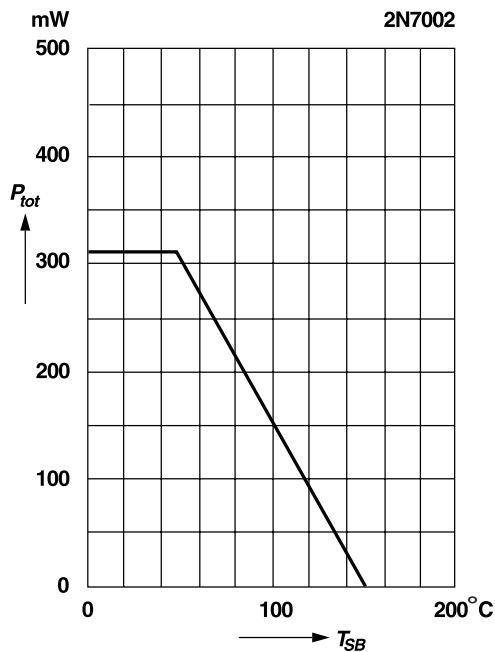
Copper leads 0.012 in. (0.3 mm)



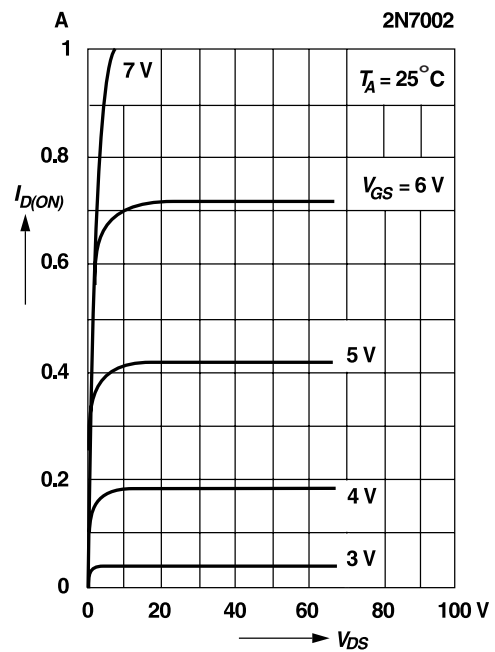
DMOS Transistors (N-Channel)

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

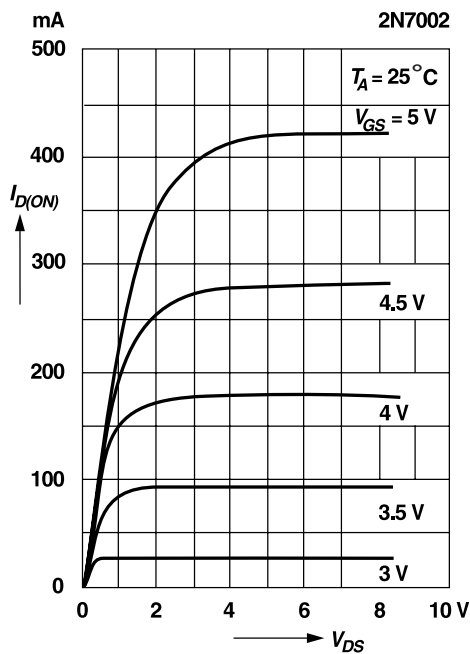
**Admissible power dissipation
versus temperature of substrate backside**
Device on fiberglass substrate, see layout



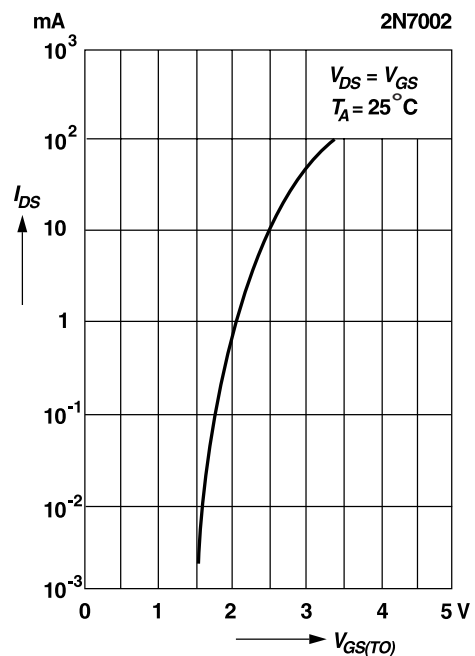
Output characteristics
Pulse test width 80 ms; pulse duty factor 1%.



Saturation characteristics
Pulse test width 80 ms; pulse duty factor 1%.



**Drain-source current
versus gate threshold voltage**

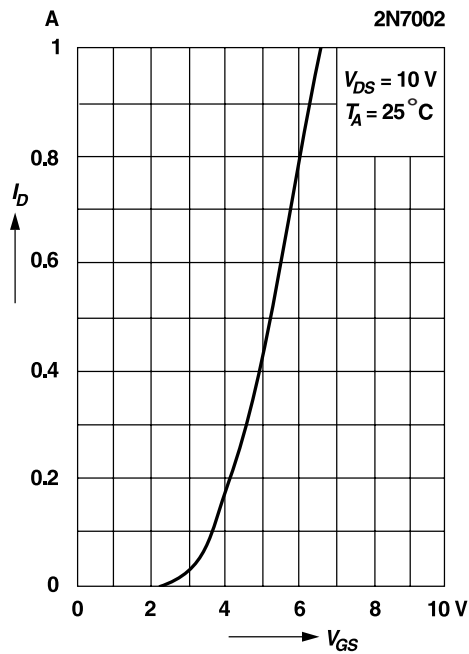


DMOS Transistors (N-Channel)

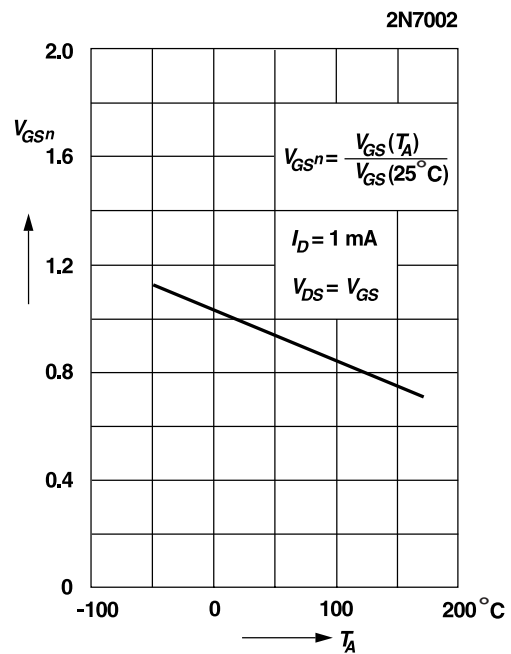
Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Drain current versus gate-source voltage

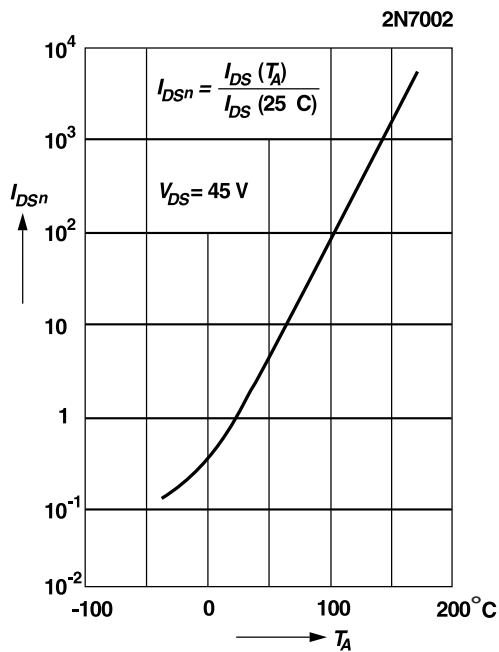
Pulse test width 80 ms; pulse duty factor 1%.



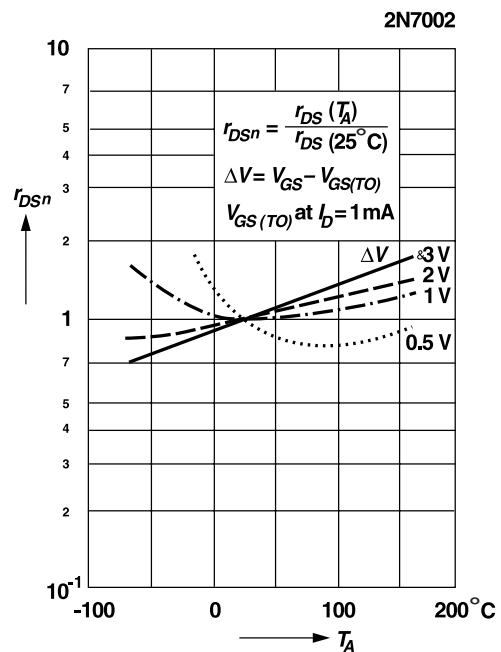
Normalized gate-source voltage versus temperature



Normalized drain-source current versus temperature



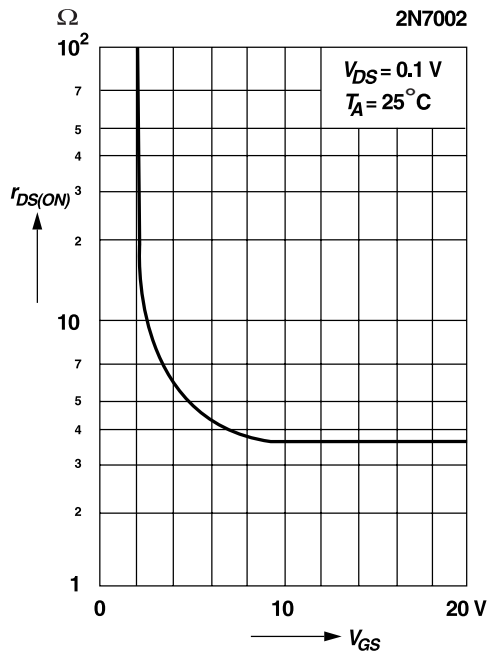
Normalized drain-source resistance versus temperature



DMOS Transistors (N-Channel)

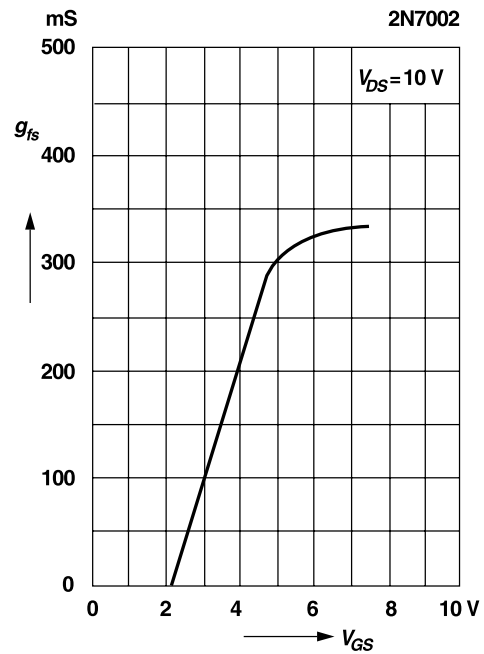
Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

**Drain-source resistance
versus gate-source voltage**



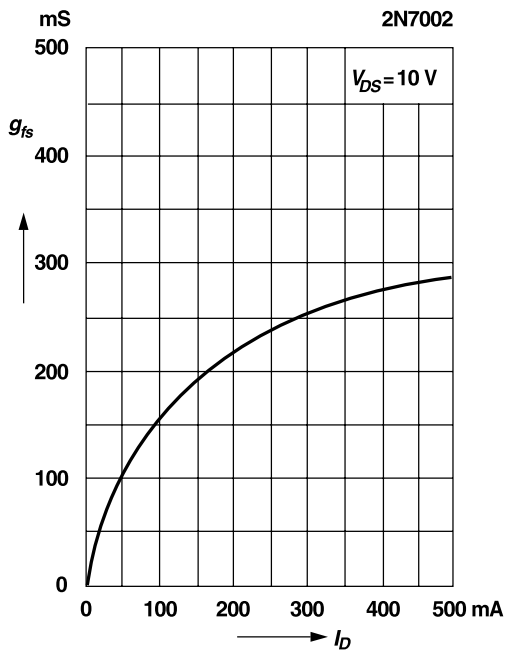
**Transconductance
versus gate-source voltage**

Pulse test width 80 ms; pulse duty factor 1%



**Transconductance
versus drain current**

Pulse test width 80 ms; pulse duty factor 1%



**Capacitance
versus drain-source voltage**

