Ordering number : ENA0879

SANYO Semiconductors

DATA SHEET

LB11691 — Monolithic digital IC Pre-Driver IC for Brushless Motor Drive in Electric Bicycles

Overview

The LB11691 are three-phase bipolar PWM drive pre-driver ICs that allow the output circuits to be implemented using only n-channel FETs. These ICs can implement, at low cost, high-efficiency drive circuits in applications that use motors that require high drive currents. These ICs include a built-in Hall sensor signal F/V conversion circuit and can provide a voltage that is proportional to motor speed for use, for example, in speedometers for electric bicycles. These ICs also support use in applications that holds the speed controlled at a constant rate as the load varies.

Features

- Three-phase bipolar PWM drive (high and low side n-channel FET drive)
- Maximum supply voltage : 45V
- Gate drive voltage : about 10V (high and low side n-channel FETs)
- Hall sensor signal F/V conversion circuit (one-shot multivibrator output)
- Synthesized three-phase Hall sensor signal output
- Built-in current limiter and undervoltage protection circuits

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	V_{CC} pin	45	V
Supply voltage 2	VB max	VB pin	60	V
Output current 1-1	I_O max1	UL, VL, and WL pins	50	mA
Output current 2-1	I_O max2-1	UH, VH, and WH pins sink current	30	mA
Output current 2-2	I_O max2-2	UH, VH, and WH pins source current	40	mA
RF pin application voltage	VRF max		4	V
LVS pin application voltage	VLVS max		60	V

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Parameter	Symbol	Conditions	Ratings	Unit
IN pin application voltage	V_{IN} max	IN1, IN2, and IN3 pins	V5+0.3	V
RES pin application voltage	VRES max		V5+0.3	V
TOC pin application voltage	VTOC max		V5+0.3	V
HSEL pin application voltage	VHSEL max		V5+0.3	V
F/R pin application voltage	VFR max		V5+0.3	V
EI+ pin application voltage	VEI^+ max		V5+0.3	V
EI- pin application voltage	VEI^- max		V5+0.3	V
RC pin application voltage	VRC max		V5+0.3	V
FV pin application voltage	VFV max		V5+0.3	V
HP pin application voltage	VHP max		45	V
FAIL pin application voltage	VFAIL max		45	V
Allowable power dissipation 1	Pd max1	Independent IC	1.5	W
Allowable power dissipation 2	Pd max2	Mounted on a board. *	2.55	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a substrate : 114.3×76.1×1.6mm^3, glass epoxy board.

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{CC}	V_{CC} pin	15 to 42	V
Supply voltage range 2	VB	VB pin	V_{CC}+13	V
Output current 1-1	I_{OUT}1-1	UL, VL, and WL pins sink current	45	mA
Output current 1-2	I_{OUT}1-2	UL, VL, and WL pins source current	-45	mA
Output current 2-1	I_{OUT}2-1	UH, VH, and WH pins sink current	25	mA
Output current 2-2	I_{OUT}2-2	UH, VH, and WH pins source current	-35	mA
12V constant-voltage output current	I_{12REG}		-30	mA
5V constant-voltage output current	I_{5REG}		-30	mA
HP pin application voltage	V_{HP}		0 to 42	V
HP pin output current	I_{HP}		0 to 5	mA
FAIL pin application voltage	VFAIL		0 to 42	V
FAIL pin output current	IFAIL		0 to 5	mA

Electrical Characteristics Ta = 25°C, V_{CC} = 36V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Source current	I_{CC}			19	24	mA
5V constant-voltage output (V5 pin)						
Output voltage	V_{5REG}	I_O = -5mA	4.7	5.0	5.3	V
Voltage fluctuation	ΔV_{5REG1}	V_{CC} = 15 to 42V		40	100	mV
Load fluctuation	ΔV_{5REG2}	I_O = -5 to -30mA		10	30	mV
Temperature coefficient	ΔV_{5REG3}	Design target value *		0		mV/°C
12 V constant-voltage output (V12 pin)						
Output voltage	V_{12REG}	I_O = -5mA	11.2	12.0	12.8	V
Voltage fluctuation	ΔV_{12REG1}	V_{CC} = 15 to 42V		120	240	mV
Load fluctuation	ΔV_{12REG2}	I_O = -5 to -30mA		10	30	mV
Temperature coefficient	ΔV_{12REG3}	Design target value *		0		mV/°C
Output Block/Conditions : U_{OUT} = V_{OUT} = W_{OUT} = 18V, VB = 48V applied						
Output H-level voltage 1	V_{OH}1	UL, VL, and WL pins I_{OH} = -10mA	V12-1.2	V12-0.8		V
Output L-level voltage 1	V_{OL}1	UL, VL, and WL pins I_{OL} = 10mA		0.8	1.2	V
Output H-level voltage 2	V_{OH}2	UH, VH, and WH pins I_{OH} = -5mA	46.8	47.2		V
Output L-level voltage 2	V_{OL}2	UH, VH, and WH pins I_{OH} = 5mA		18.2	18.6	V

* : Design target values and not tested.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Charge pump output (VB pin)						
Output voltage	VB_{OUT}		46.0	48.0	50.5	V
CP1 pin						
Output H-level voltage	V_{OH} (CP1)	ICP1 = -2mA	V_{CC}-1.9	V_{CC}-1.4		V
Output L-level voltage	V_{OL} (CP1)	ICP1 = 2mA		1.5	2.0	V
Integrating amplifier						
Input offset voltage	VIO (CONT)		-10		10	mV
Input bias current	IB (CONT)		-1		1	µA
Common-phase input voltage range	VICM		0		V5-1.7	V
Output H-level voltage	V_{OH} (CONT)	ITOC = -0.2mA	V5-1.1	V5-0.8		V
Output L-level voltage	V_{OL} (CONT)	ITOC = 0.2mA		0.8	1.1	V
Open loop gain		f (CONT) = 1kHz	45	51		dB
PWM oscillator (PWM pin)						
Output H-level voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Output L-level voltage	V_{OL} (PWM)		1.0	1.2	1.3	V
External C charge current	ICHG	VPWM = 2.1V	-35	-25	-19	µA
Oscillation frequency	f (PWM)	C = 270pF	29	36	44	kHz
Amplitude	V (PWM)		1.6	1.8	2.1	Vp-p
TOC pin						
Input voltage 1	VTOC1	Output duty 100%	2.72	3.0	3.30	V
Input voltage 2	VTOC2	Output duty 0%	0.99	1.2	1.34	V
Input voltage 1L	VTOC1L	Design target value*, 100% at V5 = 4.7V	2.72	2.80	2.90	V
Input voltage 2L	VTOC2L	Design target value*, 0% at V5 = 4.7V	0.99	1.08	1.17	V
Input voltage 1H	VTOC1H	Design target value*, 100% at V5 = 5.3V	3.08	3.20	3.30	V
Input voltage 2H	VTOC2H	Design target value*, 0% at V5 = 5.3V	1.11	1.22	1.34	V
Current limiting circuit (RF pin)						
Limiter voltage	VRF		85	100	115	mV
Low-voltage protective circuit (LVS pin)						
Operating voltage	VSDL		3.65	3.85	4.05	V
Cancellation voltage	VSDH		4.15	4.35	4.55	V
Hysteresis width	ΔVSD		0.35	0.5	0.65	V
Heat shielding operation (overheat protection circuit)						
Heat shielding operation temperature	TSD	Design target value* (junction temperature)	150	170		°C
Hysteresis width	ΔTSD	Design target value* (junction temperature)		40		°C
CSD circuit (CSD pin)						
Output H-level voltage	V_{OH} (CSD)		3.2	3.6	4.0	V
Output L-level voltage	V_{OL} (CSD)		0.9	1.1	1.3	V
External C charge current	ICHG1	VCSD = 2.35V	-14	-10	-6	µA
External C discharge current	ICHG2	VCSD = 2.35V	7	11	15	µA
Oscillation frequency	f (CSD)	C = 0.01µF		180		Hz
Amplitude	V (CSD)		2.2	2.5	2.75	Vp-p
Reset circuit (RES pin)						
Reset operating voltage	VRESL		1.17	1.27	1.37	V
Reset canceling voltage	VRESH		1.37	1.5	1.63	V
Hysteresis width	ΔVRES		0.20	0.23	0.26	V
HP pin						
Output saturation voltage	VHPL	I_O = 3mA		0.15	0.5	V
Output leak current	IHP leak	VHP = 42V			10	µA

* : Design target values and not tested.

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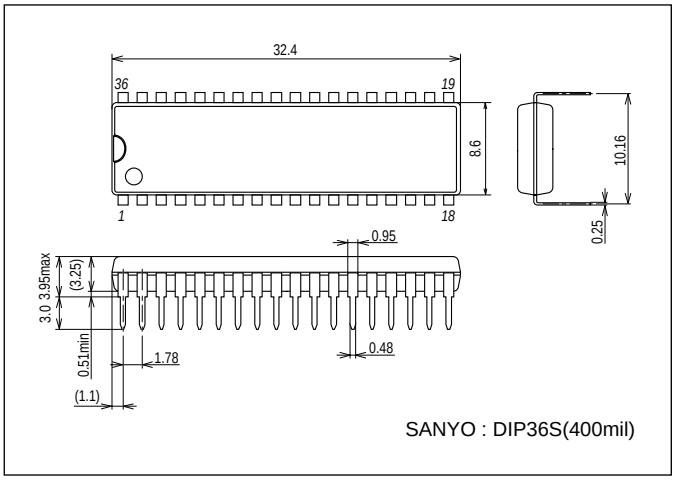
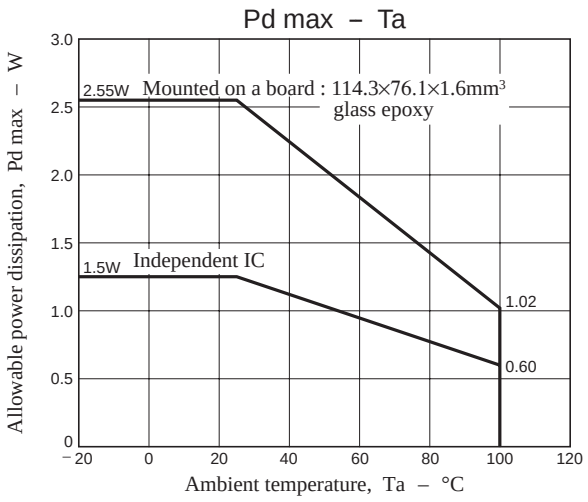
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FAIL pin						
Output saturation voltage	VFLL	I_O = 3mA		0.15	0.5	V
Output leak current	IFL leak	VFAIL = 42V			10	μA
RC pin						
Output H-level voltage	V_{OH} (RC)		3.22	3.5	3.78	V
Output L-level voltage	V_{OL} (RC)		0.72	0.8	0.88	V
Clamp voltage	VCLP (RC)			1.5		V
FV pin						
Charge current	ICHG1	VFV = 2.5V	-420	-300	-230	μA
Discharge current	ICHG2	VFV = 1V	1.3	2.5	5.0	mA
IN1, IN2, and IN3 pins						
H-level input voltage	V_{IH} (IN)		4.0		V5	V
L-level input voltage	V_{IL} (IN)		0		2.5	V
Input open voltage	V_{IO} (IN)		V5-0.5		V5	V
Hysteresis width	V_{IS} (IN)		0.55	0.9	1.25	V
H-level input current	I_{IH} (IN)	V_{IN} = V5	-10	0	10	μA
L-level input current	I_{IL} (IN)	V_{IN} = 0V		-500		μA
F/R pin						
H-level input voltage	V_{IH} (FR)		2.0		V5	V
L-level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		2.6	2.9	3.2	V
Hysteresis width	V_{IS} (FR)		0.16	0.25	0.34	V
H-level input current	I_{IH} (FR)	VF/R = V5		100	130	μA
L-level input current	I_{IL} (FR)	VF/R = 0V	-170	-130		μA
HSEL pin						
H-level input voltage	V_{IH} (HSL)		2.0		V5	V
L-level input voltage	V_{IL} (HSL)		0		1.0	V
Input open voltage	V_{IO} (HSL)		2.6	2.9	3.2	V
H-level input current	I_{IH} (HSL)	VHSEL = V5		100	130	μA
L-level input current	I_{IL} (HSL)	VHSEL = 0V	-170	-130		μA

Package Dimensions

unit : mm (typ)

3170A





Three-phase logic truth table

(1)120° (HSEL = “L”)

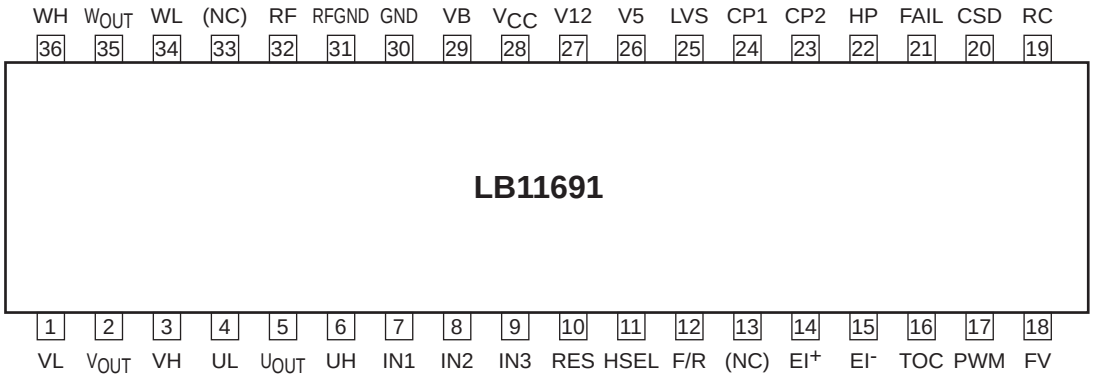
	F/R = “L”			F/R = “H”					
	IN1	IN2	IN3	IN1	IN2	IN3	Upper side gate	Lower side gate	HP
1	H	L	H	L	H	L	VH	UL	H
2	H	L	L	L	H	H	WH	UL	L
3	H	H	L	L	L	H	WH	VL	H
4	L	H	L	H	L	H	UH	VL	L
5	L	H	H	H	L	L	UH	WL	H
6	L	L	H	H	H	L	VH	WL	L

(2)60° (HSEL = “H”)

	F/R = “L”			F/R = “H”					
	IN1	IN2	IN3	IN1	IN2	IN3	Upper side gate	Lower side gate	HP
1	H	H	H	L	L	L	VH	UL	H
2	L	H	H	H	L	L	WH	UL	L
3	L	L	H	H	H	L	WH	VL	H
4	L	L	L	H	H	H	UH	VL	L
5	H	L	L	L	H	H	UH	WL	H
6	H	H	L	L	L	H	VH	WL	L

- The condition with the upper gate = VH and the lower gate = UL corresponds to a state in which the upper FET is turned ON when the VH pin is connected and the lower FET is turned ON when the UL pin is connected.
- The HP output is an open collector output. Therefore, “H” level corresponds to an open state.

Pin Assignment

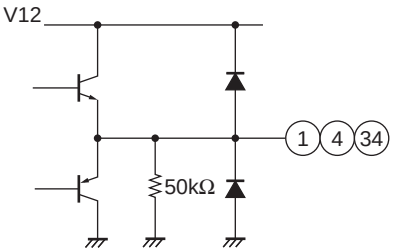
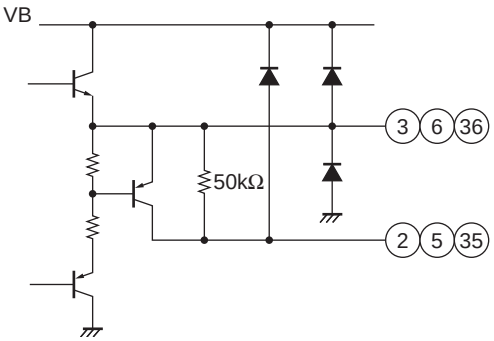
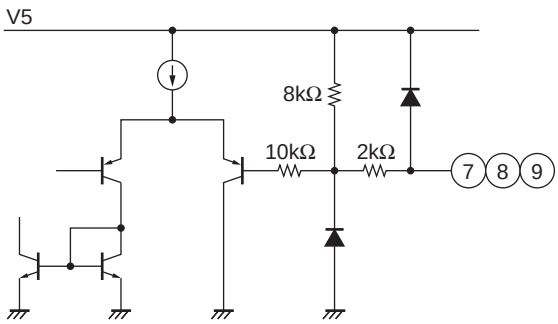
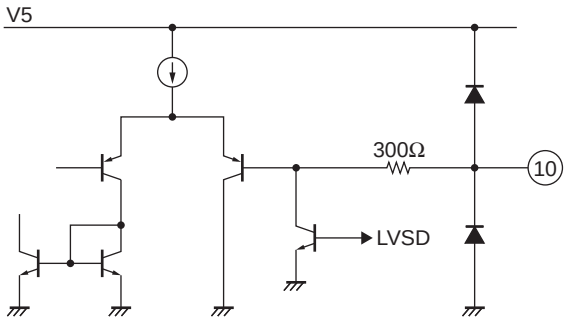
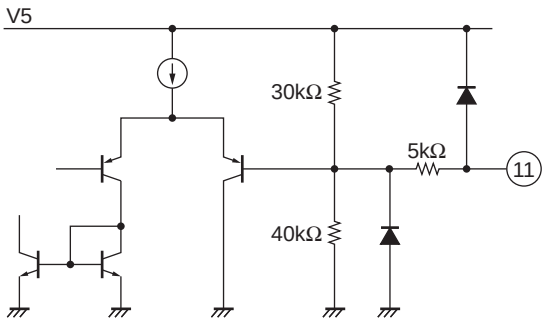


Top view

Pin Functions

Pin No.	Pin Name	Description
1 4 34	VL UL WL	Lower Nch power FET gate drive output pins.
2 5 35	VOUT UOUT WOUT	Upper Nch power FET source voltage detection pins.
3 6 36	VH UH WH	Upper Nch power FET gate drive output pin.
7 8 9	IN1 IN2 IN3	Hall input pins. A capacitor is connected for stabilization between these pins and GND.
10	RES	Reset pin. A resistor is connected between this pin and V5 while a capacitor is connected between this pin and GND.
11	HSEL	Reset pin. Connect the resistance between this pin and V5 and the capacitor between this pin and GND.
12	F/R	Pin for changeover of the phase difference of three-phase Hall input (120° and 60°). HSEL = “L” 120°, HSEL = “H” 60°
14	EI^+	Integrating amplifier non-inverted input pin.
15	EI^-	Integrating amplifier inverted input pin.
16	TOC	PWM waveform comparison pin (integrating amplifier output pin).
17	PWM	PWM oscillation frequency set pin. Connect a capacitor between this pin and GND.
18	FV	Hall signal one-shot multi-pulse output.
19	RC	One-shot multi-pulse width set pin. A resistor is connected between this pin and V5 while a capacitor is connected between this pin and GND.
20	CSD	Pin to set the operation time of the lock protection circuit. Connect the capacitor between this pin and GND.
21	FAIL	Open collector output, with the output being “L” in following cases : Abnormal Hall input, activation of the low-voltage protection circuit, activation of the lock protection circuit, and activation of the overheat protection circuit.
22	HP	Hall signal three-phase composite output pin (open collector output).
23 24	CP2 CP1	Charge pump capacitor output pin. A capacitor is connected between CP1 and CP2.
25	LVS	Low-voltage protective voltage detection pin. A Zener diode is connected in series to set the detection voltage when the supply voltage of 5V or more is to be detected.
26	V5	5V power pin (control circuit power supply). A capacitor is connected between this pin and GND.
27	V12	12V power pin (UL, VL, and WL output power supply). A capacitor is connected between this pin and GND.
28	V_{CC}	Power pin. A capacitor is connected for stabilization between this pin and GND.
29	VB	Charge pump output pins (UH, VH, and WH output power supply). A capacitor is connected between this pin and V_{CC}.
30	GND	GND pin.
31	RFGND	GND sensing pin, which is connected to the GND side of low-resistance RF connected to the RF pin.
32	RF	Output current detection pin. Low-resistance RF is connected between RF and GND. The output current is limited to the value set with I_{OUT} = 0.1/RF. (Current limiting circuit)
13 33	NC	These can be used as wiring because they are not connected with the internal parts.

Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit
1 4 34	VL UL WL	Output pin (Gate driving output pin of lower Nch power FET) For duty control	
2 5 35	VOUT UOUT WOUT	Voltage detection pin (Source voltage detection pin of upper Nch power FET)	
3 6 36	VH UH WH	Output pin (Gate driving output pin of lower Nch power FET)	
7 8 9	IN1 IN2 IN3	Hall input pin "H" in the open condition. Connect a capacitor to GND for stabilization.	
10	RES	Reset pin	
11	HSEL	Pin to change over the phase difference of three-phase Hall input HSEL = "L" 120° HSEL = "H" 60°	

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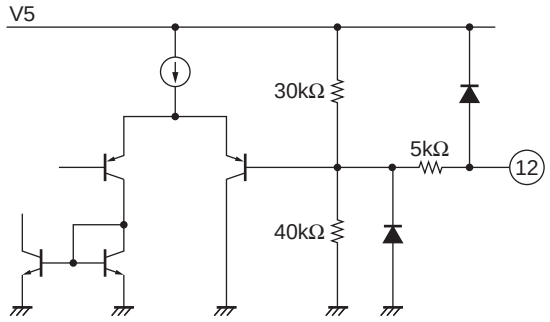
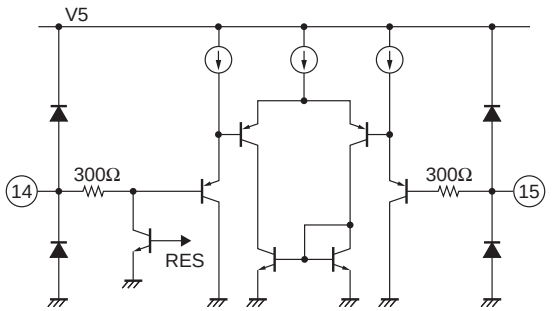
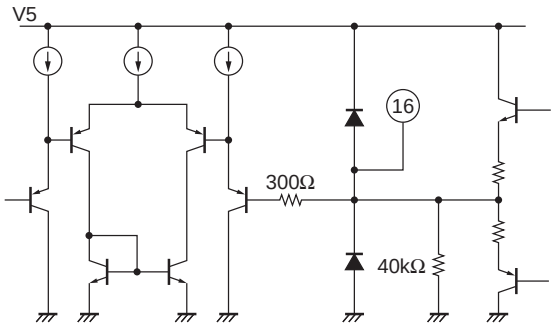
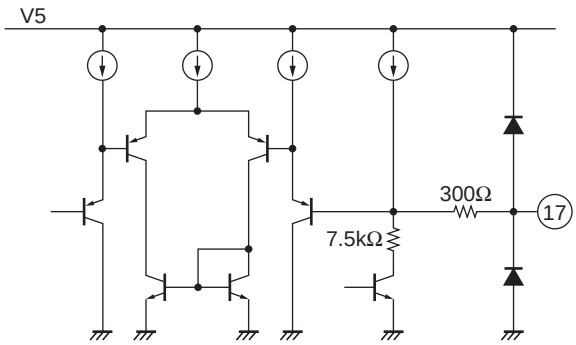
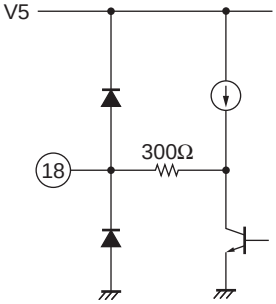
Pin No.	Pin Name	Description	Equivalent Circuit
12	F/R	Forward/backward input pin	
14	EI+	Integrating amplifier non-inverted input pin	
15	EI-	Integrating amplifier inverted input pin	
16	TOC	Integrating amplifier output pin (PWM waveform comparison pin)	
17	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND.	
18	FV	Hall signal one-shot multi-pulse output pin	

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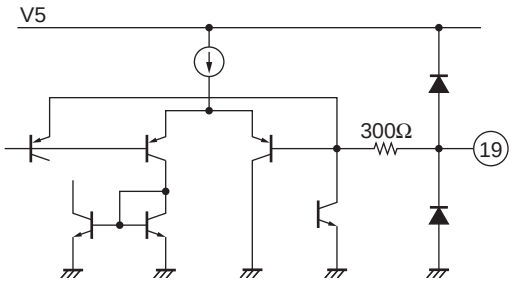
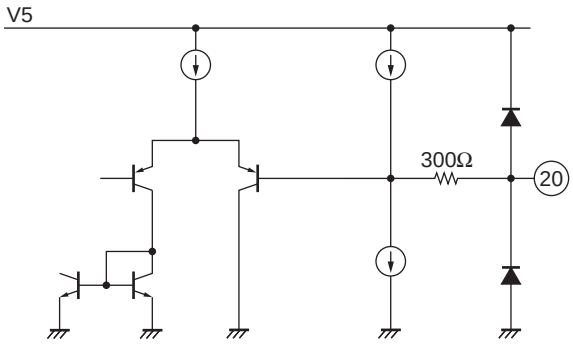
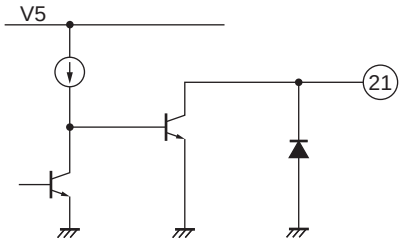
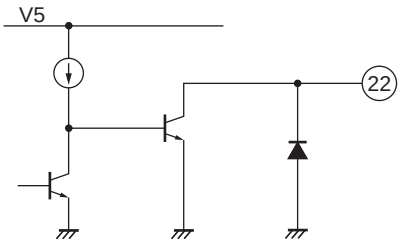
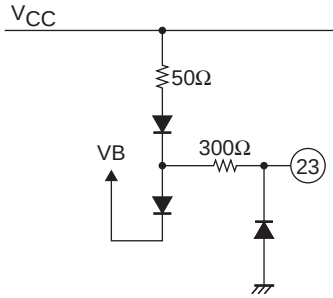
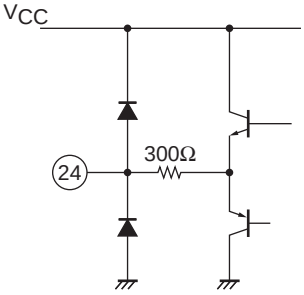
Pin No.	Pin Name	Description	Equivalent Circuit
19	RC	One-shot multi-pulse width setting pin Connect a resistor between this pin and V5 and a capacitor between this pin and GND.	
20	CSD	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND.	
21	FAIL	Open collector output, with the output being “L” in following cases : Abnormal Hall input, activation of the low-voltage protection circuit, activation of the lock protection circuit, and activation of the overheat protection circuit	
22	HP	Hall signal three-phase composite output pin (Open collector output)	
23	CP2	Charge pump capacitor connection pin Connect a capacitor between CP1 and CP2.	
24	CP1		

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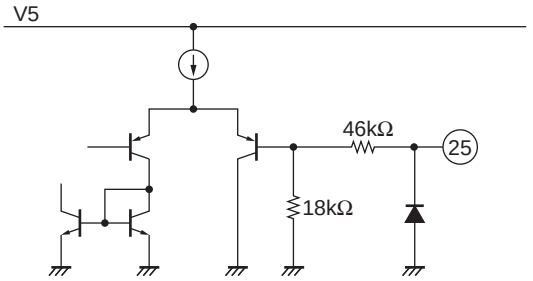
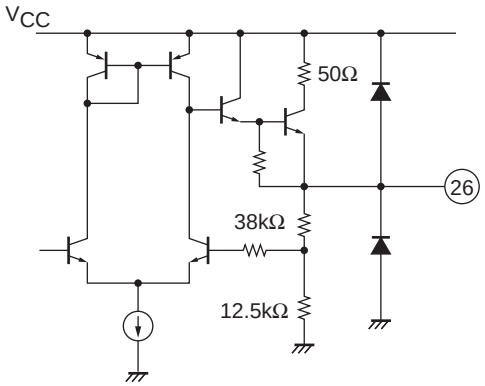
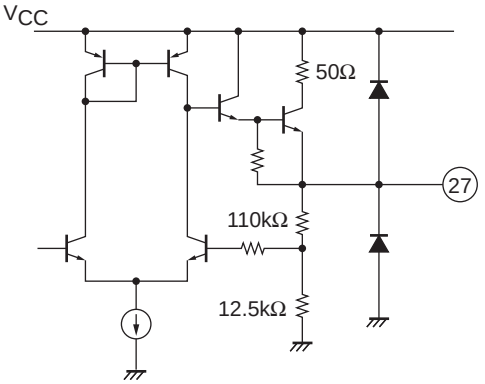
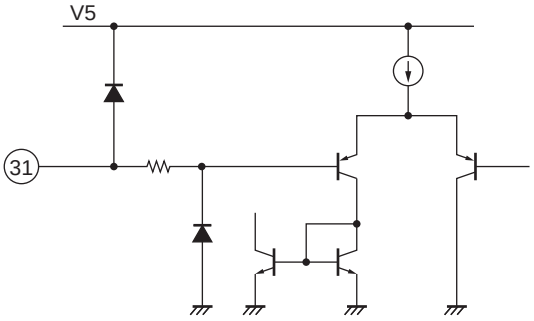
Pin No.	Pin Name	Description	Equivalent Circuit
25	LVS	Low-voltage protective voltage detection pin When the 5V or more supply voltage is to be detected, connect Zener diode in series and set the detection voltage.	
26	V5	Stabilization power supply output pin (5V output) Connect a capacitor (about 0.1µF) between this pin and GND for stabilization	
27	V12	Stabilization power supply output pin (12V output) Connect a capacitor (about 0.1µF) between this pin and GND for stabilization.	
28	V_{CC}	Power pin Connect a capacitor (about 0.1µF) between this pin and GND for stabilization	
29	VB	Charge pump output pin (UH, VH, and WH output power supply) Connect a capacitor between this pin and V_{CC}.	
30	GND	GND pin	
31	RF GND	Connected to GND of external Rf resistor.	

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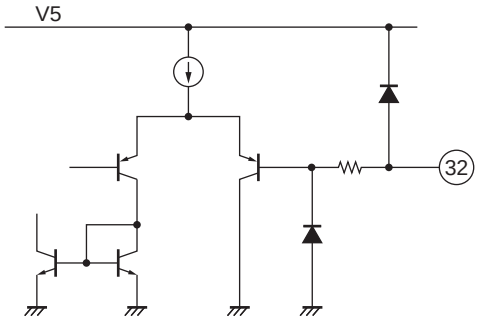
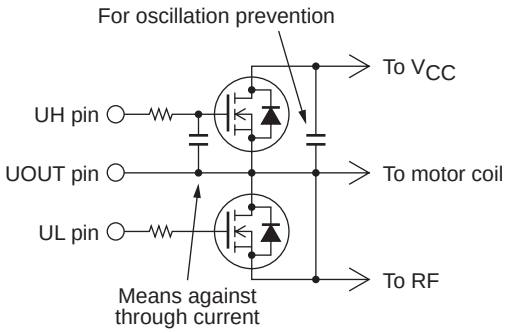
Pin No.	Pin Name	Description	Equivalent Circuit
32	RF	Output current detection pin. Connect the low resistance Rf between this pin and GND. Set with the output maximum current I_{OUT} = 0.1/Rf.	
13 33	NC	These can be used as wiring because they are not connected with the internal parts.	

Description of LB11691

1. Output drive circuit

This IC is designed on the prerequisite that NchFET is used for both upper and lower outputs. To minimize power loss at the output, the direct PWM drive method is used. Output Tr is normally saturated at ON and the motor drive power is adjusted by changing the ON-duty of the output. PWM switching of the output is made on the lower output side to which UL, VL, and WL pins are connected. Diode built into the upper output FET on the non-PWM side should be selected with care because the reverse recovery time is important (the through current flows in an instant when the PWM side Tr is turned ON if the diode with the short reverse recovery time is not used).

Near each three-phase output FET, provide a capacitor to prevent high-frequency oscillation (about 0.1μF) because of substrate pattern routing.



If the switching speed of FET is so high as to cause a problem, insert a series resistor to the gate to adjust the speed. Through current may flow if the ON speed of lower FET on the PWM side is too fast. However, insertion of excessively large resistor in the gate may make the gate waveform dull and the gate voltage may be deficient when the PWM on-duty is small, resulting in heat generation or damage of the lower FET. The same phenomena occur if the FET gate capacity is large even when the resistor has not been inserted. In this case, it is necessary to limit the minimum duty to be used by taking into account ASO of the switching element to be used.

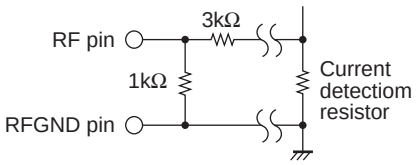
Depending on FET to be used, the through current may flow when the PWM on-duty is small. As a countermeasure, a capacitor may be inserted between the gate and source of upper FET. Note that insertion of a capacitor with excessively high capacitance may delay switching too much, resulting in heat generation in the upper FET.

2. Current limiting circuit

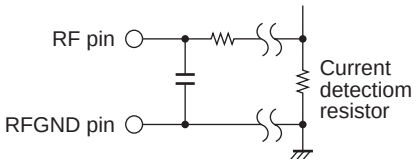
The current limiting circuit limits the current to the value determined by I = VRF/Rf (VRF = 0.1Vtyp, Rf : current detection resistance) (that is, the peak current is limited). Current is limited by decreasing on-duty of the output.

Connection of RF and RFGND pins to both ends near the current detection resistor ensures operation with the correct current limiting value.

When the current detection resistor with extremely small resistance is to be used, the pattern design must be such as to ensure the equal wiring resistance component by substrate pattern for all phases as much as possible. If the wiring resistance component varies among phases, the current limit value fluctuates each time the shift is changed, resulting in vibration or noise in the motor.



The reference voltage has been set to 0.1Vtyp to minimize the power of current detection resistor. In certain applications, enter the voltage divided by the resistor into RF pin when the current detection resistance is to be increased. For the resistance ratio shown in the figure right, the detection current value may be increased by about four times.



The current limiting circuit has a filter circuit so that erroneous current limiting is not made when the circuit detects the reverse recovery current of the output diode because of PWM operation. In the normal application, the internal filter circuit is allowed. If erroneous limiting occurs (if the reverse recovery current of diode flows for 1μS or more), it is necessary to add the external filter circuit (R and C low-path filter). Note also that excessive delay may cause delay in detection of current limiting.

3. PWM oscillation circuit

The PWM frequency is determined from a capacitor capacity C (F) to be connected to the PWM pin :

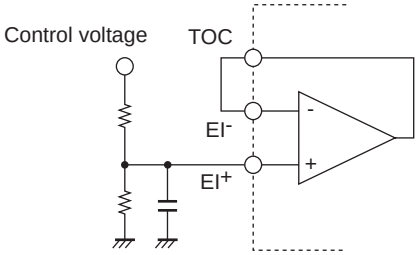
$$fPWM \approx 1/(102000 \times C)$$

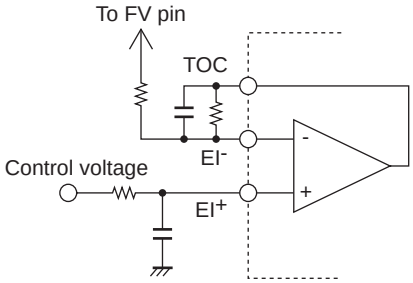
Connection of a 270pF capacitor causes oscillation of about 36kHz. Excessively low PWM frequency causes a switching sound from the motor while excessively high PWM frequency causes increase in the power loss at output. Therefore, the PWM frequency of about 20k to 50kHz would be acceptable. Wire GND of a capacitor to be connected as much near as possible to the GND pin of IC to prevent effects of output noise.

4. Control method

The output duty is determined from comparison between the PWM oscillation waveform and TOC pin voltage. The duty becomes 0% when the TOC pin voltage is about 1.2V or less and 100% when the pin voltage is about 3.0V or more.

Normally, the integrating amplifier is used as a full return amplifier (EI^- pin and TOC pin connected) and the control voltage is entered to EI^+ pin. (The output duty increases with increasing EI^+ pin voltage.) At resetting with the RES pin, the EI^+ pin is lowered approximately to the GND voltage by IC internal TR (for capacitor discharge). Therefore, always enter the voltage via resistor, instead of direct connection of the low-impedance power. Also connect a pull-down resistor between the EI^+ pin and GND to prevent the motor from being driven when the control voltage is open. When the control voltage contains noise or in order to suppress sudden fluctuation of the control voltage, connect a capacitor between the EI^+ pin and GND to remove the noise. The operating voltage range of control input can be widened by entering the voltage divided by the resistor into the EI^+ pin, as shown in the figure right.





To perform control while keeping the rotation speed constant to a certain degree under load fluctuation, the speed control circuit with FV pin output may be formed as shown in the right. Select a 25kΩ or more resistance to be inserted between FV and EI^- pins. Select the return capacitor capacity so that the TOC pin voltage is sufficiently stable at low speed.

5. Charge pump circuit

The voltage is raised by the charge pump circuit, generating the gate voltage of upper output FET. The voltage is raised by a capacitor CP connected between CP1 and CP2 pins, accumulating the charge in the capacitor CB between VB and V_{CC} pins. The capacitance value of CP and CB must always have the following relationship :

$$CB \geq 4 \times CP$$

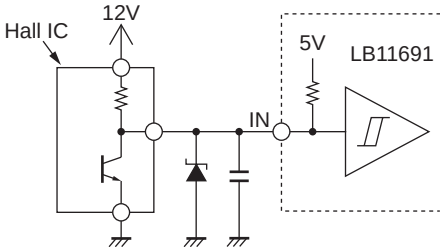
CP capacitor charge and discharge are made on the basis of PWM cycle. Though the VB power supply current capacity increases with increasing capacity of the CP capacitor, excessively large capacity may cause faulty charge/discharge operation. The VB voltage becomes more stable when the CB capacitor capacity is larger, but excessively large capacity causes longer time of VB voltage generation at a time of power ON. Set the capacity of CP and CB by referring to the table below.

When the V_{CC} voltage decreases below 20V, the current capacity of VB power supply deteriorates suddenly, causing drop of VB voltage. Therefore, due care must be taken when designing.

V_{CC} voltage	24V	36V
CP	0.1μF	6800pF
CB	1μF	0.47μF

6. Hall input signal

Connect the Hall IC output to the Hall input. As an about 10kΩ pull-up resistor is incorporated for the 5V regulator, it is normally not necessary to connect the pull-up resistor externally. If the Hall IC with built-in pull-up resistor is used, it is enough to use the Hall IC power supply with 5V. If the Hall IC power supply is to be used with 12V, it is necessary to add the pull-down resistor or voltage clamp Zener diode to prevent application of voltage of 5V or more to the Hall input.

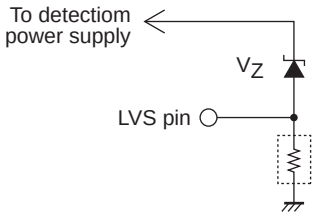


The input is a comparator input with about 0.9V hysteresis width. If the noise presents problem, connect a noise removing capacitor between the input and GND.

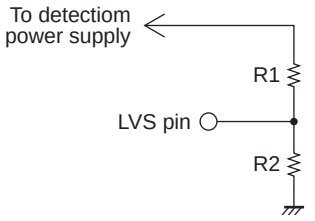
When three inputs of Hall input signal are in the same input condition, both upper and lower outputs are turned OFF.

7. Low-voltage protective circuit

The low-voltage protective circuit performs detection using the voltage applied to the LVS pin and turns OFF all drive outputs when the voltage drops below the operating voltage (3.85Vtyp). The circuit has hysteresis to prevent repetition of ON/OFF near the protected operating voltage. The output is not recovered when the voltage does not rise by about 0.5V above the operating voltage. In the protection operation, the RES pin voltage becomes “L” too.



The protection operating voltage is based on the 5V system detection level. To raise the detection level, connect Zener diode in series to the LVS pin and shift the detection level (detection voltage = 3.85Vtyp+Vz). The LVS pin inrush current at detection is about 62μA. If it is necessary to stabilize rise of the Zener diode voltage and to suppress fluctuation of the Zener voltage, insert a resistor between LVS pin and GND to increase the diode current. The detection voltage may also be raised, without using Zener diode, by resistive potential division. When connection as shown in the right is made ;



Detection voltage ≈ ((3.85 ÷ R2) + 62μA) × (R1+R2)

Cancellation voltage ≈ ((4.35 ÷ R2) + 70μA) × (R1+R2)

With R1 = 13kΩ and R2 = 2.2kΩ, the detection voltage becomes about 28V while the cancellation voltage becomes about 32V. Pay due attention when raising R2 because the error of detection voltage may increase because of temperature and variance.

When the protective circuit is not to be used, do not open the LVS pin (output OFF when this is opened) and apply the voltage on an inoperative level.

8. RES circuit

Apply initial reset with the RES pin to ensure stable operation at power ON. Initial reset includes the following operations :

- All drive outputs OFF
- EI^+ pin voltage at “L”
- FV pin voltage at “L”

Normally, connect a resistor and capacitor between RES and V5 pins and between these pins and GND respectively and set the reset time. Use a 2.7kΩ or more resistor. Set so that the time constant becomes R × C ≥ 1m (0.1μF or more if this is 10kΩ). If the charge of a capacitor connected to EI^+ or FV pin must be completely discharged, set the reset time by taking into account the discharge time of these pins. It is also recommended to set the reset time longer than the time necessary for stabilization of the VB voltage at power ON.

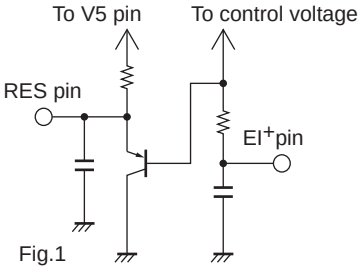


Fig.1

In addition to initial reset, reset may be applied when the control voltage is low as shown in Fig. 1 in the right. In this case, all drive outputs can be turned OFF when the control voltage becomes about 0.67V(1.27V - V_{BE}). The reset cancellation voltage is about 0.9V (0.67V+0.23V). If only the control voltage is 0% duty (1.2V or less), the motor is braked when driven in the reverse direction. This is an effective application when braking is not necessary during reverse drive. If the control voltage cannot be decreased to 1V or less, application as shown in Fig. 3 may be used.

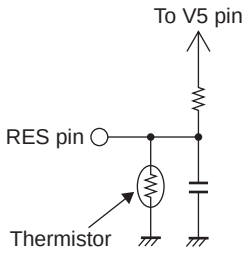


Fig.2

Heat detection with thermistor may also be considered to prevent thermal breakdown of output FET. Connect as shown in Fig. 2 in the right and adjust the external resistance, and the protective operation can be done. Fig. 4 shows a combination of this application with thermistor and an application shown in Fig. 3.

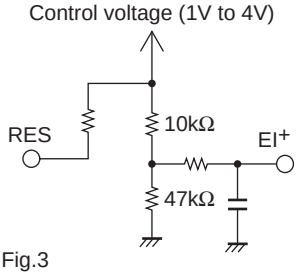


Fig.3

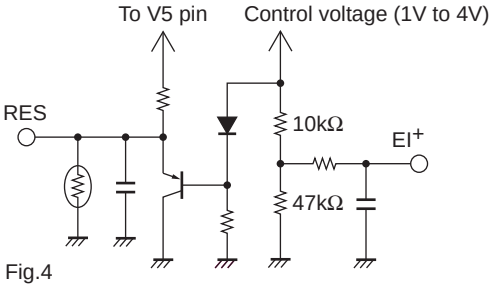


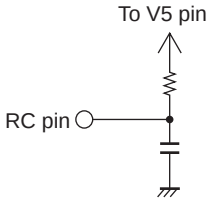
Fig.4

9. RC and FV circuits

The RC pin is to set the pulse width ("H" time) generated in the FV pin for both edges of HP signal (Hall three-phase composite signal). Connect a resistor and capacitor between RS and VE pins and between this pin and GND respectively and set the pulse width. The pulse width TRC can be approximated by the following equation.

$$TRC\ (S) \approx 1.1 \times R \times C$$

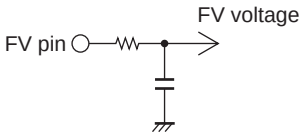
Connect the smoothing circuit comprising a resistor and capacitor, as shown in the right, to the FV pin. Select the 25kΩ or more resistor. The capacitor must have the capacitance ensuring sufficient smoothing of FV voltage when the motor rotation speed is low.



Assume that the HP signal frequency at the maximum motor speed is fHP (Hz). Set so that the following equation is established :

$$TRC\ (S) \leq 1 \div (2 \times fHP)$$

In this case, the FV voltage changes from 0 to about 5V according to the motor speed. The FV voltage can be used as a signal for speed meter indication of analog or level meter IC or speed return.



If FV output is not to be used, connect the RC pin to GND and keep the FV pin open.

10. Power stabilization

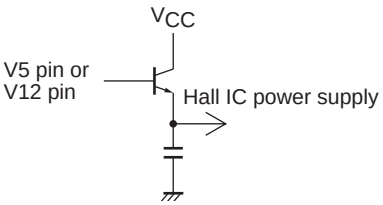
This IC is of a switching drive type, causing a state in which the power line is readily displaced. It is therefore necessary to connect the capacitor with sufficient capacity between the V_{CC} pin and GND for stabilization.

When a diode is to be inserted into the power line to prevent breakdown due to reverse connection of power supply, the power line tends to be displaced readily. It is therefore necessary to select the larger capacity.

11. Stabilizing the regulator output voltage

Connect the capacitor of 0.1μF or more between V5 pin (5V : control circuit power supply) or V12 pin (12V : lower drive output circuit power supply) and GND. Wire the capacitor GND as near to IC GND pin as possible.

Each output can output the current of 30mA or less to the outside of IC. Due care must be taken however because IC heat generation increases. If this is used in the Hall IC power supply and presents a problem of heat generation, connect Tr as shown in the right so that Tr receives heat generation.



12. Lock protection circuit

The lock protection circuit is incorporated to protect IC and motor when the motor is locked. When the Hall input signal is not changed over for a certain period while the motor is being driven, the output on one side (UL, VL, WL) is turned OFF. The time is set with the capacitor capacitance connected to the CSD pin.

$$\text{Set time (s)} \approx 30 \times C\ (\mu F)$$

Connection of the 0.01μF capacitor ensures the protection period of about 0.3 seconds (the drive is turned OFF when one cycle of Hall input signal exceeds this set time). Be sure to set the time with sufficient allowance, so that the protection circuit is not activated at normal motor startup. For the capacitor, use 4700pF or more. To cancel the lock protection state, take any one of following steps :

- Resetting,
- Maintaining the output duty 0% state by TOC input for the period of tCSD × 2,
- Re-applying the power.

13. Forward/backward operation

For forward/backward changeover during running, the measure is taken to prevent through current at the output (through current caused by the output Tr OFF delay time at a time of changeover). However, changeover during running causes the current exceeding the current limit to flow through the output Tr due to the motor coil resistance and motor counter electro-motive force. It is therefore necessary either to select the external output Tr that does not suffer breakage by this current or to design changeover with the motor speed reduced to a certain degree.

14. FAIL Hall input

The output becomes "L" in following states with the open collector output :

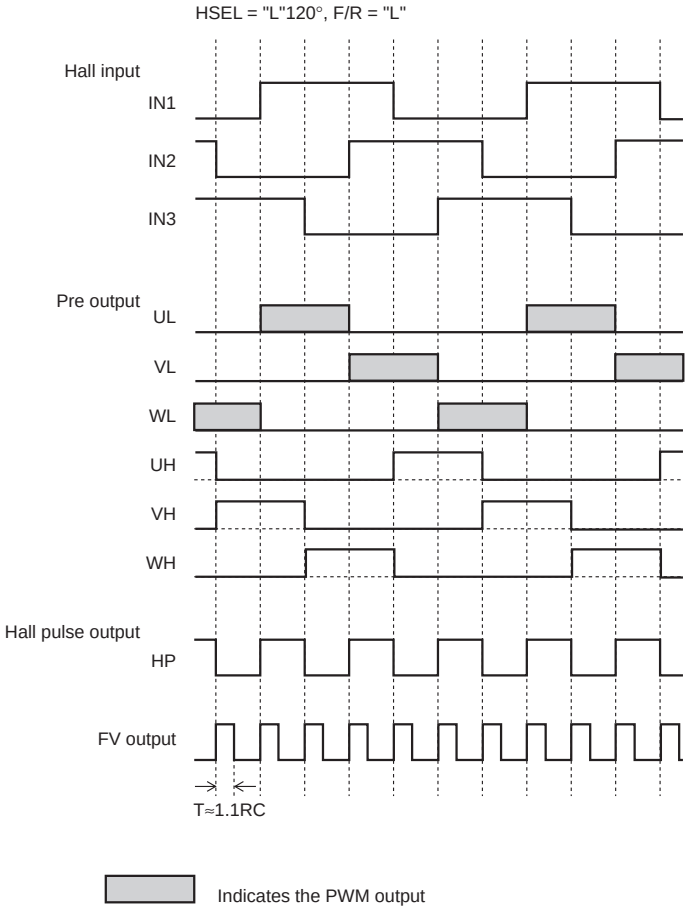
- At abnormal Hall input
- When the low-voltage protection circuit is activated
- When the lock protection circuit is activated
- When the overheat protection circuit is activated

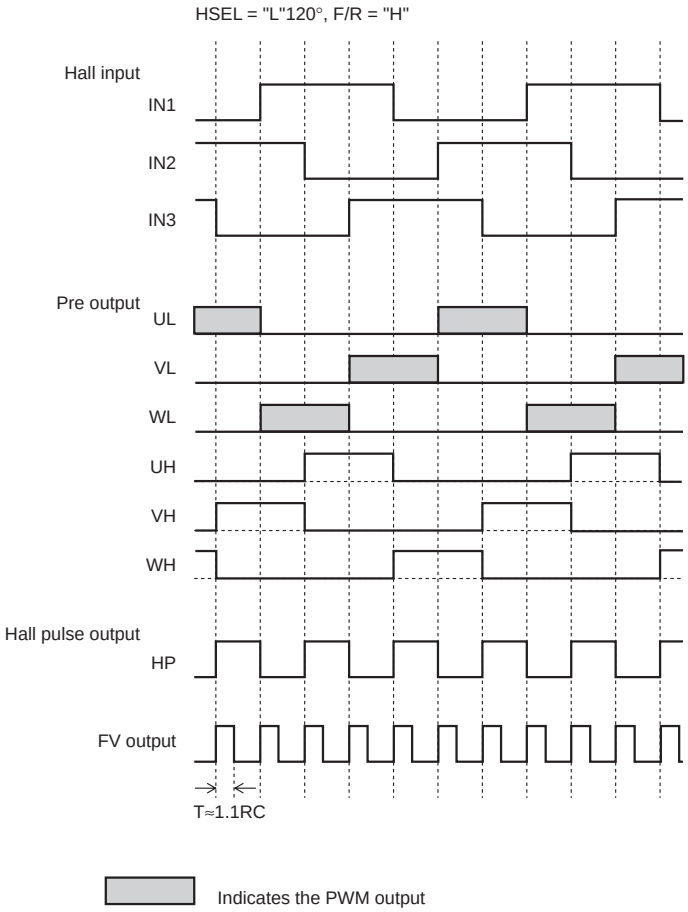
15. HSEL

Phase difference (120° and 60°) can be changed over for the three-phase Hall input.

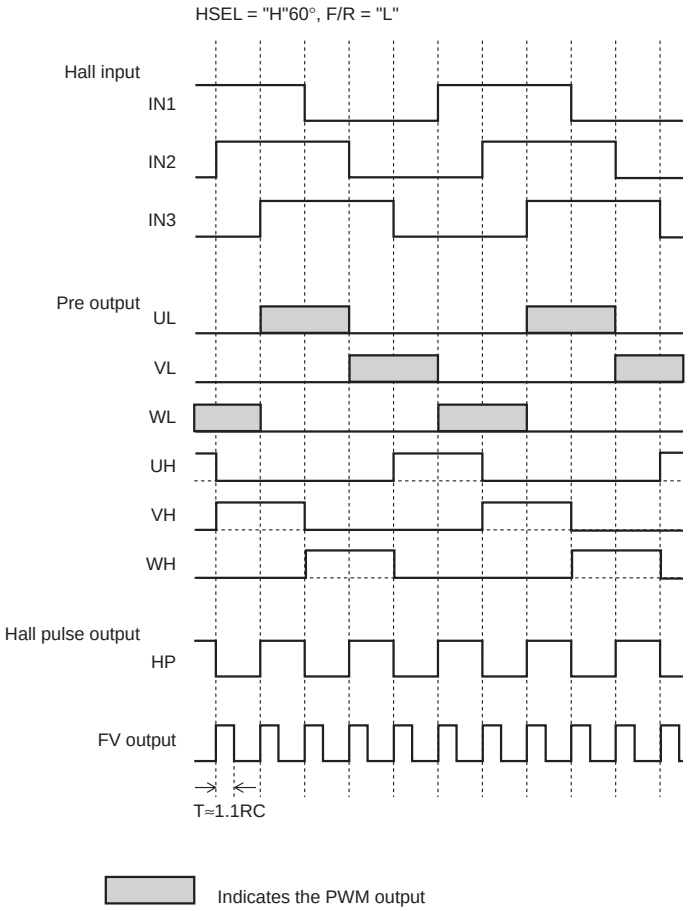
- HSEL = “L” 120°
- HSEL = “H” 60°

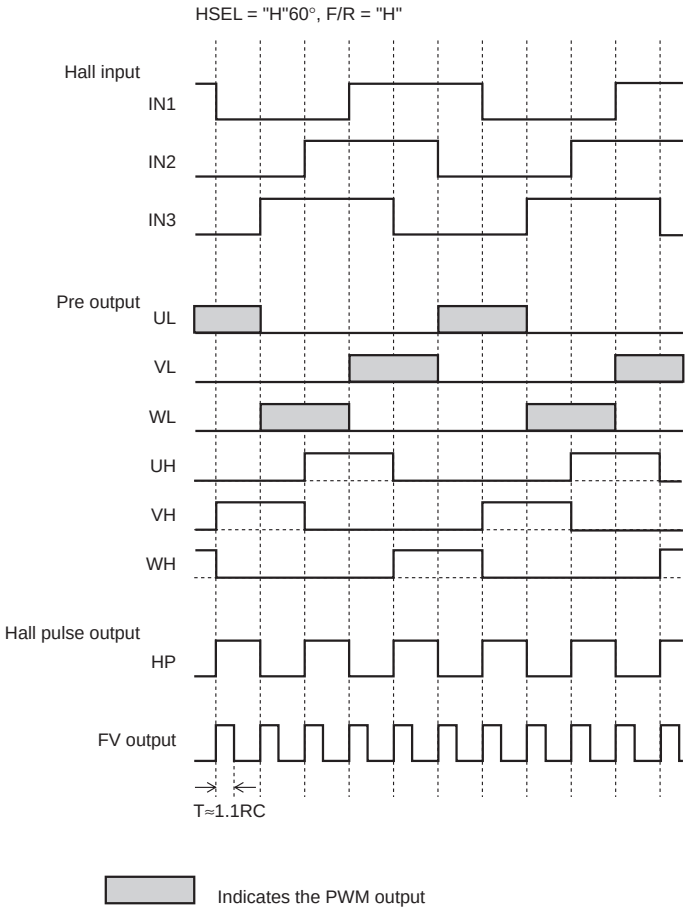
Hall input – each output timing chart (For three-phase Hall input phase difference of 120°)



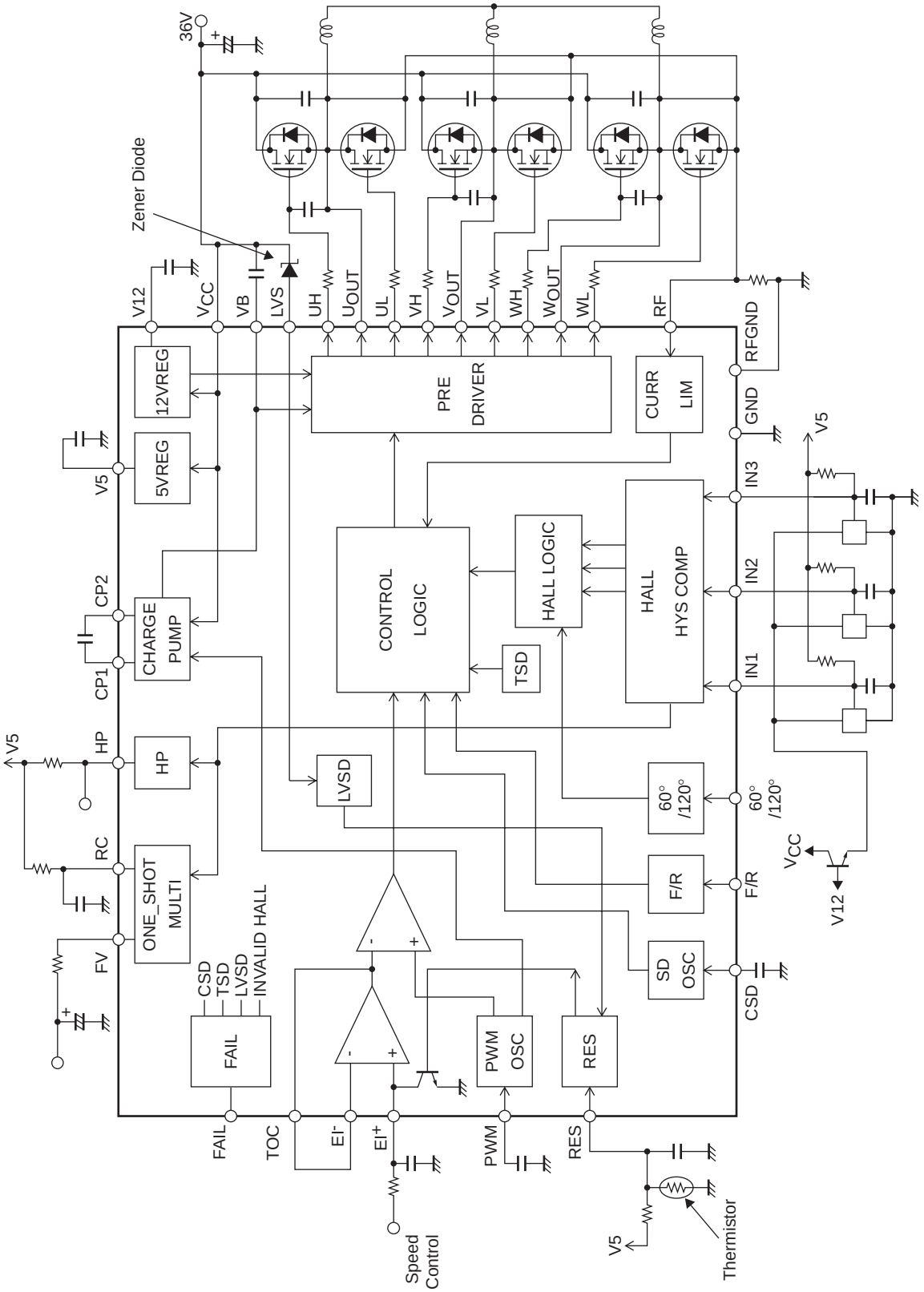


Hall input – each output timing chart (For three-phase Hall input phase difference of 60°)





Sample Application Circuit



Sample Application Circuit

Sample Application (Closed Loop Speed Control)