



# Monolithic digital IC Pre-Driver IC for Brushless Motor Drive in Electric Bicycles

#### Overview

The LB11691 are three-phase bipolar PWM drive pre-driver ICs that allow the output circuits to be implemented using only n-channel FETs. These ICs can implement, at low cost, high-efficiency drive circuits in applications that use motors that require high drive currents. These ICs include a built-in Hall sensor signal F/V conversion circuit and can provide a voltage that is proportional to motor speed for use, for example, in speedometers for electric bicycles. These ICs also support use in applications that holds the speed controlled at a constant rate as the load varies.

#### Features

- Three-phase bipolar PWM drive (high and low side n-channel FET drive)
- Maximum supply voltage : 45V
- Gate drive voltage : about 10V (high and low side n-channel FETs)
- Hall sensor signal F/V conversion circuit (one-shot multivibrator output)
- Synthesized three-phase Hall sensor signal output
- Built-in current limiter and undervoltage protection circuits

#### **Specifications**

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V <sub>CC</sub> max	V <sub>CC</sub> pin	45	V
Supply voltage 2	VB max	VB pin	60	V
Output current 1-1	I <sub>O</sub> max1	UL, VL, and WL pins	50	mA
Output current 2-1	IO max2-1	UH, VH, and WH pins sink current	30	mA
Output current 2-2	IO max2-2	UH, VH, and WH pins source current	40	mA
RF pin application voltage	VRF max		4	V
LVS pin application voltage	VLVS max		60	V

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<u> 声明 LDH09日代別1</u> Parameter	Symbol	Conditions	Ratings	Unit
IN pin application voltage	V <sub>IN</sub> max	IN1, IN2, and IN3 pins	V5+0.3	V
RES pin application voltage	VRES max		V5+0.3	V
TOC pin application voltage	VTOC max		V5+0.3	V
HSEL pin application voltage	VHSEL max		V5+0.3	V
F/R pin application voltage	VFR max		V5+0.3	V
EI+ pin application voltage	VEI+ max		V5+0.3	V
EI- pin application voltage	VEI⁻ max		V5+0.3	V
RC pin application voltage	VRC max		V5+0.3	V
FV pin application voltage	VFV max		V5+0.3	V
HP pin application voltage	VHP max		45	V
FAIL pin application voltage	VFAIL max		45	V
Allowable power dissipation 1	Pd max1	Independent IC	1.5	W
Allowable power dissipation 2	Pd max2	Mounted on a board. *	2.55	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

\* Mounted on a substrate : 114.3×76.1×1.6mm<sup>3</sup>, glass epoxy board.

### Allowable Operating Conditions at $Ta=25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V <sub>CC</sub>	V <sub>CC</sub> pin	15 to 42	V
Supply voltage range 2	VB	VB pin	V <sub>CC</sub> +13	V
Output current 1-1	IOUT <sup>1-1</sup>	UL, VL, and WL pins sink current	45	mA
Output current 1-2	IOUT <sup>1-2</sup>	UL, VL, and WL pins source current	-45	mA
Output current 2-1	I <sub>OUT</sub> 2-1	UH, VH, and WH pins sink current	25	mA
Output current 2-2	I <sub>OUT</sub> 2-2	UH, VH, and WH pins source current	-35	mA
12V constant-voltage output current	I <sub>12REG</sub>		-30	mA
5V constant-voltage output current	I <sub>5REG</sub>		-30	mA
HP pin application voltage	V <sub>HP</sub>		0 to 42	V
HP pin output current	I <sub>HP</sub>		0 to 5	mA
FAIL pin application voltage	VFAIL		0 to 42	V
FAIL pin output current	IFAIL		0 to 5	mA

### Electrical Characteristics $Ta = 25^{\circ}C$ , $V_{CC} = 36V$

Deremeter	Sumbol	Conditions		Unit		
Parameter	Symbol	Conditions	min	typ	max	Unit
Source current	Icc			19	24	mA
5V constant-voltage output (V5 p	pin)	-				
Output voltage	V <sub>5REG</sub>	I <sub>O</sub> = -5mA	4.7	5.0	5.3	V
Voltage fluctuation	∆V5REG1	V <sub>CC</sub> = 15 to 42V		40	100	mV
Load fluctuation	$\Delta V_{5}$ REG2	I <sub>O</sub> = -5 to -30mA		10	30	mV
Temperature coefficient	$\Delta V_{5}$ REG3	Design target value *		0		mV/°C
12 V constant-voltage output (V1	2 pin)	-				
Output voltage	V <sub>12REG</sub>	I <sub>O</sub> = -5mA	11.2	12.0	12.8	V
Voltage fluctuation	$\Delta V_{12REG1}$	V <sub>CC</sub> = 15 to 42V		120	240	mV
Load fluctuation	∆V12REG2	I <sub>O</sub> = -5 to -30mA		10	30	mV
Temperature coefficient	$\Delta V_{12REG3}$	Design target value *		0		mV/°C
Output Block/Conditions : UOUT	= V <sub>OUT</sub> = W <sub>OUT</sub> =	= 18V, VB = 48V applied				
Output H-level voltage 1	V <sub>OH</sub> 1	UL, VL, and WL pins I <sub>OH</sub> = -10mA	V12-1.2	V12-0.8		V
Output L-level voltage 1	V <sub>OL</sub> 1	UL, VL, and WL pins I <sub>OL</sub> = 10mA		0.8	1.2	V
Output H-level voltage 2	V <sub>OH</sub> 2	UH, VH, and WH pins I <sub>OH</sub> = -5mA	46.8	47.2		V
Output L-level voltage 2 V <sub>OL</sub> 2		UH, VH, and WH pins I <sub>OH</sub> = 5mA		18.2	18.6	V

\* : Design target values and not tested.

Charge pump output (VB pin)         VB <sub>OUT</sub> Output voltage         VB <sub>OUT</sub> ICP1 pin           Output Hevel voltage         V <sub>OL</sub> (CP1)         ICP1 = -2mA         V <sub>OC</sub> Integrating amplifier         Integrating amplifier         Integrating amplifier         Integrating amplifier           Input offset voltage         VIO (CONT)         ICP1 = -2mA         ICP1 = -2mA           Common-phase input voltage range         VIO (CONT)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (CONT)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (CONT)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (CONT)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         VIO           Output L-level voltage         V <sub>OL</sub> (PWM)         ITOC = -0.2mA         Ito	min	Ratings			
Output voltage         VB <sub>QUT</sub> CP1 pin         CP1 pin           Output L-level voltage $V_{OL}$ (CP1)         ICP1 = 2mA $V_{CR}$ Integrating amplifier         ICP1         ICP1 = 2mA         Vic           Input offset voltage         VIO (CONT)         ICP1 = 2mA         Vic           Input offset voltage         VIO (CONT)         ICP1 = 2mA         Vic           Input offset voltage         VIO (CONT)         ITOC = -0.2mA         Vic           Output I-level voltage         VO <sub>L</sub> (CONT)         ITOC = -0.2mA         Vic           Output I-level voltage         VO <sub>L</sub> (CONT)         ITOC = -0.2mA         Vic           Output I-level voltage         VO <sub>L</sub> (PWM)         ITOC = -0.2mA         Vic           Output I-level voltage         VO <sub>L</sub> (PWM)         ITOC = -0.2mA         Vic           Output I-level voltage         VO <sub>L</sub> (PWM)         ITOC = -0.2mA         Vic           Socialitation frequency         f (PWM)         C         2.1V         Octoput 1-level voltage         VO <sub>L</sub> (PWM)         Iterase           Socialitation frequency         f (PWM)         C = 270pF         Amplitude         V (PWM)         Iterase         Iterase         Iterase         Iterase         Iterase         Itera	111111	typ	max	Unit	
CP1 pin         Undput H-level voltage $V_{OH}$ (CP1)         ICP1 = 2mA $V_{CQ}$ Output L-level voltage $V_{OL}$ (CP1)         ICP1 = 2mA					
Output H-level voltage $V_{OH}$ (CP1)         ICP1 = 2mA $V_{CI}$ Output L-level voltage $V_{OL}$ (CP1)         ICP1 = 2mA         Integrating amplifier           Input dised voltage         VIO (CONT)         ICD1 = 2mA         Imput bias current         IB (CONT)           Input bias current         IB (CONT)         ICC         Imput bias current         IB (CONT)           Output H-level voltage         VICM (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (CONT)         ITOC = -0.2mA         VI           Output H-level voltage         VOL (PWM)         Imput voltage         Imput voltage         VOL (PWM)           Output H-level voltage         VOL (PWM)         C = 270PF         Imput voltage 1         VTOC1         Output duty 100%         Imput voltage 1         VTOC1         Output duty 100%         Imput voltage 1         VTOC1         Design target value*, 100% at V5 = 5.3V	46.0	48.0	50.5	V	
Output L-level voltage $V_{OL}$ (CP1)ICP1 = 2mAIntegrating amplifierInput offset voltageVIO (CONT)Input bias currentIB (CONT)Common-phase input voltage rangeVICMOutput H-level voltageVOH (CONT)ITOC = -0.2mAV/OHOutput L-level voltageVOH (CONT)ITOC = 0.2mAV/OHOutput L-level voltageVOH (CONT)ITOC = 0.2mAV/OHOutput L-level voltageVOH (CONT)Output L-level voltageVOH (PWM)Output L-level voltageVOH (PWM)Output L-level voltageVOH (PWM)Current IservalICHGVPWM oscillator (PWM pin)VOL (PWM)Output L-level voltageVOH (PWM)Current IservalICHGVPWM oscillator frequencyf (FWM)C = 270pFAmplitudeV (PWM)CCollage 1VTOC1Output duty 100%VIInput voltage 1VTOC1Output duty 0%VIInput voltage 11VTOC1LDesign target value*, 100% at V5 = 4.7VInput voltage 11HVTOC1LDesign target value*, 0% at V5 = 5.3VInput voltage 11HVTOC2LDesign target value*, 0% at V5 = 5.3VInput voltage 2VSDLCurrent limiting circuit (RF pin)Uniter voltageVSDLCancellation voltageVSDLCancellation voltageVSDLCancellation voltageVSDLCancellation voltageVSDLHeat s	r				
Integrating amplifier         Input offset voltage       VIO (CONT)         Input bias current       IB (CONT)         Common-phase input voltage range       VICM         Output H-level voltage       V <sub>OL</sub> (CONT)         ITOC = -0.2mA       ViO         Output L-level voltage       V <sub>OL</sub> (CONT)         ITOC = 0.2mA       ViO         Output L-level voltage       V <sub>OL</sub> (CONT)         PWM oscillator (PWM pin)       ITOC = 0.2mA         Output L-level voltage       V <sub>OL</sub> (PWM)         External C charge current       ICHG         VPWM oscillator (Pewerent)       ICHG         Amplitude       V (PWM)         TOC pin       Input voltage 1         Input voltage 1       VTOC1       Output duty 100%         Input voltage 1       VTOC1       Output duty 00%         Input voltage 1       VTOC1       Output duty 00% at V5 = 4.7V         Input voltage 1L       VTOC2L       Design target value*, 10% at V5 = 4.7V         Input voltage 1H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Input voltage 1H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       Imput voltage       VSDL         Cancellation voltage	′CC <sup>-1.9</sup>	V <sub>CC</sub> -1.4		V	
Input offset voltage VIC (CONT) Input bias current IB (CONT) IF (		1.5	2.0	V	
Input bias current       IB (CONT)         Common-phase input voltage range       VICM         Common-phase input voltage       V <sub>QH</sub> (CONT)         Output L-level voltage       V <sub>QL</sub> (CONT)         Open loop gain       f (CONT) = 1kHz         PWM oscillator (PWM pin)          Output L-level voltage       V <sub>QL</sub> (PWM)         Output L-level voltage       V <sub>QL</sub> (PWM)         Cutput L-level voltage       V <sub>QL</sub> (PWM)         Cutput L-level voltage       V <sub>QL</sub> (PWM)         Cutput L-level voltage       V <sub>QL</sub> (PWM)         Catternal C charge current       ICHG         Doscillation frequency       f (PWM)         C C pin          Input voltage 1       VTOC1         Input voltage 2       VTOC2         Output duty 100%          Input voltage 1L       VTOC1L         Design target value*, 100% at V5 = 4.7V         Input voltage 1L       VTOC2L         Design target value*, 100% at V5 = 4.7V         Input voltage 2L       VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage 2N       VTOC1H         Design target value*, 0% at V5 = 5.3V         Current Imiting circuit (RF pin)         Carrellation voltage<			-		
Common-phase input voltage range       VICM         Output H-level voltage       V <sub>OH</sub> (CONT)       ITOC = -0.2mA       V/O         Output L-level voltage       V <sub>OL</sub> (CONT)       ITOC = 0.2mA       V/O         Open loop gain       f (CONT) = 1kHz       PVM oscillator (PVM pin)       ITOC = 0.2mA       V/O         Output H-level voltage       V <sub>OL</sub> (PVM)       ITOC = 0.2mA       V/O       ITOC = 0.2mA       V/O         Output H-level voltage       V <sub>OL</sub> (PVM)       ITOC = 0.2mA       V/O       ITOC = 0.2mA       V/O         Output H-level voltage       V <sub>OL</sub> (PVM)       ITOC = 0.2mA       V/O       ITOC       ITOC = 0.2mA       V/O       Ito 200	-10		10	mV	
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Open loop gain       f (CONT) = 1kHz         PWM oscillator (PWM pin)         Output L-level voltage $V_{OH}$ (PWM)         Output L-level voltage $V_{OL}$ (PWM)         External C charge current       ICHG         VPWM escillation frequency       f (PWM)         Calilation frequency       f (PWM)         Cancellation voltage       VTOC1       Output duty flow, at V5 = 4.7V         Input voltage 1L       VTOC2L       Design target value*, 100% at V5 = 4.7V         Input voltage 2L       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       Current limiting circuit (RF pin)         Operating voltage       VSDL       Cancellation voltage       VSDL	V5-1.1	V5-0.8		V	
PWM oscillator (PWM pin)         Image: Second		0.8	1.1	V	
Output H-level voltage $V_{OH}$ (PWM)Output L-level voltage $V_{OL}$ (PWM)External C charge currentICHGVPWM = 2.1VOscillation frequencyf (PWM)C = 270pFAmplitudeV (PWM)TOC pinTOC pinInput voltage 1VTOC1Output duty 100%Input voltage 2VTOC2Output duty 0%Input voltage 1LVTOC1LDesign target value*, 100% at V5 = 4.7VInput voltage 2LVTOC2LDesign target value*, 0% at V5 = 4.7VInput voltage 2HVTOC1HDesign target value*, 0% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VCurrent limiting circuit (RF pin)Limiter voltageVSDLLimiter voltageVSDLCancellation voltageVSDHHysteresis width $\Delta$ VSDHeat shielding operation (overheat protection circuit)Heat shielding operationTSDDesign target value*Hysteresis width $\Delta$ TSDDesign target value*(junction temperature)Hysteresis width $\Delta$ TSDDutput L-level voltage $V_{OH}$ (CSD)COutput L-level voltage $V_{OL}$ (CSD)External C charge currentI CHG2VCSD = 2.35VExternal C discharge currentI CHG2VCSD = 2.35VDesign langet value*Oscillation frequencyf (CSD)C = 0.01 $\mu$ F	45	51		dB	
Output L-level voltage $V_{OL}$ (PWM)         External C charge current         ICHG         VPWM = 2.1V           Descillation frequency         f (PWM)         C = 270pF         Input voltage         V           Amplitude         V (PWM)         C = 270pF         Input voltage 1         VTOC1         Output duty 100%         Input voltage 2         VTOC2         Output duty 0%         Input voltage 1         VTOC1         Design target value*, 100% at V5 = 4.7V         Input voltage 2L         VTOC2L         Design target value*, 0% at V5 = 4.7V         Input voltage 2L         VTOC1H         Design target value*, 0% at V5 = 5.3V         Input voltage 2H         VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage 2H         VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage 2H         VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage 2H         VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage 2H         VTOC2H         Design target value*, 0% at V5 = 5.3V         Input voltage         VSD         Input voltage         Input voltage <td></td> <td></td> <td></td> <td></td>					
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ConstructionConstructionOscillation frequencyf (PWM)C = 270pFAmplitudeV (PWM)TOC pinInput voltage 1VTOC1Output duty 100%Input voltage 2VTOC2Output duty 0%Input voltage 1LVTOC1LDesign target value*, 100% at V5 = 4.7VInput voltage 2LVTOC2LDesign target value*, 0% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VCurrent limiting circuit (RF pin)LLimiter voltageVRFLow-voltage protective circuit (LVS pin)Operating voltageVSDLCancellation voltageVSDHHeat shielding operation (overheat protection circuit)Heat shielding operation (overheat protection circuit)Heat shielding operationTSDDesign target value* (junction temperature)Hysteresis width $\Delta$ TSDDesign target value* (junction temperature)CSD circuit (CSD pin)Output L-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OH}$ (CSD)External C discharge currentICHG2VCSD = 2.35VCscillation frequencyAmplitudeV (CSD)	1.0	1.2	1.3	V	
Amplitude       V (PWM)         TOC pin       TOC pin         Input voltage 1       VTOC1       Output duty 100%         Input voltage 2       VTOC2       Output duty 0%         Input voltage 1L       VTOC1       Design target value*, 100% at V5 = 4.7V         Input voltage 2L       VTOC2L       Design target value*, 0% at V5 = 5.3V         Input voltage 1H       VTOC1H       Design target value*, 0% at V5 = 5.3V         Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       Input voltage       VRF         Low-voltage protective circuit (LVS pin)       Operating voltage       VSDL         Cancellation voltage       VSDL       Cancellation voltage       VSDH         Hysteresis width $\Delta VSD$ Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD       Design target value*       (junction temperature)         Hysteresis width $\Delta TSD$ Design target value*       (junction temperature)         CSD circuit (CSD pin)       Output L-level voltage $V_{OH}$ (CSD)       Output L-level voltage       VOL (CSD)         External C charge current	-35	-25	-19	μΑ	
TOC pin       Input voltage 1       VTOC1       Output duty 100%         Input voltage 1       VTOC2       Output duty 0%       Input voltage 1L       VTOC2       Output duty 0%         Input voltage 1L       VTOC1       Design target value*, 100% at V5 = 4.7V       Input voltage 2L       VTOC2L       Design target value*, 0% at V5 = 4.7V         Input voltage 2L       VTOC1H       Design target value*, 0% at V5 = 5.3V       Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V       Current limiting circuit (RF pin)         Limiter voltage       VRF       Input voltage       VSDL         Cancellation voltage       VSDL       Cancellation voltage       VSDH         Hysteresis width $\Delta VSD$ Input voltage       VSD         Heat shielding operation (overheat protection circuit)       Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD       Design target value*       I(junction temperature)         Hysteresis width $\Delta TSD$ Design target value*       I(junction temperature)       CSD circuit (CSD pin)         Output H-level voltage $V_{OH}$ (CSD)       Output L-level voltage $V_{OL}$ (CSD)       External C charge current       ICHG1	29	36	44	kHz	
Input voltage 1       VTOC1       Output duty 100%         Input voltage 2       VTOC2       Output duty 0%         Input voltage 1L       VTOC1L       Design target value*, 100% at V5 = 4.7V         Input voltage 2L       VTOC2L       Design target value*, 0% at V5 = 4.7V         Input voltage 1H       VTOC1H       Design target value*, 0% at V5 = 5.3V         Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       Limiter voltage       VRF         Limiter voltage       VRF          Low-voltage protective circuit (LVS pin)           Operating voltage       VSDL           Cancellation voltage       VSDH           Heat shielding operation (overheat protection circuit)            Heat shielding operation (overheat protection circuit)            Hysteresis width $\Delta$ TSD       Design target value* (junction temperature)          Hysteresis width $\Delta$ TSD       Design target value* (junction temperature)          CSD circuit (CSD pin)              Output H-level voltage       V <sub>OL</sub> (CSD)	1.6	1.8	2.1	Vp-p	
Input voltage 2       VTOC2       Output duty 0%         Input voltage 1L       VTOC1L       Design target value*, 100% at V5 = 4.7V         Input voltage 2L       VTOC2L       Design target value*, 0% at V5 = 4.7V         Input voltage 1H       VTOC1H       Design target value*, 0% at V5 = 5.3V         Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       Limiter voltage       VRF         Low-voltage protective circuit (LVS pin)       Operating voltage       VSDL         Cancellation voltage       VSDH       Person and target value*         Heat shielding operation (overheat protection circuit)       Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD       Design target value*         (junction temperature)       Hysteresis width $\Delta$ TSD         Hysteresis width $\Delta$ TSD       Design target value*         (junction temperature)       CDuctor temperature)       CDuctor temperature)         Mysteresis width $\Delta$ TSD       Design target value*       (junction temperature)         CSD circuit (CSD pin)       Cutput H-level voltage       V <sub>OL</sub> (CSD)       Cutput H-level voltage       V <sub>OL</sub> (CSD)         Cutput H-level voltage       V <sub>OL</sub> (CSD)       Cutput -level voltage					
Input voltage 1LVTOC1LDesign target value*, 100% at V5 = 4.7VInput voltage 2LVTOC1LDesign target value*, 0% at V5 = 4.7VInput voltage 1HVTOC1HDesign target value*, 100% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VCurrent limiting circuit (RF pin)Input voltage protective circuit (LVS pin)Operating voltageVRFLow-voltage protective circuit (LVS pin)Operating voltageVSDLCancellation voltageVSDHHeat shielding operation (overheat protection circuit)Heat shielding operationTSDtemperatureDesign target value* (junction temperature)Hysteresis width $\Delta$ TSDDoutput H-level voltageVO <sub>H</sub> (CSD)Output L-level voltageVO <sub>L</sub> (CSD)External C charge currentICHG1VCSD = 2.35VCSDExternal C discharge currentICHG2VCSD)C = 0.01 $\mu$ FAmplitudeV (CSD)	2.72	3.0	3.30	V	
Input voltage 2LVTOC2LDesign target value*, 0% at V5 = 4.7VInput voltage 1HVTOC1HDesign target value*, 100% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VCurrent limiting circuit (RF pin)Limiter voltageVRFLimiter voltageVRFLow-voltage protective circuit (LVS pin)Operating voltageVSDLOperating voltageVSDHHysteresis width $\Delta$ VSDHeat shielding operation (overheat protection circuit)Heat shielding operationHysteresis width $\Delta$ TSDDesign target value* (junction temperature)Hysteresis width $\Delta$ TSDDesign target value* (junction temperature)CSD circuit (CSD pin)Output H-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OL}$ (CSD)External C charge currentICHG1VCSD = 2.35VExternal C discharge currentICHG2VCSD = 2.35VOscillation frequencyf (CSD)C = 0.01 \muFAmplitudeV (CSD)	0.99	1.2	1.34	V	
Input voltage 1HVTOC1HDesign target value*, 100% at V5 = 5.3VInput voltage 2HVTOC2HDesign target value*, 0% at V5 = 5.3VCurrent limiting circuit (RF pin)Limiter voltageVRFLow-voltage protective circuit (LVS pin)Operating voltageVSDLCancellation voltageVSDHHysteresis width $\Delta VSD$ Heat shielding operation (overheat protection circuit)Heat shielding operationTSDLysteresis width $\Delta TSD$ Hysteresis width $\Delta TSD$ Design target value* (junction temperature)Hysteresis width $\Delta TSD$ Design target value* (junction temperature)CSD circuit (CSD pin)Output H-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OL}$ (CSD)External C charge currentICHG1VCSD = 2.35VICHG2Oscillation frequencyf (CSD)Carlend C discharge currentICHG2VCSD = 2.35VICHG2Oscillation frequencyf (CSD)Cordupt C discharge currentICHG2V (CSD)ICHG2Descillation frequencyf (CSD)Cordupt C discharge currentICHG2VCSD = 2.35VICHG2Descillation frequencyf (CSD)Cordupt C discharge currentICHG2CSD (CSD)ICHG2Cordupt C discharge currentICHG2CSD (CSD)ICHG2Cordupt C discharge currentICHG2COSD (ICSD)ICHG2Cordupt C discharge cu	2.72	2.80	2.90	V	
Input voltage 2H       VTOC2H       Design target value*, 0% at V5 = 5.3V         Current limiting circuit (RF pin)       VRF         Limiter voltage       VRF         Low-voltage protective circuit (LVS pin)       Operating voltage       VSDL         Operating voltage       VSDL       Cancellation voltage       VSDH         Hysteresis width $\Delta VSD$ Meat shielding operation (overheat protection circuit)         Heat shielding operation (overheat protection circuit)       Design target value* (junction temperature)       Concellation temperature)         Hysteresis width $\Delta TSD$ Design target value* (junction temperature)       CSD circuit (CSD pin)         Output H-level voltage $V_{OH}$ (CSD)       Cancellation temperature)       CSD circuit CSD pin)         Output L-level voltage       VOL (CSD)       Cancellation temperature)       CSD circuit (CSD pin)         Output L-level voltage       VOL (CSD)       Cancellation temperature)       Concellation temperature)         Output L-level voltage       VOL (CSD)       Cancellation temperature)       Cancellation temperature)         Output L-level voltage       VOL (CSD)       Cancellation temperature)       Cancellation temperature)         Collation frequency       f (CSD)       C = 0.01 $\mu$ F       Cancellation temperature)       Cancellation temperature) <td>0.99</td> <td>1.08</td> <td>1.17</td> <td>V</td>	0.99	1.08	1.17	V	
Current limiting circuit (RF pin)         Limiter voltage       VRF         Low-voltage protective circuit (LVS pin)         Operating voltage       VSDL         Cancellation voltage       VSDH         Hysteresis width $\Delta$ VSD         Heat shielding operation (overheat protection circuit)         Heat shielding operation (overheat protection circuit)         Heat shielding operation         TSD       Design target value*         (junction temperature)         Hysteresis width $\Delta$ TSD         Design target value*         (junction temperature)         Hysteresis width $\Delta$ TSD         Design target value*         (junction temperature)         CSD circuit (CSD pin)         Output H-level voltage       V <sub>OL</sub> (CSD)         Output L-level voltage       V <sub>OL</sub> (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C = 0.01 \mu F         Amplitude       V (CSD)       C	3.08	3.20	3.30	V	
Limiter voltage       VRF         Low-voltage protective circuit (LVS pin)         Operating voltage       VSDL         Cancellation voltage       VSDH         Hysteresis width $\Delta VSD$ Heat shielding operation (overheat protection circuit)         Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD         Design target value*         (junction temperature)         Hysteresis width $\Delta TSD$ Design target value*         (junction temperature)         Hysteresis width $\Delta TSD$ Design target value*         (junction temperature)         CSD circuit (CSD pin)         Output H-level voltage $V_{OH}$ (CSD)         Output L-level voltage $V_{OL}$ (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C         Amplitude       V (CSD)       C	1.11	1.22	1.34	V	
Jost Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"Colspan="2					
Operating voltage       VSDL         Cancellation voltage       VSDH         Hysteresis width $\Delta$ VSD         Heat shielding operation (overheat protection circuit)         Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD         Design target value*         (junction temperature)         Hysteresis width $\Delta$ TSD         Design target value*         (junction temperature)         CSD circuit (CSD pin)         Output H-level voltage       V <sub>OH</sub> (CSD)         Output L-level voltage       V <sub>OL</sub> (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C = 0.01 $\mu$ F	85	100	115	mV	
Cancellation voltage       VSDH         Hysteresis width $\Delta$ VSD         Heat shielding operation (overheat protection circuit)         Heat shielding operation temperature         Heat shielding operation         TSD       Design target value*         (junction temperature)         Hysteresis width $\Delta$ TSD         Design target value*         (junction temperature)         CSD circuit (CSD pin)         Output H-level voltage $V_{OH}$ (CSD)         Output L-level voltage $V_{OL}$ (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C = 0.01 \mu F         Amplitude       V (CSD)       C		•			
$\Delta VSD$ $\Delta VSD$ Heat shielding operation (overheat protection circuit)         Heat shielding operation temperature       TSD       Design target value* (junction temperature)         Hysteresis width $\Delta TSD$ Design target value* (junction temperature)         Hysteresis width $\Delta TSD$ Design target value* (junction temperature)         CSD circuit (CSD pin)       Design target value       Output H-level voltage $V_{OH}$ (CSD)         Output L-level voltage $V_{OL}$ (CSD)       External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V       Oscillation frequency       f (CSD)       C         Amplitude       V (CSD)       C<= 0.01 $\mu$ F       C       C       C       C	3.65	3.85	4.05	V	
Heat shielding operation (overheat protection circuit)         Heat shielding operation       TSD       Design target value*         temperature       (junction temperature)         Hysteresis width $\Delta TSD$ Design target value*         (junction temperature)       (junction temperature)         CSD circuit (CSD pin)       0         Output H-level voltage $V_{OH}$ (CSD)         Output L-level voltage $V_{OL}$ (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C         Amplitude       V (CSD)       C	4.15	4.35	4.55	V	
Heat shielding operation temperatureTSDDesign target value* (junction temperature)Hysteresis width $\Delta TSD$ Design target value* (junction temperature)CSD circuit (CSD pin)0Output H-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OL}$ (CSD)External C charge currentICHG1VCSD = 2.35VExternal C discharge currentICHG2VCSD = 2.35VOscillation frequencyf (CSD)CSDC = 0.01 $\mu$ F	0.35	0.5	0.65	V	
temperature(junction temperature)Hysteresis width $\Delta TSD$ Design target value* (junction temperature)CSD circuit (CSD pin) $V_{OH}$ (CSD)Output H-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OL}$ (CSD)External C charge currentICHG1VCSD = 2.35VExternal C discharge currentICHG2VCSD = 2.35VOscillation frequencyf (CSD)C = 0.01 $\mu$ FAmplitudeV (CSD)					
Hysteresis width $\Delta TSD$ Design target value* (junction temperature)CSD circuit (CSD pin)Output H-level voltage $V_{OH}$ (CSD)Output L-level voltage $V_{OL}$ (CSD)External C charge currentICHG1VCSD = 2.35VExternal C discharge currentICHG2VCSD = 2.35VOscillation frequencyf (CSD)C = 0.01 $\mu$ FAmplitudeV (CSD)	150	170		°C	
(junction temperature)         CSD circuit (CSD pin)         Output H-level voltage       V <sub>OH</sub> (CSD)         Output L-level voltage       V <sub>OL</sub> (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C = 0.01 µF         Amplitude       V (CSD)       C = 0.01 µF					
CSD circuit (CSD pin)         Output H-level voltage       V <sub>OH</sub> (CSD)         Output L-level voltage       V <sub>OL</sub> (CSD)         External C charge current       ICHG1       VCSD = 2.35V         External C discharge current       ICHG2       VCSD = 2.35V         Oscillation frequency       f (CSD)       C = 0.01 µF         Amplitude       V (CSD)       C = 0.01 µF		40		°C	
Output H-level voltage     V <sub>OH</sub> (CSD)       Output L-level voltage     V <sub>OL</sub> (CSD)       External C charge current     ICHG1     VCSD = 2.35V       External C discharge current     ICHG2     VCSD = 2.35V       Oscillation frequency     f (CSD)     C = 0.01 µF       Amplitude     V (CSD)     V					
Output L-level voltage     VOL (CSD)       External C charge current     ICHG1     VCSD = 2.35V       External C discharge current     ICHG2     VCSD = 2.35V       Oscillation frequency     f (CSD)     C = 0.01 µF       Amplitude     V (CSD)     V	3.2	3.6	4.0	V	
External C charge current     ICHG1     VCSD = 2.35V       External C discharge current     ICHG2     VCSD = 2.35V       Oscillation frequency     f (CSD)     C = 0.01μF       Amplitude     V (CSD)     V	0.9	3.0 1.1		V	
External C discharge current     ICHG2     VCSD = 2.35V       Oscillation frequency     f (CSD)     C = 0.01µF       Amplitude     V (CSD)     V		-10	1.3		
Oscillation frequency     f (CSD)     C = 0.01μF       Amplitude     V (CSD)	-14 7		-6 15	μA A	
Amplitude V (CSD)	/	11	15	μΑ	
		180	0.75	Hz	
Peacet aircuit (PES nin)	2.2	2.5	2.75	Vp-p	
Reset circuit (RES pin)	4 47	4 07	4 07		
Reset operating voltage VRESL	1.17	1.27	1.37	V	
Reset canceling voltage VRESH	1.37	1.5	1.63	V	
Hysteresis width ΔVRES	0.20	0.23	0.26	V	
HP pin		<u> </u>	T		
Output saturation voltage         VHPL         IO = 3mA		0.15	0.5	V	

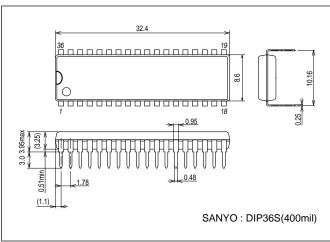
\* : Design target values and not tested.

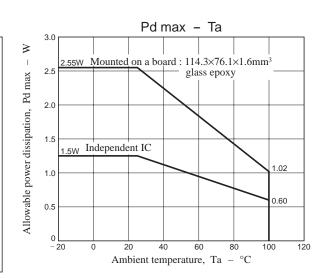
	Symbol	Conditions		Ratings		Unit
T diamotor	Cymbol		min	typ	max	Onic
FAIL pin		-				
Output saturation voltage	VFLL	I <sub>O</sub> = 3mA		0.15	0.5	V
Output leak current	IFL leak	VFAIL = 42V			10	μΑ
RC pin						
Output H-level voltage	V <sub>OH</sub> (RC)		3.22	3.5	3.78	V
Output L-level voltage	V <sub>OL</sub> (RC)		0.72	0.8	0.88	V
Clamp voltage	VCLP (RC)			1.5		V
FV pin						
Charge current	ICHG1	VFV = 2.5V	-420	-300	-230	μA
Discharge current	ICHG2	VFV = 1V	1.3	2.5	5.0	mA
IN1, IN2, and IN3 pins			<u>_</u>	•		
H-level input voltage	V <sub>IH</sub> (IN)		4.0		V5	V
L-level input voltage	V <sub>IL</sub> (IN)		0		2.5	V
Input open voltage	V <sub>IO</sub> (IN)		V5-0.5		V5	V
Hysteresis width	V <sub>IS</sub> (IN)		0.55	0.9	1.25	V
H-level input current	I <sub>IH</sub> (IN)	V <sub>IN</sub> = V5	-10	0	10	μΑ
L-level input current	I <sub>IL</sub> (IN)	$V_{IN} = 0V$		-500		μA
F/R pin				•	•	
H-level input voltage	V <sub>IH</sub> (FR)		2.0		V5	V
L-level input voltage	V <sub>IL</sub> (FR)		0		1.0	V
Input open voltage	V <sub>IO</sub> (FR)		2.6	2.9	3.2	V
Hysteresis width	V <sub>IS</sub> (FR)		0.16	0.25	0.34	V
H-level input current	I <sub>IH</sub> (FR)	VF/R = V5		100	130	μΑ
L-level input current	I <sub>IL</sub> (FR)	VF/R = 0V	-170	-130		μΑ
HSEL pin	•	•				
H-level input voltage	V <sub>IH</sub> (HSL)		2.0		V5	V
L-level input voltage	V <sub>IL</sub> (HSL)		0		1.0	V
Input open voltage	V <sub>IO</sub> (HSL)		2.6	2.9	3.2	V
H-level input current	I <sub>IH</sub> (HSL)	VHSEL = V5		100	130	μA
L-level input current	IIL (HSL)	VHSEL = 0V	-170	-130		μA

## Package Dimensions

unit : mm (typ)

3170A





## The Bhase legicatruth table

(1)120° (HSEL = "L")

		F/R = "L"		F/R = "H"					
	IN1	IN2	IN3	IN1	IN2	IN3	Upper side gate	Lower side gate	HP
1	Н	L	Н	L	н	L	VH	UL	Н
2	Н	L	L	L	Н	Н	WH	UL	L
3	Н	Н	L	L	L	Н	WH	VL	н
4	L	н	L	Н	L	Н	UH	VL	L
5	L	Н	Н	Н	L	L	UH	WL	Н
6	L	L	Н	Н	Н	L	VH	WL	L

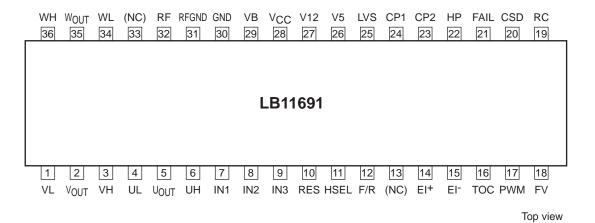
#### (2)60° (HSEL = "H")

		F/R = "L"		F/R = "H"					
	IN1	IN2	IN3	IN1	IN2	IN3	Upper side gate	Lower side gate	HP
1	н	Н	Н	L	L	L	VH	UL	Н
2	L	Н	Н	Н	L	L	WH	UL	L
3	L	L	Н	Н	Н	L	WH	VL	Н
4	L	L	L	Н	Н	Н	UH	VL	L
5	Н	L	L	L	Н	Н	UH	WL	Н
6	Н	Н	L	L	L	Н	VH	WL	L

• The condition with the upper gate = VH and the lower gate = UL corresponds to a state in which the upper FET is turned ON when the VH pin is connected and the lower FET is turned ON when the UL pin is connected.

• The HP output is an open collector output. Therefore, "H" level corresponds to an open state.

### **Pin Assignment**



Pin No.	Pin Name	Description
1	VL	Lower Nch power FET gate drive output pins.
4	UL	
34	WL	
2	VOUT	Upper Nch power FET source voltage detection pins.
5	UOUT	
35	WOUT	
3	VH	Upper Nch power FET gate drive output pin.
6 26	UH WH	
36 7	IN1	Hall input pins. A capacitor is connected for stabilization between these pins and GND.
8	IN1 IN2	
9	IN3	
10	RES	Reset pin. A resistor is connected between this pin and V5 while a capacitor is connected between this pin and GND.
11	HSEL	Reset pin. Connect the resistance between this pin and V5 and the capacitor between this pin and GND.
12	F/R	Pin for changeover of the phase difference of three-phase Hall input (120° and 60°). HSEL = "L" 120°, HSEL = "H" 60°
14	EI+	Integrating amplifier non-inverted input pin.
15	EI	Integrating amplifier inverted input pin.
16	TOC	PWM waveform comparison pin (integrating amplifier output pin).
17	PWM	PWM oscillation frequency set pin. Connect a capacitor between this pin and GND.
18	FV	Hall signal one-shot multi-pulse output.
19	RC	One-shot multi-pulse width set pin. A resistor is connected between this pin and V5 while a capacitor is connected between this pin and GND.
20	CSD	Pin to set the operation time of the lock protection circuit. Connect the capacitor between this pin and GND.
21	FAIL	Open collector output, with the output being "L" in following cases : Abnormal Hall input, activation of the low-voltage protection circuit, activation of the lock protection circuit, and activation of the overheat protection circuit.
22	HP	Hall signal three-phase composite output pin (open collector output).
23 24	CP2 CP1	Charge pump capacitor output pin. A capacitor is connected between CP1 and CP2.
25	LVS	Low-voltage protective voltage detection pin. A Zener diode is connected in series to set the detection voltage when the supply voltage of 5V or more is to be detected.
26	V5	5V power pin (control circuit power supply). A capacitor is connected between this pin and GND.
27	V12	12V power pin (UL, VL, and WL output power supply). A capacitor is connected between this pin and GND.
28	VCC	Power pin. A capacitor is connected for stabilization between this pin and GND.
29	VB	Charge pump output pins (UH, VH, and WH output power supply). A capacitor is connected between this pin and V $_{ m CC}$ .
30	GND	GND pin.
31	RFGND	GND sensing pin, which is connected to the GND side of low-resistance RF connected to the RF pin.
32	RF	Output current detection pin. Low-resistance RF is connected between RF and GND.
		The output current is limited to the value set with $I_{OUT} = 0.1/RF$ . (Current limiting circuit)
13 33	NC	These can be used as wiring because they are not connected with the internal parts.

Pin Des	scription		
富调	Cription Den Name	应商 Description	Equivalent Circuit
1	VL	Output pin	V12
4	UL	(Gate driving output pin of lower Nch power FET)	
34	WL	For duty control	
			ζ ≸50kΩ ▲
2	VOUT	Voltage detection pin	
5	UOUT	(Source voltage detection pin of upper Nch power	VB
35	WOUT	FET)	
		,	
			ξ50kΩ
3	VH	Output pin	
3 6	UH	(Gate driving output pin of lower Nch power FET)	
6 36	WH	(Cate driving output pill of lower Not power FET)	
50	****		
			<i>m</i>
7	IN1	Hall input pin	
8	IN2	"H" in the open condition.	<u>V5</u>
8 9	IN3	Connect a capacitor to GND for stabilization.	
3	INS	Connect a capacitor to GND for stabilization.	8κΩ ξ
10	RES	Reset pin	
10	1120		<u>V5</u>
			the the the the
11	HSEL	Pin to change over the phase difference of	
		three-phase Hall input	<u>V5</u>
		HSEL = "L" 120°	(↓) 30kΩ ≨ <b>⊥</b>
		$HSEL = "H" 60^{\circ}$	
			540
			-
			40kΩ \$ <b>★</b>
	1		

Continued fr	om preceding pag	代应商	
			Equivalent Circuit
12 14	EI+	Description Forward/backward input pin Integrating amplifier non-inverted input pin	Equivalent Circuit V5 $30k\Omega \ge 5k\Omega$ $40k\Omega \ge 12$ $40k\Omega \ge 12$ 40
15	EI-	Integrating amplifier inverted input pin	
16	тос	Integrating amplifier output pin (PWM waveform comparison pin)	V5
17	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND.	V5 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
18	FV	Hall signal one-shot multi-pulse output pin	

	rom preceding page D 1 0 1 1 7 Pin Name	Description	Equivalent Circuit
19	RC	One-shot multi-pulse width setting pin	V5
		Connect a resistor between this pin and V5 and a capacitor between this pin and GND.	
20	CSD	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND.	<u>V5</u>
21	FAIL	Open collector output, with the output being "L" in following cases :	
		Abnormal Hall input, activation of the low-voltage protection circuit, activation of the lock protection	() ()
		circuit, and activation of the overheat protection circuit	
			<i>m m m</i>
22	HP	Hall signal three-phase composite output pin (Open collector output)	
			() (22)
23	CP2	Charge pump capacitor connection pin	
		Connect a capacitor between CP1 and CP2.	
			<i>≩</i> 50Ω
			VB 300Ω (23)
			¥ ,
24	CP1		V <sub>CC</sub>
			(24) 300Ω
			Continued on next page.

	om preceding pag	<del>应商</del> Description	Equivalent Circuit
 25	LVS	Low-voltage protective voltage detection pin	
		When the 5V or more supply voltage is to be detected, connect Zener diode in series and set the detection voltage.	V5 46kΩ 25 18kΩ π π π π π π
26	V5	Stabilization power supply output pin (5V output) Connect a capacitor (about 0.1µF) between this pin and GND for stabilization	Vcc
27	V12	Stabilization power supply output pin (12V output) Connect a capacitor (about 0.1µF) between this pin and GND for stabilization.	V <sub>C</sub> C
28	V <sub>CC</sub>	Power pin Connect a capacitor (about 0.1µF) between this pin and GND for stabilization	
29	VB	Charge pump output pin (UH, VH, and WH output power supply) Connect a capacitor between this pin and V <sub>CC</sub> .	
30	GND	GND pin	
31	RF GND	Connected to GND of external Rf resistor.	

Continued fr	om preceding pag DI 100111 Pin Name	应商 Description	Equivalent Circuit
32	RF	Output current detection pin. Connect the low resistance Rf between this pin and GND. Set with the output maximum current I <sub>OUT</sub> = 0.1/Rf.	
13 33	NC	These can be used as wiring because they are not connected with the internal parts.	

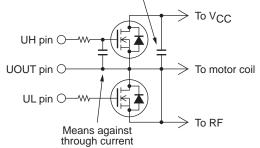
#### Description of LB11691 查询 LB11691 供应商

#### 1. Output drive circuit

This IC is designed on the prerequisite that NchFET is used for both upper and lower outputs. To minimize power loss at the output, the direct PWM drive method is used. Output Tr is normally saturated at ON and the motor drive power is adjusted by changing the ON-duty of the output. PWM switching of the output is made on the lower output side to which UL, VL, and WL pins are connected. Diode built into the upper output FET on the non-PWM side should be selected with care because the reverse recovery time is important (the through current flows in an instant when the PWM side Tr is turned ON if the diode with the short reverse recovery time is not used).

Near each three-phase output FET, provide a capacitor to prevent high-frequency oscillation (about  $0.1\mu$ F) because of substrate pattern routing.

If the switching speed of FET is so high as to cause a problem, insert a series resistor to the gate to adjust the speed. Through current may flow if the ON speed of lower FET on the PWM side is too fast. However, insertion of excessively large resistor in the gate may make the gate waveform dull and the gate voltage may be deficient when the PWM on-duty is small, resulting in heat generation or damage of the lower FET. The same phenomena occur if the FET gate capacity is large even when the resistor has not been inserted. In this case, it is For oscillation prevention



necessary to limit the minimum duty to be used by taking into account ASO of the switching element to be used. Depending on FET to be used, the through current may flow when the PWM on-duty is small. As a countermeasure, a capacitor may be inserted between the gate and source of upper FET. Note that insertion of a capacitor with excessively high capacitance may delay switching too much, resulting in heat generation in the upper FET.

#### 2. Current limiting circuit

The current limiting circuit limits the current to the value determined by I = VRF/Rf (VRF = 0.1Vtyp, Rf : current detection resistance) (that is, the peak current is limited). Current is limited by decreasing on-duty of the output.

Connection of RF and RFGND pins to both ends near the current detection resistor ensures operation with the correct current limiting value. When the current detection resistor with extremely small resistance is to be used, the pattern design must be such as to ensure the equal wiring resistance component by substrate pattern for all phases as much as possible. If the wiring resistance component varies among phases, the current limit value fluctuates each time the shift is changed, resulting in vibration or noise in the motor.

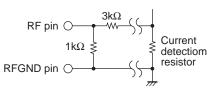
The reference voltage has been set to 0.1Vtyp to minimize the power of current detection resistor. In certain applications, enter the voltage divided by the resistor into RF pin when the current detection resistance is to be increased. For the resistance ratio shown in the figure right, the detection current value may be increased by about four times.

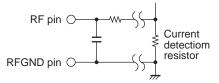
The current limiting circuit has a filter circuit so that erroneous current limiting is not made when the circuit detects the reverse recovery current of the output diode because of PWM operation. In the normal application, the internal filter circuit is allowed. If erroneous limiting occurs (if the reverse recovery current of diode flows for  $1\mu$ S or more), it is necessary to add the external filter circuit (R and C low-path filter). Note also that excessive delay may cause delay in detection of current limiting.

#### 3. PWM oscillation circuit

The PWM frequency is determined from a capacitor capacity C (F) to be connected to the PWM pin : fPWM  $\approx 1/(102000 \times C)$ 

Connection of a 270pF capacitor causes oscillation of about 36kHz. Excessively low PWM frequency causes a switching sound from the motor while excessively high PWM frequency causes increase in the power loss at output. Therefore, the PWM frequency of about 20k to 50kHz would be acceptable. Wire GND of a capacitor to be connected as much near as possible to the GND pin of IC to prevent effects of output noise.

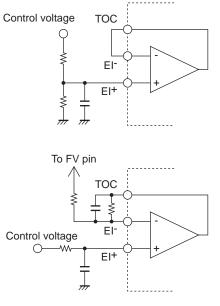




## 4\_Control method

查询"LB11691"供应商 The omplit duty is determined from comparison between the PWM oscillation waveform and TOC pin voltage. The duty becomes 0% when the TOC pin voltage is about 1.2V or less and 100% when the pin voltage is about 3.0V or more.

Normally, the integrating amplifier is used as a full return amplifier (EI- pin and TOC pin connected) and the control voltage is entered to EI+ pin. (The output duty increases with increasing EI<sup>+</sup> pin voltage.) At resetting with the RES pin, the EI+ pin is lowered approximately to the GND voltage by IC internal TR (for capacitor discharge). Therefore, always enter the voltage via resistor, instead of direct connection of the low-impedance power. Also connect a pull-down resistor between the EI+ pin and GND to prevent the motor from being driven when the control voltage is open. When the control voltage contains noise or in order to suppress sudden fluctuation of the control voltage, connect a capacitor between the EI+ pin and GND to remove the noise. The operating voltage range of control input can be widened by entering the voltage divided by the resistor into the EI<sup>+</sup> pin, as shown in the figure right.



To perform control while keeping the rotation speed constant to a certain degree under load fluctuation, the speed control circuit with FV pin output may be formed as shown in the right. Select a  $25k\Omega$  or more resistance to be inserted between FV and EI- pins. Select the return capacitor capacity so that the TOC pin voltage is sufficiently stable at low speed.

#### 5. Charge pump circuit

The voltage is raised by the charge pump circuit, generating the gate voltage of upper output FET. The voltage is raised by a capacitor CP connected between CP1 and CP2 pins, accumulating the charge in the capacitor CB between VB and VCC pins. The capacitance value of CP and CB must always have the following relationship :

 $CB \ge 4 \times CP$ 

CP capacitor charge and discharge are made on the basis of PWM cycle. Though the VB power supply current capacity increases with increasing capacity of the CP capacitor, excessively large capacity may cause faulty charge/discharge operation. The VB voltage becomes more stable when the CB capacitor capacity is larger, but excessively large capacity causes longer time of VB voltage generation at a time of power ON. Set the capacity of CP and CB by referring to the table below.

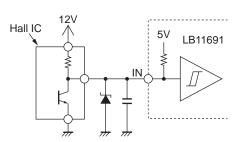
When the V<sub>CC</sub> voltage decreases below 20V, the current capacity of VB power supply deteriorates suddenly, causing drop of VB voltage. Therefore, due care must be taken when designing.

V <sub>CC</sub> voltage	24V	36V
CP	0.1µF	6800pF
СВ	1μF	0.47µF

#### 6. Hall input signal

Connect the Hall IC output to the Hall input. As an about  $10k\Omega$  pull-up resistor is incorporated for the 5V regulator, it is normally not necessary to connect the pull-up resistor externally. If the Hall IC with built-in pull-up resistor is used, it is enough to use the Hall IC power supply with 5V. If the Hall IC power supply is to be used with 12V, it is necessary to add the pull-down resistor or voltage clamp Zener diode to prevent application of voltage of 5V or more to the Hall input.

The input is a comparator input with about 0.9V hysteresis width. If the noise presents problem, connect a noise removing capacitor between the input and GND.



When three inputs of Hall input signal are in the same input condition, both upper and lower outputs are turned OFF.

## 7\_Low-voltage protective circuit

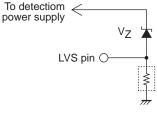
The low-voltage protective circuit performs detection using the voltage applied to the LVS pin and turns OFF all drive outputs when the voltage drops below the operating voltage (3.85Vtyp). The circuit has hysteresis to prevent repetition of ON/OFF near the protected operating voltage. The output is not recovered when the voltage does not rise by about 0.5V above the operating voltage. In the protection operation, the RES pin voltage

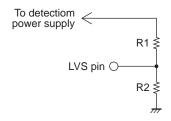
becomes "L" too. The protection operating voltage is based on the 5V system detection level. To raise the detection level, connect Zener diode in series to the LVS pin and shift the detection level (detection voltage = 3.85Vtyp+Vz). The LVS pin inrush current at detection is about 62µA. If it is necessary to stabilize rise of the Zener diode voltage and to suppress fluctuation of the Zener voltage, insert a resistor between LVS pin and GND to increase the diode current. The detection voltage may also be raised, without using Zener diode, by resistive potential division. When connection as shown in the right is made;

Detection voltage  $\approx ((3.85 \div R2) + 62\mu A) \times (R1+R2)$ 

Cancellation voltage  $\approx ((4.35 \div R2) + 70\mu A) \times (R1+R2)$ 

With  $R1 = 13k\Omega$  and  $R2 = 2.2k\Omega$ , the detection voltage becomes about 28V while the cancellation voltage becomes about 32V. Pay due attention when raising R2 because the error of detection voltage may increase because of temperature and variance. When the protective circuit is not to be used, do not open the LVS pin (output OFF when this is opened) and apply the voltage on an inoperative level.





#### 8. RES circuit

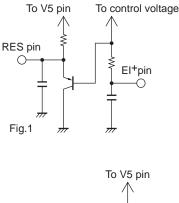
Apply initial reset with the RES pin to ensure stable operation at power ON. Initial reset includes the following operations :

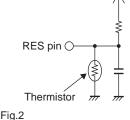
- All drive outputs OFF
- EI+ pin voltage at "L"
- FV pin voltage at "L"

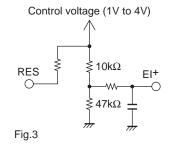
Normally, connect a resistor and capacitor between RES and V5 pins and between these pins and GND respectively and set the reset time. Use a  $2.7k\Omega$  or more resistor. Set so that the time constant becomes  $R \times C \ge 1m (0.1 \mu F)$  or more if this is 10k $\Omega$ ). If the charge of a capacitor connected to EI<sup>+</sup> or FV pin must be completely discharged, set the reset time by taking into account the discharge time of these pins. It is also recommended to set the reset time longer than the time necessary for stabilization of the VB voltage at power ON.

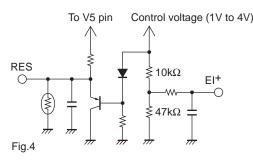
In addition to initial reset, reset may be applied when the control voltage is low as shown in Fig. 1 in the right. In this case, all drive outputs can be turned OFF when the control voltage becomes about  $0.67V(1.27V - V_{BE})$ . The reset cancellation voltage is about 0.9V (0.67V+0.23V). If only the control voltage is 0% duty (1.2V or less), the motor is braked when driven in the reverse direction. This is an effective application when braking is not necessary during reverse drive. If the control voltage cannot be decreased to 1V or less, application as shown in Fig. 3 may be used.

Heat detection with thermistor may also be considered to prevent thermal breakdown of output FET. Connect as shown in Fig. 2 in the right and adjust the external resistance, and the protective operation can be done. Fig. 4 shows a combination of this application with thermistor and an application shown in Fig. 3.









9. RC and FV circuits 1.691. How the pulse width ("H" time) generated in the FV pin for both edges of HP signal (Hall three-phase composite signal). Connect a resistor and capacitor between RS and VE pins and between this pin and GND respectively and set the pulse width. The pulse width TRC can be approximated by the following equation.

TRC (S)  $\approx 1.1 \times R \times C$ 

Connect the smoothing circuit comprising a resistor and capacitor, as shown in the right, to the FV pin. Select the  $25k\Omega$  or more resistor. The capacitor must have the capacitance ensuring sufficient smoothing of FV voltage when the motor rotation speed is low. Assume that the HP signal frequency at the maximum motor speed is fHP (Hz). Set so that the following equation is established :

TRC (S)  $\leq 1 \div (2 \times \text{fHP})$ 

In this case, the FV voltage changes from 0 to about 5V according to the motor speed. The FV voltage can be used as a signal for speed meter indication of analog or level meter IC or speed return.

If FV output is not to be used, connect the RC pin to GND and keep the FV pin open.

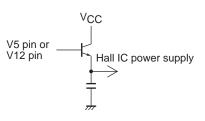
#### 10. Power stabilization

This IC is of a switching drive type, causing a state in which the power line is readily displaced. It is therefore necessary to connect the capacitor with sufficient capacity between the V<sub>CC</sub> pin and GND for stabilization.

When a diode is to be inserted into the power line to prevent breakdown due to reverse connection of power supply, the power line tends to be displaced readily. It is therefore necessary to select the larger capacity.

#### 11. Stabilizing the regulator output voltage

Connect the capacitor of 0.1µF or more between V5 pin (5V : control circuit power supply) or V12 pin (12V : lower drive output circuit power supply) and GND. Wire the capacitor GND as near to IC GND pin as possible. Each output can output the current of 30mA or less to the outside of IC. Due care must be taken however because IC heat generation increases. If this is used in the Hall IC power supply and presents a problem of heat generation, connect Tr as shown in the right so that Tr receives heat generation.



12. Lock protection circuit

The lock protection circuit is incorporated to protect IC and motor when the motor is locked. When the Hall input signal is not changed over for a certain period while the motor is being driven, the output on one side (UL, VL, WL) is turned OFF. The time is set with the capacitor capacitance connected to the CSD pin.

Set time (s)  $\approx 30 \times C (\mu F)$ 

Connection of the 0.01µF capacitor ensures the protection period of about 0.3 seconds (the drive is turned OFF when one cycle of Hall input signal exceeds this set time). Be sure to set the time with sufficient allowance, so that the protection circuit is not activated at normal motor startup. For the capacitor, use 4700pF or more. To cancel the lock protection state, take any one of following steps :

- Resetting.
- Maintaining the output duty 0% state by TOC input for the period of tCSD  $\times$  2,
- Re-applying the power.

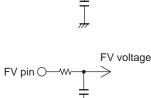
#### 13. Forward/backward operation

For forward/backward changeover during running, the measure is taken to prevent through current at the output (through current caused by the output Tr OFF delay time at a time of changeover). However, changeover during running causes the current exceeding the current limit to flow through the output Tr due to the motor coil resistance and motor counter electro-motive force. It is therefore necessary either to select the external output Tr that does not suffer breakage by this current or to design changeover with the motor speed reduced to a certain degree.

#### 14. FAIL Hall input

The output becomes "L" in following states with the open collector output :

- At abnormal Hall input
- When the low-voltage protection circuit is activated
- When the lock protection circuit is activated
- When the overheat protection circuit is activated

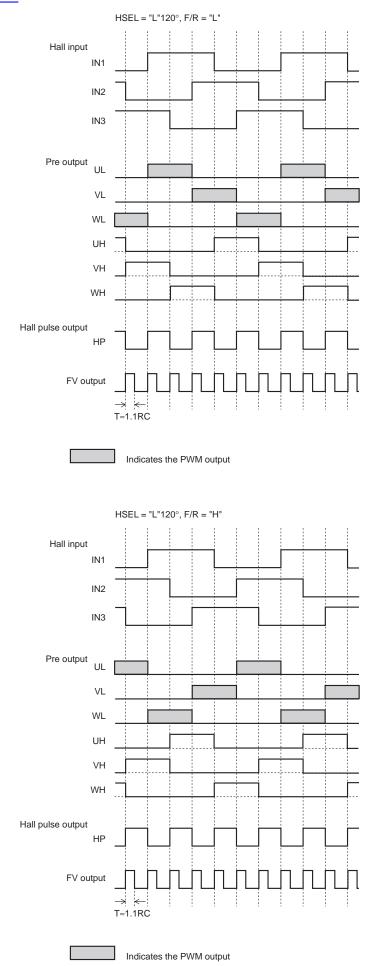


RC pin C

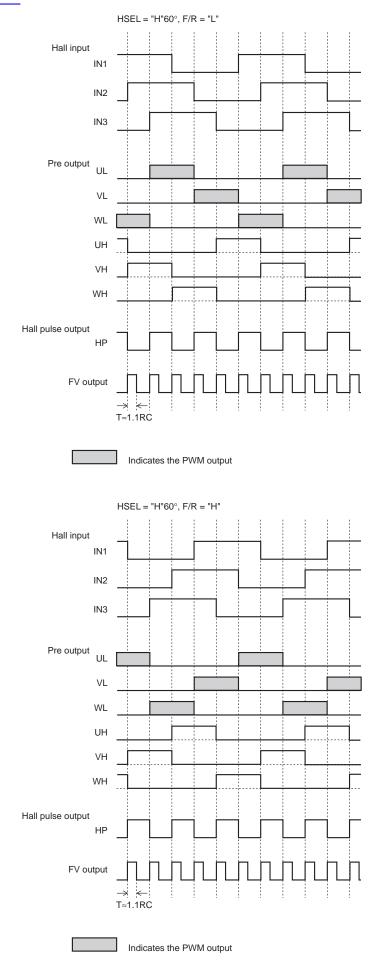
To V5 pin

- 15. HSEL 当19 【B11691】(井京商 中的名字 difference (120<sup>-</sup> and 60<sup>°</sup>) can be changed over for the three-phase Hall input.
  - HSEL = "L" 120°
  - HSEL = "H" 60°

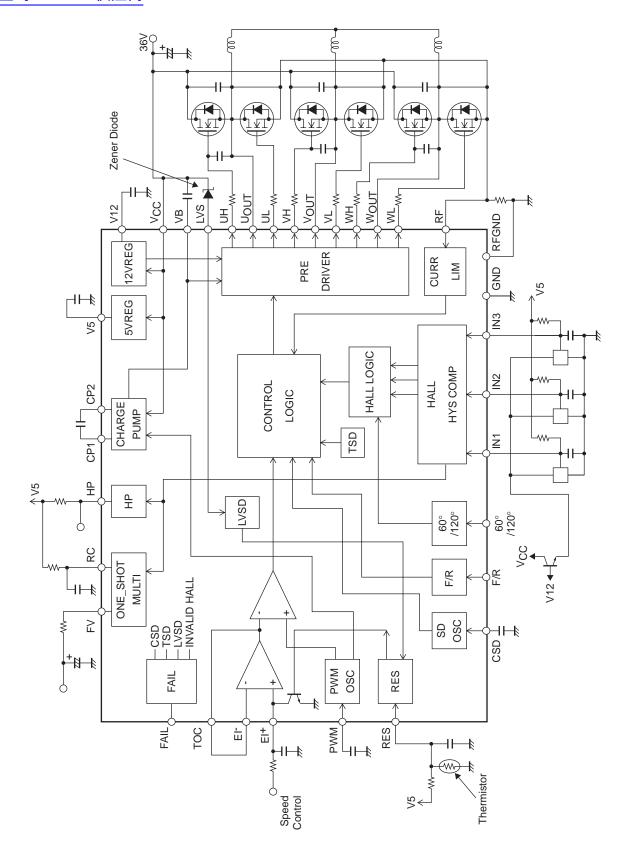
#### Hall input \_ each output timing chart (For three-phase Hall input phase difference of 120°) 查询上B11691 供应商



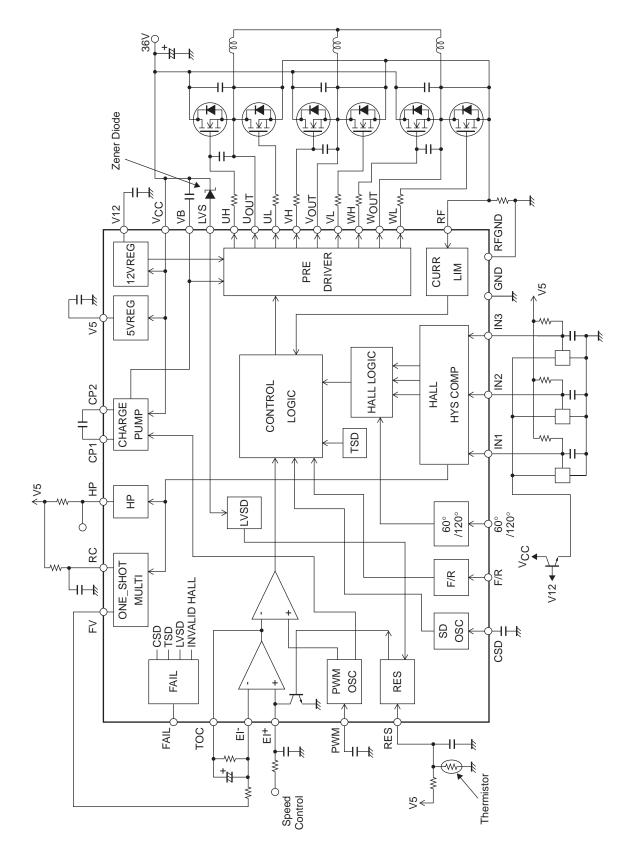
#### Hall input \_ each output timing chart (For three-phase Hall input phase difference of 60°) 查询上B11691 供应商



Sample Application Circuit



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