National Semiconductor

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T-45-07

100181

100181
4-Bit Binary/BCD Arithmetic Logic Unit

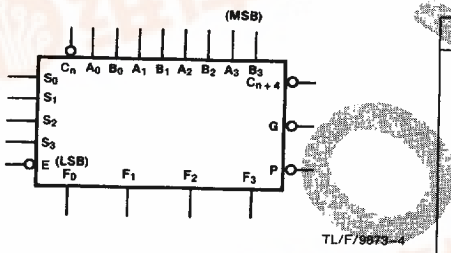
General Description

The 100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input LOW makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F_n outputs and to the ripple Carry output, $\overline{C}_{n+4}$. Group Carry Lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the Carry input $\overline{C}_n$. The $\overline{P}$ output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in a plus mode, or when their difference is greater than zero in a minus mode. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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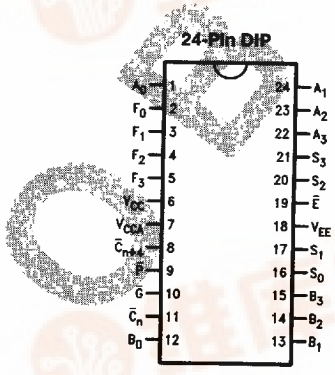
Pin Names	Description
A_0–A_3	Word A Operand Inputs
B_0–B_3	Word B Operand Inputs
$\overline{C}_n$	Carry Input (Active LOW)
S_0–S_3	Function Select Inputs
$\overline{E}$	Latch Enable Input (Active LOW)
$\overline{P}$	Carry Lookahead Propagate Output (Active LOW)
$\overline{G}$	Carry Lookahead Generate Output (Active LOW)
$\overline{C}_{n+4}$	Carry Output
F_0–F_3	Function Outputs

Connection Diagrams

24-Pin DIP



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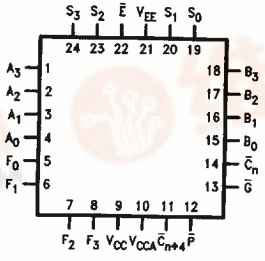
24-Pin Quad Cerpak



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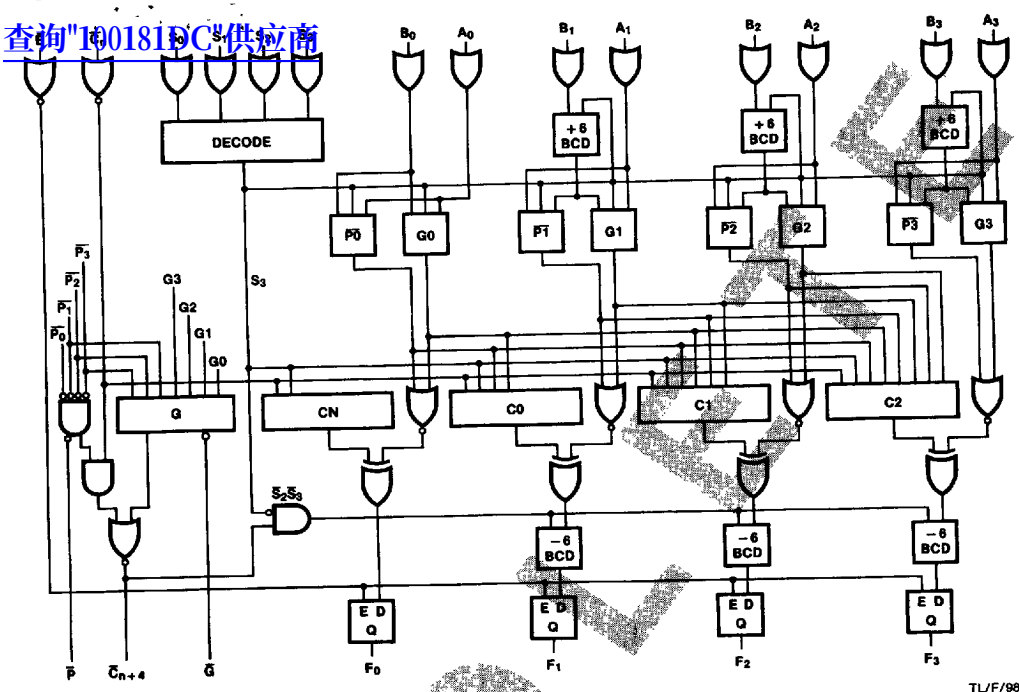
Logic Diagram



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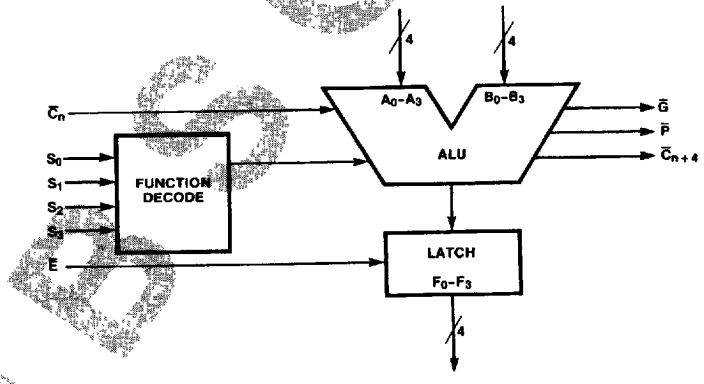
Block Diagram



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Functional Description

There are two modes of operation: Arithmetic and Logic. The S_3 input controls these two modes:

S_3 = LOW for Arithmetic mode

S_3 = HIGH for Logic mode

The arithmetic mode includes decimal and binary arithmetic operations. S_2 is the control input: with S_3 = LOW,

S_2 = LOW for Decimal Arithmetic (BCD)

S_2 = HIGH for Binary Arithmetic

DECIMAL ARITHMETIC OPERATION

Addition

$F = A$ plus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically performs the "+6" and "−6" logic correction internally.

Subtraction

$F = A$ minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the nines complement of B and adds "+6". A "−6" adjustment is made if the subtraction algorithm calls for it. If there is a carry out, the result is a positive number. With no carry out, the result is a negative number expressed in its nines complement form. Therefore, to perform a subtraction with results in the tens complement form, an initial carry should be forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(tens complement of B) = (nines complement of B) + 1

$F = B$ minus A plus C_n. Operation is similar to and results are the same as $F = A$ minus B plus C_n.

BINARY ARITHMETIC OPERATION

Addition

$F = A$ minus B plus C_n. Arguments A and B are directly applied to the inputs.

Subtraction

$F = A$ minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the ones complement of B (by inverting B internally). If there is a carry out the result is a positive number. With no carry out, the result is a negative number expressed in its ones complement form. Therefore, to perform a subtraction with results in the twos complement form, an initial carry should forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(twos complement of B) = (ones complement of B) + 1

$F = B$ minus A plus C_n. Operation is similar and results are the same as $F = A$ minus B plus C_n.

Function Table

S_3	S_2	S_1	S_0	F_n Function	G_n (n = 0 to 3)	P_n (n = 0 to 3)	Outputs		
					Internal Signals		$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	L	$F_n = A$ plus B plus C_n (BCD)	$A_n\overline{D}_n$	$A_n + D_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	H	$F_n = A$ minus B plus C_n (BCD)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	L	$F_n = B$ minus A plus C_n (BCD)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	H	$F_n = 0$ minus B plus C_n (BCD)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
L	H	L	L	$F_n = A$ plus B plus C_n (Binary)	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	L	H	$F_n = A$ minus B plus C_n (Binary)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	L	$F_n = B$ minus A plus C_n (Binary)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	H	$F_n = 0$ minus B plus C_n (Binary)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	L	L	L	$F_n = A_nB_n + \overline{A}_n\overline{B}_n$	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	L	H	$F_n = A_n\overline{B}_n + \overline{A}_nB_n$	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	H	L	$F_n = A_n + B_n$	A_n	$\overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}_x$	$\overline{P}$
H	L	H	H	$F_n = A_n$	A_n	H	$\overline{C}_{n+4}$	$\overline{G}$	L
H	H	L	L	$F_n = \overline{B}_n$	L	B_n	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	L	H	$F_n = B_n$	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	L	$F_n = A_nB_n$	L	$\overline{A}_n + \overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	H	$F_n =$ LOW	L	H	$\overline{C}_n$	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

$$\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$$

$$\overline{G} = \overline{G}_3 + P_3\overline{G}_2 + P_3P_2\overline{G}_1 + P_3P_2P_1\overline{G}_0$$

$$\overline{C}_{n+4} = \overline{G} \bullet (\overline{P} + \overline{C}_n)$$

Arithmetic Operations

$$F_n = \overline{G_n + \overline{P}_n \oplus C_i} \quad i = 0 \text{ to } 3$$

Logic Operations

$$F_n = G_n + \overline{P}_n$$

Internal Equations for Carry Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$

$$C_1 = G_0 + P_0C_n + S_3$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$$

Internal Equations for +6 Logic

$$D_0 = B_0$$

$$D_1 = \overline{B}_1$$

$$D_2 = B_1B_2 + \overline{B}_1\overline{B}_2$$

$$D_3 = B_1 + B_2 + B_3$$

$$\overline{G}_x = \overline{G_3P_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If military/aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_n, $\overline{E}$ All Others			350 250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−300	−210	−130	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.90	2.10	6.80	2.30	7.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.70	1.40	4.40	1.40	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.50	2.00	6.50	2.10	6.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	5.10	1.60	5.20	1.60	5.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	3.00	1.40	3.00	1.40	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.80	1.50	8.60	1.50	9.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.40	2.00	5.90	2.00	6.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	10.10	2.80	8.50	2.90	8.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.40	0.90	3.60	1.10	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.70	0.45	2.60	0.45	2.70	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	7.60 8.70 4.80		7.60 8.50 5.00		8.10 9.60 5.30		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	0.10 0.60 0.60		0.10 0.60 0.60		0.10 0.60 0.60		ns	
$t_{pw(L)}$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

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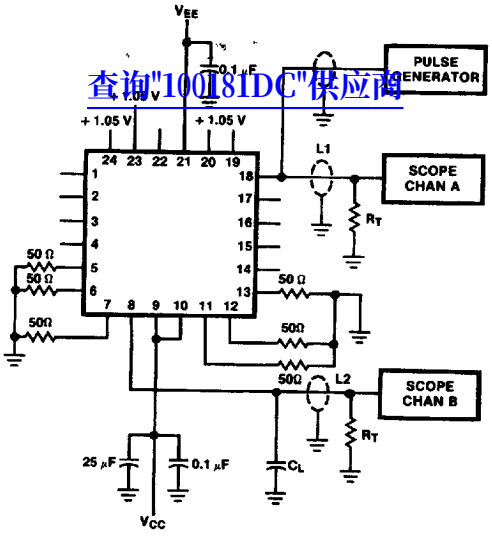
Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.70	2.10	6.60	2.30	7.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.50	1.40	4.20	1.40	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.30	2.00	6.30	2.10	6.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	4.90	1.60	5.00	1.60	5.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	2.80	1.40	2.80	1.40	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.60	1.50	8.40	1.50	8.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.20	2.00	5.70	2.00	6.30	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	9.90	2.80	8.30	2.90	8.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.20	0.90	3.40	1.10	3.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.60	0.45	2.50	0.45	2.60	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	7.50 8.60 4.70		7.50 8.40 4.90		8.00 9.50 5.20		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	0 0.50 0.50		0 0.50 0.50		0 0.50 0.50		ns	
t_{pw}(L)	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

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FIGURE 1. AC Test Circuit

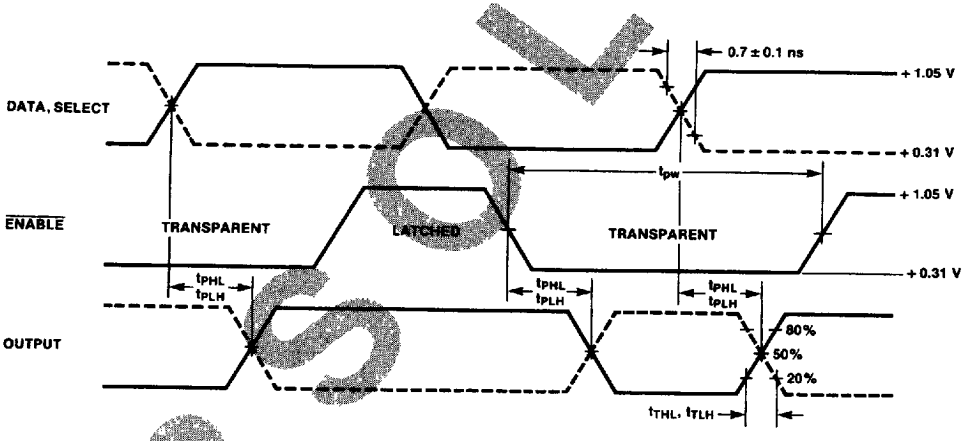

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FIGURE 2. Enable Timing

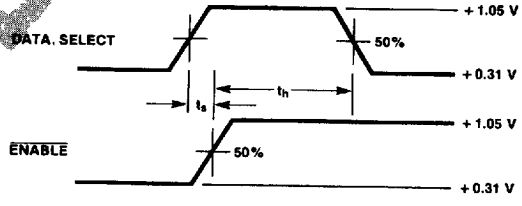

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FIGURE 3. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.