REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Table I, page 7; correct $\overline{SCLR}$ minimum limit. Change code ident no. to 67268. Page 4, V_{OH} and V_{OL} Editorial corrections for V_{IN} Page 11, Fig 3; Correct CCO output. Editorial changes	15 OCT 1987	R P Evans

CURRENT CAGE CODE 67268

REV																										
PAGE																										
REV STATUS OF PAGES	REV	A	A		A			A				A			A	A	A									
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17								

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
1 April 1987

AMSC N/A

PREPARED BY: Monica Grose

CHECKED BY: D A DiCenzo

APPROVED BY: M A Frank

SIZE: A

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REV: A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, BIPOLAR SYNCHRONOUS FOUR-BIT BINARY UP-DOWN COUNTER, MONOLITHIC SILICON

DWG NO. 5962-87544

PAGE 1 OF 17

5962-E606

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87544	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	25LS2569	Synchronous four-bit binary up-down counter with three state outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead 1/4" x 1 1/16"), dual-in-line package
S	F-9 (20-lead 1/4" x 1/2"), flat package
2	C-2 (20-terminal .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	0.7 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	30°C/W
Case S	25°C/W
Case 2	20°C/W
Junction temperature (T_J)	+150°C
DC input current	-30 mA to +5.0 mA
DC output current into output	30 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = +4.5 V V_{IN} = 0.7 V or 2.0 V	Y outputs I_{OH} = -1.0 mA	1,2,3	2.4		V
			I_{OH} = -440 µA CCO, $\overline{RCO}$ outputs	1,2,3	2.5		V
Low level output voltage	V_{OL}	V_{CC} = +4.5 V V_{IN} = 0.7 V or 2.0 V	I_{OL} = 4.0 mA	1,2,3		0.4	V
			I_{OL} = 8.0 mA	1,2,3		0.45	V
Input clamp voltage	V_{IC}	I_{IN} = -18 mA V_{CC} = 4.5 V		1,2,3		-1.5	V
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.7 V		1,2,3		20	µA
	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 7.0 V		1,2,3		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.4 V	$\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{LOAD}$	1,2,3		-300	µA
			A, B, C, D, CP, $\overline{CEP}$	1,2,3		-400	µA
			$\overline{CET}$, $\overline{SCLR}$	1,2,3		-650	µA
Off-state output current (high impedance)	I_{OZ}	V_{CC} = 5.5 V	V_{OUT} = 0.4 V	1,2,3		-20	µA
			V_{OUT} = 2.4 V	1,2,3		20	µA
Output short circuit current	I_{OS}	V_{CC} = 5.5 V V_{OUT} = 0.0 V	1/	1,2,3	-15	-85	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V $\overline{OE}$ = High	All inputs = GND	1,2,3		43	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Functional testing		See 4.3.1c		7			
Propagation delay time clock to any Q $\overline{Load}$ = low	t_{PLH1}	R_{L1} = 5 kΩ R_{L2} = 2 kΩ (figure 4)	C_L = 50 pF 2/	9,10,11		24	ns
			C_L = 15 pF 3/	9		18	
	t_{PHL1}		C_L = 50 pF 2/	9,10,11		35	ns
			C_L = 15 pF 3/	9		21	
Propagation delay time clock to any Q $\overline{Load}$ = high	t_{PLH2}		C_L = 50 pF 2/	9,10,11		24	ns
			C_L = 15 pF 3/	9		18	
	t_{PHL2}		C_L = 50 pF 2/	9,10,11		35	ns
			C_L = 15 pF 3/	9		21	
Propagation delay time $\overline{CET}$ to $\overline{RCO}$	t_{PLH3}	R_L = 2 kΩ (figure 4)	C_L = 50 pF 2/	9,10,11		19	ns
			C_L = 15 pF 3/	9		16	
	t_{PHL3}		C_L = 50 pF 2/	9,10,11		21	ns
			C_L = 15 pF 3/	9		14	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time U/D to $\overline{RCO}$	t_{PLH4}	R_L = 2 kΩ (figure 4)	C_L = 50 pF 2/	9,10,11		28	ns
			C_L = 15 pF 3/	9		23	
	t_{PHL4}		C_L = 50 pF 2/	9,10,11		30	ns
			C_L = 15 pF 3/	9		20	
Propagation delay time clock to $\overline{RCO}$	t_{PLH5}		C_L = 50 pF 2/	9,10,11		40	ns
			C_L = 15 pF 3/	9		35	
	t_{PHL5}		C_L = 50 pF 2/	9,10,11		39	ns
			C_L = 15 pF 3/	9		26	
Propagation delay time clock to CCO	t_{PLH6}		C_L = 50 pF 2/	9,10,11		18	ns
			C_L = 15 pF 3/	9		15	
	t_{PHL6}		C_L = 50 pF 2/	9,10,11		27	ns
			C_L = 15 pF 3/	9		15	
Propagation delay time $\overline{CET}$ or $\overline{CEP}$ to CCO	t_{PLH7}		C_L = 50 pF 2/	9,10,11		17	ns
			C_L = 15 pF 3/	9		15	
	t_{PHL7}		C_L = 50 pF 2/	9,10,11		45	ns
			C_L = 15 pF 3/	9		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time $\overline{ACLR}$ to any Q	t_{PLH8}	$R_{L1} = 5\ k\Omega$ $R_{L2} = 2\ k\Omega$ (figure 4)	$C_L = 50\ pF$ 2/	9,10,11		N/A	ns
			$C_L = 15\ pF$ 3/	9		N/A	
	t_{PHL8}		$C_L = 50\ pF$ 2/	9,10,11		45	ns
			$C_L = 15\ pF$ 3/	9		26	
Setup time A, B, C, D	t_{s1}	2/		9,10,11	30		ns
		3/		9	22		
Setup time $\overline{SCLR}$	t_{s2}	2/		9,10,11	35		ns
		3/		9	20		
Setup time $\overline{LOAD}$	t_{s3}	2/		9,10,11	45		ns
		3/		9	30		
Setup time U/$\overline{D}$	t_{s4}	2/		9,10,11	45		ns
		3/		9	30		
Setup time $\overline{CET}$, $\overline{CEP}$	t_{s5}	2/		9,10,11	47		ns
		3/		9	32		
Setup time $\overline{SCLR}$ recovery time (inactive to clock)	t_{s6}	2/		9,10,11	50		ns
		3/		9	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

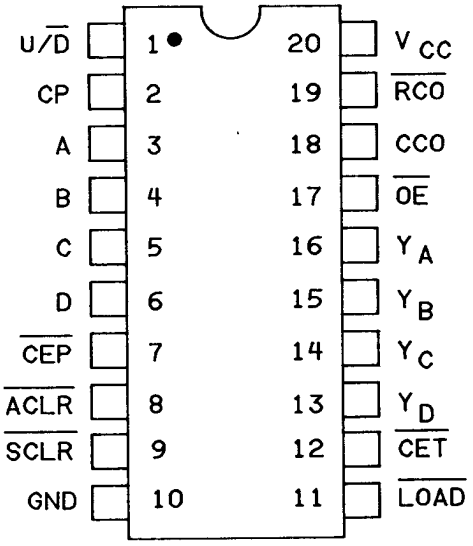
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ Unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Data hold	t_H	2/		9,10,11	5		ns
		3/		9	0		
Clock pulse width	t_{PW}	2/		9,10,11	37	$\frac{1}{37}$ = 27 MHz	ns
		3/		9	25		
Enable time $\overline{OE}$ to any Q	t_{PZH}	R_{L1} = 5 kΩ R_{L2} = 2 kΩ (figure 4)	C_L = 50 pF 2/	9,10,11		20	ns
			C_L = 15 pF 3/	9		11	
Enable time $\overline{OE}$ to any clock	t_{PZL}		C_L = 50 pF 2/	9,10,11		34	ns
			C_L = 15 pF 3/	9		19	
Disable time $\overline{OE}$ to any Q	t_{PHZ}	C_L = 5 pF R_{L1} = 5 kΩ R_{L2} = 2 kΩ	2/	9,10,11		22	ns
			3/	9		18	
	t_{PLZ}		2/	9,10,11		36	ns
			3/	9		24	

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed one second.

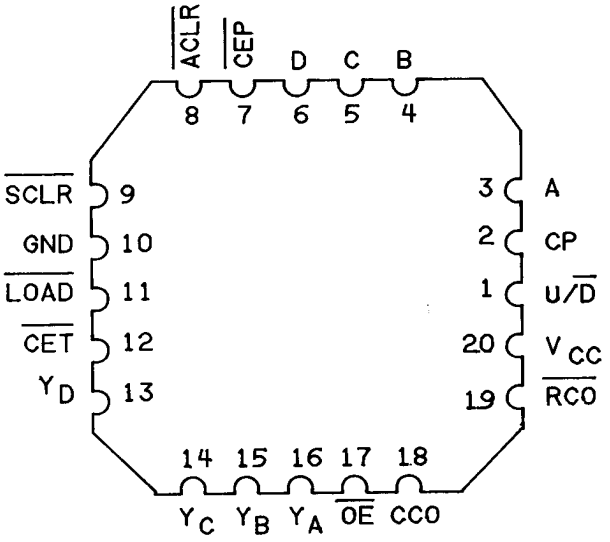
2/ Supply voltage = +4.5 V to +5.5 V, operating temperature = -55°C to +125°C.

3/ Supply voltage = +5.0 V, operating temperature = +25°C.

CASES R AND S



CASE 2



(TOP VIEW)

FIGURE 1. Terminal connections.

Mode	Inputs												Outputs					
	Load	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Async clear	Sync clear	$\overline{OE}$ 1/	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	Clock carry
Clear (async)	X X	X X	X X	1 0	0 0	X X	0 0	X X	X X	X X	X X	X X	0 0	0 0	0 0	0 0	1 0	1 2/
Clear (sync)	X X	X X	X X	1 0	1 1	0 0	0 0	X X	X X	X X	X X	. .	0 0	0 0	0 0	0 0	1 0	1 2/
Load	0 0 0	X X X	1 0 0	X 0 1	1 1 1	1 1 1	0 0 0	X 0 1	X 0 1	X 0 1	X 0 1	. . .	0 1	$Q_n=D_n$ 0 1	0 1	0 1	1 0 0	1 2/ 2/
Count up	1	0	0	1	1	1	0	X	X	X	X	.	Q_n +1				3/	4/
Count down	1	0	0	1	1	1	0	X	X	X	X	.	Q_n -1				5/	4/
Inhibit	1 1 1	0 1 1	1 0 1	X X X	1 1 1	1 1 1	0 0 0	X X X	X X X	X X X	X X X	↑ ↑ ↑	NC NC NC				NC NC NC	1 1 1
Output disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	NC	NC

↑ = Clock low-to-high transition
X = Don't care
D_n = D_0 through D_3 input level prior to clock transition
Qn + 1 = Next higher count in binary sequence
Qn - 1 = Next lower count in binary sequence
NC = No change

NOTES:
1. Register performs at correct logic for any state of $\overline{OE}$, but $\overline{OE}$ = 0 to view outputs.
2. Follows clock if $\overline{CET}$ = $\overline{CEP}$ = 0, otherwise remains high.
3. Low for one full clock cycle when maximum count is reached otherwise remains high.
4. Follows clock when RC = 0.
5. Low for one full clock cycle when minimum count is reached otherwise remains high.

FIGURE 2. Truth table.

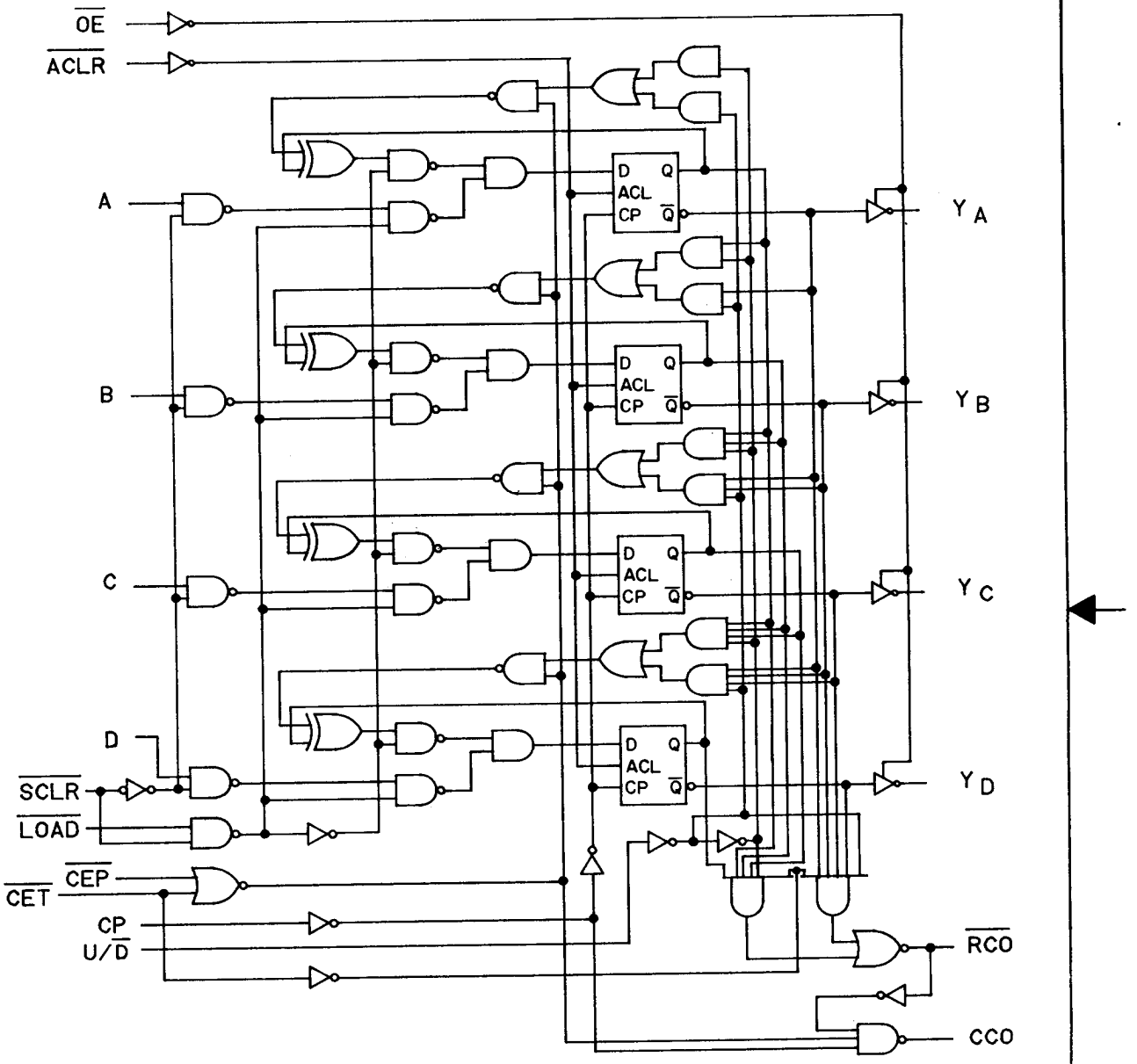
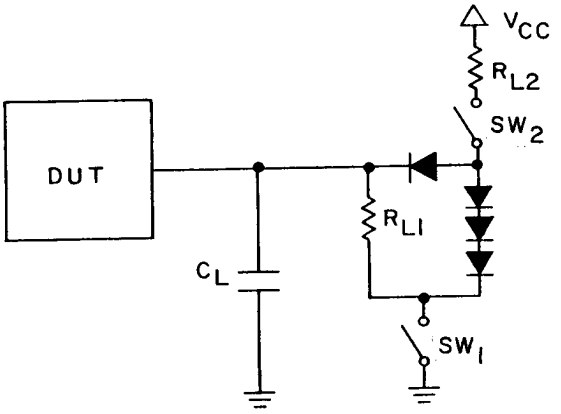
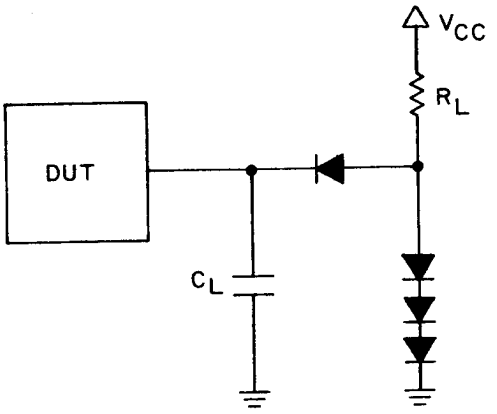


FIGURE 3. Logic diagram.

AC Bench load test circuit
for three-state outputs



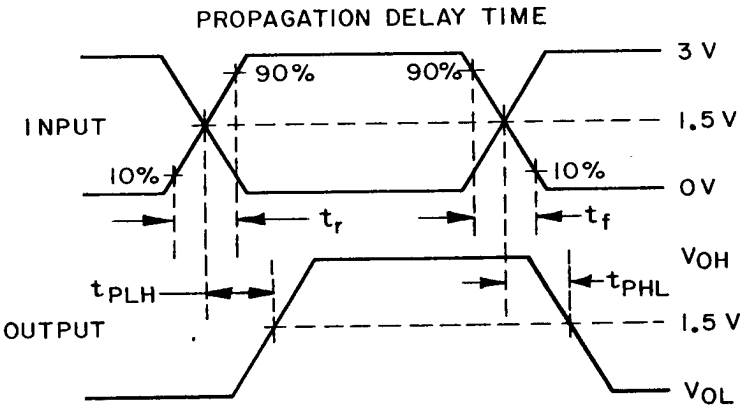
AC Bench load test circuit
for non three-state outputs



Switch Matrix

Parameter	SW_1	SW_2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{ZL}	Open	Closed
t_{ZH}	Closed	Open
t_{LZ}	Closed	Closed
t_{HZ}	Closed	Closed

FIGURE 4. Switching waveforms and test circuits.



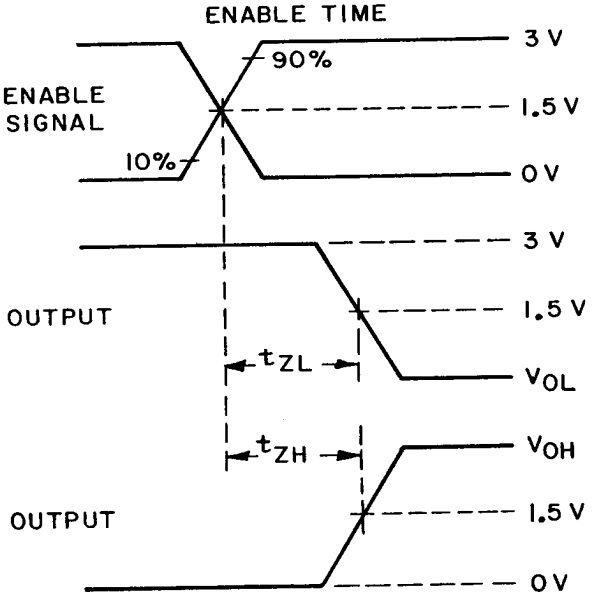
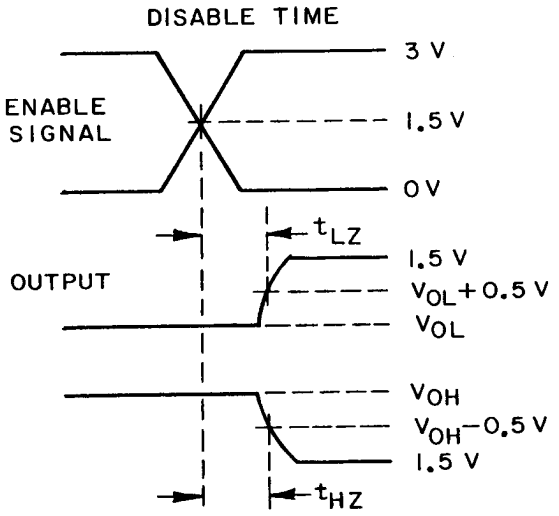


FIGURE 4. Switching waveforms and test circuits - Continued.



NOTES:
1. Pulse generator for all pulses:
2. Rate < 1.0 MHz; Z_O = 50Ω; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.
3. C_L Tncludes probe and jig capacitance.
4. All diodes are 1N916 or 1N3064.

FIGURE 4. Switching waveforms and test circuits - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8754401RX	34335	AM25LS2569/BRA
5962-8754401SX	34335	AM25LS2569/BSA
5962-87544012X	34335	AM25LS2569/B2C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088