

# Trige的Line Beceive供应商

### ELECTRICALLY TESTED PER: 5962-8750201

The 10H516 is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 125 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated

2

MECL 10K-Compatible

	PI		ENTS	
FUNCTION	DIL	FLATS	LCC	BURN-IN
				(CONDITION C)
VCC1	1	5	2	GND
AOUT	2	6	3	51 Ω to VTT
AOUT	з	7	4	51 $\Omega$ to V <sub>TT</sub>
AIN	4	8	5	GND
AIN	5	9	7	VBB
BOUT	6	10	8	51 $\Omega$ to V <sub>TT</sub>
BOUT	7	11	9	51 $\Omega$ to V <sub>TT</sub>
VEE	8	12	10	VEE
BIN	9	13	12	GND
BIN	10	14	13	VBB
VBB	11	15	14	VBB
CIN	12	16	15	GND
CIN	13	1	17	VBB
COUT	14	2	18	51 Ω to VTT
COUT	15	3	19	51 $\Omega$ to V <sub>TT</sub>
VCC2	16	4	20	GND

#### **BURN - IN CONDITIONS:**

Powered

 $V_{TT} = -2.0 V MAX/ - 2.2 V MIN$  $V_{EE} = -5.7 V MAX/ - 5.2 V MIN$ 

 $V_{BB}^{--}$  = All pins designated for V<sub>BB</sub> must be tied together, no external voltage applied.

# Military 10H516

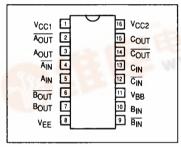


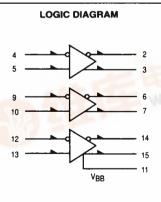
AVAILABLE AS

1) JAN: N/A 2) SMD: 5962-8750201 3) 883: 10H516/BXAJC X = CASE OUTLINE AS FOLLOWS:

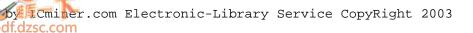
PACKAGE: CERDIP: E CERFLAT: F LCC: 2

The letter "M" appears before the slash on LCC.

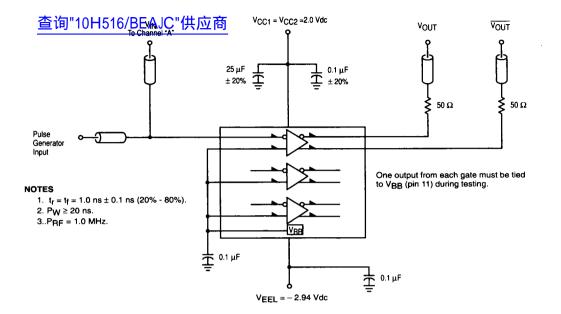




MOTOROLA MILITARY MECL DATA 2-52



## 10H516



#### NOTES

- 1. All input and output cables to the scope are equal lengths of 50  $\Omega$  coaxial cable. Wire length should be  $\leq$  0.250 inches (6.35 mm) from TP<sub>IN</sub> to input pin and TP<sub>OUT</sub> to output pin.
- 2. Outputs not under test should be connected to a 100  $\Omega$  resistor to ground.

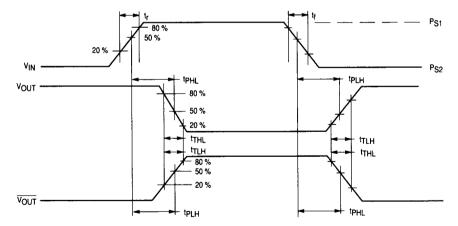


Figure 1. Switching Test Circuit and Waveforms

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	* ELECTRICAL CHARACTERISTICS	ACTER	ISTICS						Test				Test	Voltage	fest Voltage Values (Volts)	(olts)	10H	
Each ME	Each MECL 10H series o	circuit ha	s been d	lesigned	to meet	es circuit has been designed to meet the dc specifications	ecificatio	SU .	lempera		11 <u>/</u> [1	VIH2	VIL2	PS1	PS2	VEE1 V	VEE2 K	EEL VCB
shown in in a taet e	shown in the test table, after thermal equilibrium has been established. The circuit is in a test souk of or monitoring on a printipal discuit board and transverse sit flow creator	er thermé	al equilibri atod oircu	ium has b iit board s	been esta	blished.	he circui	tis	TA = 25°C	°C -0.78	78 -1.95	-1.11	-1.480	+1.11	+0.31	-5.46	4.94	2.94 -5.2
than 500	in a test soucce of mounted on a primed or court over a and mansverse an now greater than 500 linear form is maintained. On things are terminated through a 1000 resistor	ntained .		are termir	anu nans aatad thre	verse an	now grea	j j	TA = 125°C	5°C -0.65	65 -1.95	96.0- 3	-1.465	+1.24	+0.36	-5.46	-4.94	.94 -5.2
to -2.0 V.		וומוופת	Sindino		ומובח ווזוו	יישוומ וי	01001750	5	TA = -55°C	5°C -0.84	84 -1.95	5 -1.16	-1.510	+1.01	+0.28	-5.46	-4.94	2.94 -5.2
										<u>C"供</u>							C"供/	
Symbol	Parameter			Ë	Limits			Units			TES	T VOLTA	GE APP	LIED TC	B SNIG	ELOW	应ī	
	-		+ 25 °C	+ 12	+ 125 °C	- 55 °C	ပ္			Pino	uts refer	enced al	re for DI	L packa	ge, chec	k Pin Ass	ignment:	. 0
	Functional Parameters:	Subgroup 1	oup 1	Subgr	Subgroup 2	Subgr	Subgroup 3				>	CC = 0 V	, Outpu	t Load =	100 Ω t(	0 - 2.0 V		
		Min	Max	Min	Max	Min	Max		VIH1	VIL1	VIH2	VIL2		VEE 2	vcc	VBB	VCB	P. U. T.
ЧОЧ	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	>	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			æ		1, 16			2, 3, 6, 7, 14, 15
NOL	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	>	4 5, 9, 10, 12, 13, 14	4, 5, 9, 10, 12			80		1, 16			2, 3, 6, 7, 14, 15
Ион	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	>	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	80	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
VOL1	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	>	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	æ	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
VBB1	Reference Voltage**	-1.37	-1.25	-1.31	-1.15	-1.41	-1.27	>						80	1, 16			7
lee	Power Supply Current	-21		-23		23		٩w	4, 9, 12	5, 10, 13			8		1, 16			œ
Ŧ	Input Current High		140		235		235	Ϋ́́	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8		1, 16			4, 5, 9, 10, 12, 13
ICBO	Input Leakage Current	-1.0		-1.0		-1.5		μA	4, 5, 9, 10, 12,	4, 5, 9, 10, 12,				œ	1, 16	4, 5, 9, 10, 12, 12	4, 5, 9, 10, 12,	4, 5, 9, 10, 12, 12

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				Ø	UIES	CEN			*							<u> 5</u> 询"10	
<b>CTE</b>	* ELECTRICAL CHARACTERISTICS	SS	-		-	1		Test Temperature				Test Vo	Itage Va	Test Voltage Values (Volts)	olts)	)H5 <sup>,</sup>	
Ircuit	nas bee	Each MECL 10H series circuit has been designed to meet the dc specifications	ned to n	neet the	dc spec	ITICATION:			۷IH1	VIH1 VIL1 VIH2 VIL2 PS1	/IH2	VIL2		PS2 V	EE1 V	VEE1 VEE2 DEEL	EL VCB
	nrinted c	shown in the test table, alter the internal equilibrium has been established. The chorus in a test socket or monitoted on a printed circuit hoard and transverse air flow freater	ard and t	ransvers	se air flov	s un cun is N nreatei		TA = 25 °C	-0.78	-1.95 -	1.11	-1.11 -1.480 +1.11		+0.31 -	-2.46 -4	-4.94 23.94	94 -5.2
ainer	d. Outpu	that solves the maintained $\sim$ 0 the late terminated through a 100 $\Omega$ resistor	rminated	d through	2001 a r	2 resistor		TA = 125 °C	-0.65	1.95	0.96	-0.96 -1.465 +1.24		+0.36	-5.46 -4	-4.94	94 -5.2
	, + , , , , , , , , , , , , , , , , , ,							TA = -55 °C -0.84 -1.95 -1.16 -1.510 +1.01 +0.28	-0.84	-1.95	1.16	1.510	+1.01	-0.28	-5.46 -4	-4.94 -2.94	94 -5.2
																́Ӊ	
Parameter			Lin	Limits			Units			TEST V	OLTAG	E APPL	IED TO	TEST VOLTAGE APPLIED TO PINS BELOW	ROW	应	
	+ 25	+ 25 °C	+ 12	+ 125 °C	- 55	55 °C		Pin	iouts ref	ferencec	d are for	r DIL pa	ckage, c	check Pi	Pinouts referenced are for DIL package, check Pin Assignment		
Functional Parameters:	Subgr	Subgroup 9	Subgroup 10	oup 10	Subgroup 11	up 11				VCC = 2	2.0 V, O	utput Lo	oad = 1(	VCC = 2.0 V, Output Load = 100 $\Omega$ to GND	QND	-	
	Min	Мах	Min	Мах	Min	Мах		NIN	_	Vout		vcc Vcc		VEE1		P.U.T	
	0.4	1.35	0.4	1.5	0.4	1.25	us	12		15		1, 16		8		2, 3, 6, 7, 14, 15	14, 15
	0.4	1.35	0.4	1.5	0.4	1.25	SL	12		15		1, 16		æ		2, 3, 6, 7, 14, 15	14, 15
n Delay	0.4	4.1	0.4	1.6	0.4	1.3	SI	4		2		1, 16		æ		2, 3, 6, 7, 14, 15	14, 15
Delay	0.4	1.4	0.4	1.6	0.4	1.3	su	4		2		1, 16		æ		2, 3, 6, 7, 14, 15	14, 15

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