Triple Line Receiver

ELECTRICALLY TESTED PER:
5962-8750201

The 10H516 is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 125 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	GND
A_{IN}	5	9	7	V_{BB}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
$\overline{B_{IN}}$	9	13	12	GND
B_{IN}	10	14	13	V_{BB}
V_{BB}	11	15	14	V_{BB}
$\overline{C_{IN}}$	12	16	15	GND
C_{IN}	13	1	17	V_{BB}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

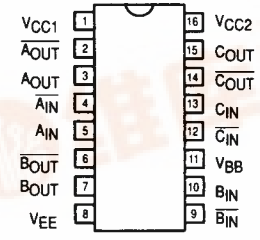
Military 10H516

AVAILABLE AS

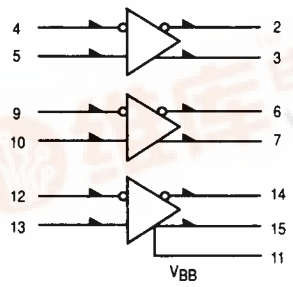
1) JAN: N/A
2) SMD: 5962-8750201
3) 883: 10H516/BXAJC
X = CASE OUTLINE AS FOLLOWS:

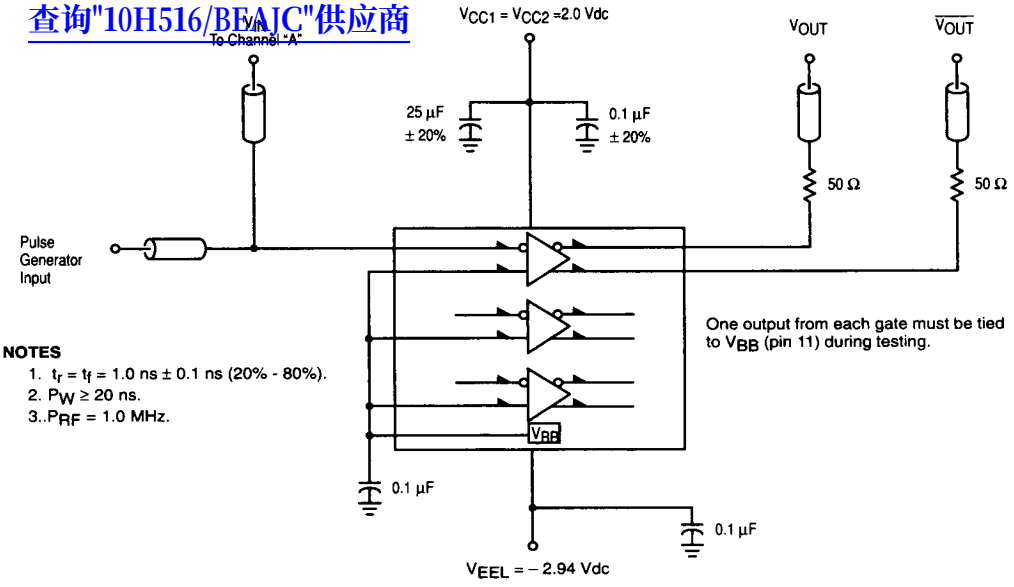
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% - 80%).
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

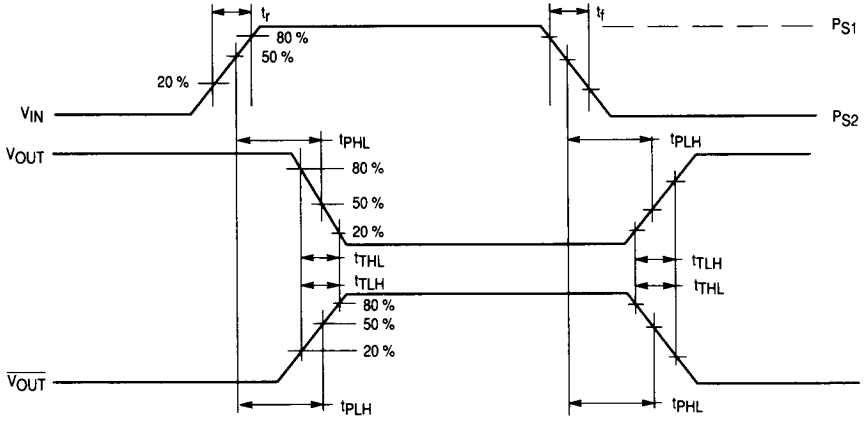


Figure 1. Switching Test Circuit and Waveforms

10H516
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 V.

Test Temperature	Test Voltage Values (Volts)									
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}	V_{CB}
T_A = 25°C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-5.2
T_A = 125°C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-5.2
T_A = -55°C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	V_{BB}	V_{CB}	P. U. T.
V_{OH}	High Output Voltage	−1.01	−0.78	−0.86	−0.65	−1.06	−0.84	V	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8		1, 16			2, 3, 6, 7, 14, 15
V_{OL}	Low Output Voltage	−1.95	−1.58	−1.95	−1.565	−1.95	−1.61	V	4, 5, 9, 10, 12, 13, 14	4, 5, 9, 10, 12			8		1, 16			2, 3, 6, 7, 14, 15
V_{OH1}	High Output Voltage	−1.01	−0.78	−0.86	−0.65	−1.06	−0.84	V	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	8	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
V_{OL1}	Low Output Voltage	−1.95	−1.58	−1.95	−1.565	−1.95	−1.61	V	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	8	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
V_{BB1}	Reference Voltage**	−1.37	−1.25	−1.31	−1.15	−1.41	−1.27	V						8	1, 16			11
I_{EE}	Power Supply Current	−21		−23		−23		mA	4, 9, 12	5, 10, 13			8		1, 16			8
I_{IH}	Input Current High		140		235		235	µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8		1, 16			4, 5, 9, 10, 12, 13
I_{CBO}	Input Leakage Current	−1.0		−1.0		−1.5		µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13				8	1, 16	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13

** For V_{BB1} connect pin 5, 10, 13 to pin 11.

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
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		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P.U.T
t_{TLH}	Rise Time	0.4	1.35	0.4	1.5	0.4	1.25	ns	12	15	1, 16	8	2, 3, 6, 7, 14, 15
t_{THL}	Fall Time	0.4	1.35	0.4	1.5	0.4	1.25	ns	12	15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL}	Propagation Delay	0.4	1.4	0.4	1.6	0.4	1.3	ns	4	2	1, 16	8	2, 3, 6, 7, 14, 15
t_{PLH}	Propagation Delay	0.4	1.4	0.4	1.6	0.4	1.3	ns	4	2	1, 16	8	2, 3, 6, 7, 14, 15