查询"BU2373FV"供应商

Structure Silicon monolithic Integrated circuit
Product VCO

Type **BU2373FV**

Feature VCO & Phase-Detector for PLL System
The VCO enables midpoint settings within the range of oscillation through the external resistance.
The rising edge trigger type of phase comparator is built in.
Power-down mode setting can be made independently with the VCO and the phase comparator.

○Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 ～ 7.0	V
Input Voltage	VIN	-0.5 ～ VDD+0.5	V
Storage Temperature range	Tstg	-30 ～ 125	℃
Power dissipation	PD	400 ※1	mW

※1 A measure value at mounting on 50×50×1.6mm glass epoxy substrate.
In the case of exceeding Ta=25℃, 4.0mW should be reduced per 1℃.
※ The radiation-resistance design is not carried out.
※ Operation is not guaranteed.

○Operating Conditions (Ta=-20～+75℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (TYP3.0V)	VDD	2.85	3.00	3.15	V
(TYP3.3V)		3.15	3.30	3.45	
(TYP5.0V)		4.75	5.00	5.25	
Input "H" Voltage	VIH	0.8VDD	-	VDD	V
Input "L" Voltage	VIL	0	-	0.2VDD	V
Output load	CL	0	-	15	pF

Application example
・ROHM cannot provide adequate confirmation of patents.
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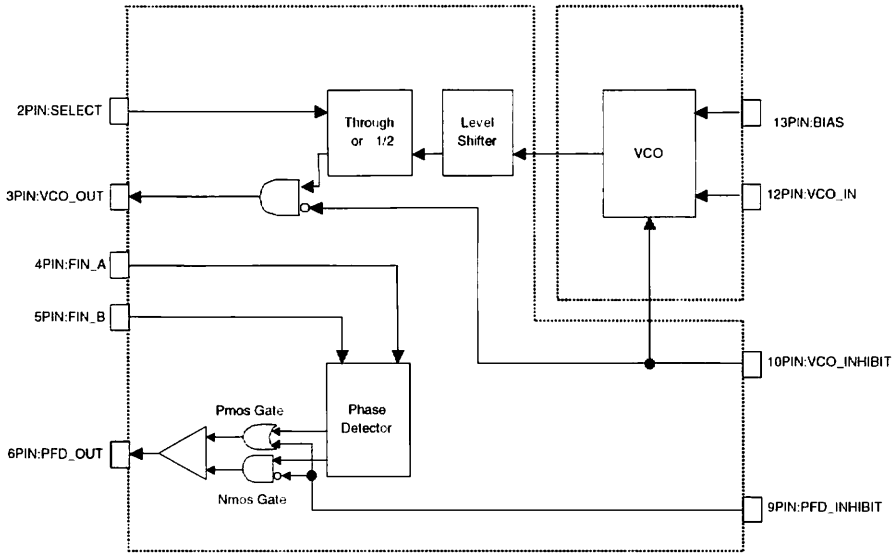
○Electrical Characteristics (VDD=3.3V,Ta=25℃,at No Load ,unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<VCO Section>						
Output H voltage	VOH	3.0	-	-	V	IOH=-2.0mA
Output L voltage	VOL	-	-	0.3	V	IOL=2.0mA
Input current (VCO_INHIBIT,SELECT)	IIH,IIL	-	-	±1	μA	
VCO_IN input impedance	Zi	-	10	-	MΩ	
Consumption current (while in standby mode)	IDD (INH)	-	-	1	μA	at VCO_IN=GND, VCO_INHIBIT=VDD PFD_INHIBIT=VDD
Consumption current (while in normal mode)	IDD (VCO)	-	15	-	mA	With 60 MHz output
Control voltage	VI (vco_in)	0.5	-	VDD-0.5	V	
Oscillation range	frange	37	-	60	MHz	VDD=3.0V
		37	-	65		VDD=3.3V
		43	-	100		VDD=5.0V
Bias resistor range	Rbias	1.6	-	2.2	KΩ	VDD=3.3V
Frequency sensitivity	β1	-	23	-	MHz/V	

○Electrical Characteristics (VDD=5.0V,Ta=25℃,at No Load ,unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<PFD Section>						
Output H voltage	VOH	4.5	-	-	V	IOH=-2.0mA
Output L voltage	VOL	-	-	0.5	V	IOL=2.0mA
Input current (PFD_INHIBIT,FINA,FINB)	IIH,IIL	-	-	±1	μA	
Consumption current (while in standby mode)	IDD (INH)	-	-	1	μA	at FIN_A&B=GND, VCO_INHIBIT=VDD PFD_INHIBIT=VDD
Consumption current (while in normal mode)	IDD (PFD)	-	1	-	mA	FIN_A&B=1MHz

○Block diagram



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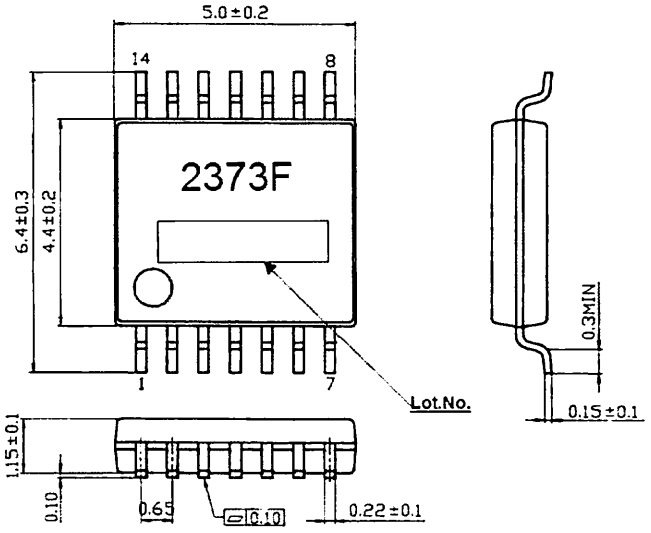
○Package outline, Appearance of Marker



○Pin function

PIN No.	PIN NAME	Function
1	LOGIC_VDD	Power supply for the internal Logic and the VCO output, which should be separated from power supply for the VCO_VDD (analog block).
2	SELECT	VCO output frequency dividing mode selection pin. H: Frequency dividing output, L: Through output
3	VCO_OUT	VCO output pin. If the VCO_INHIBIT is set to "H", the VCO_OUT will be fixed to L.
4	FIN_A	Reference frequency input pin
5	FIN_B	VCO block frequency dividing input pin, which inputs after the VCO output frequency is divided through the external counter.
6	PFD_OUT	Phase comparator output pin. If the PFD_INHIBIT is set to "H", the PFD_OUT will be set to Hi-Z output.
7	LOGIC_GND	GND for the internal Logic and the VCO output
8	TEST	Test mode pin, which is normally used with set to OPEN or fixed to L. Equipped with Pull-down resistor.
9	PFD_INIHIBIT	Phase comparator inhibit control pin. If the PFD_INHIBIT is set to "H", the PFD_OUT will be set to Hi-Z output.
10	VCO_INHIBIT	VCO inhibit control pin. If the VCO_INHIBIT is set to "H", the VCO_OUT will be fixed to L output.
11	VCO_GND	GND for VCO (Analog block GND)
12	VCO_IN	VCO control pin, to which loop filter output for the PLL system is connected due to frequency control on normal system.
13	BIAS	Bias current setting pin for the shift of VCO oscillation range. A resistor is connected to the VCO_VDD for the control of bias current.
14	VCO_VDD	VDD for VCO (power supply for analog block)

●Cautions on use (BU2373FV)

VCO_VDD,VCO_GND : Please take care this Power line. Because this line is most weak in digital noise. So this line must be separated from LOGIC_VDD,GND. And place bypass capacitor (0.01uF) for power pin as close to bu2373fv as possible.

LOGIC_VDD,LOGIC_GND : This line is noise source. So it should be separated from AVDD (AGND). And place bypass capacitor (0.01uF) for power pin as close to bu2373fv as possible. And this line should be connected VDD of external vco-out divide.

* It is recommended to use bypass capacitors of good high-frequency characteristics.
* It is recommended to apply power supply in the LOGIC_VDD and LOGIC_GND circuits for the SELECT. PFD_INHIBIT, and VCO_INHIBIT control pins.

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●Cautions on use(common)

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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As of 18th. April 2005