SINGLE 10-A OUTPUT, 4.75-V to 14-V INPUT, NON-ISOLATED, DIGITAL POWERTRAIN™ MODULE

Check for Samples: PTD08A210W

FEATURES

- **Single 10-A Output**
- **4.75-V to 14-V Input Voltage**
- **Programmable Wide-Output Voltage (0.7 V to 3.6 V)**
- **Efficiencies up to 96%**
- **Digital I/O**
  - **PWM signal**
  - **Fault Flag (FF)**
  - **Sychronous Rectifier Enable (SRE)**
- **Analog I/O**
  - **Temperature**
  - **Output currrent**
- **Safety Agency Approvals:**
  - **UL/IEC/CSA-C22.2 60950-1**
- **Operating Temperature: –40°C to 85°C**

APPLICATIONS

- **Digital Power Systems using UCD9XXX Digital Controllers**
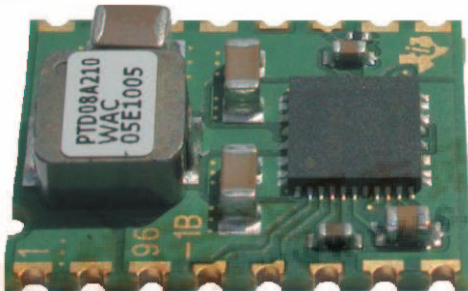
DESCRIPTION

The PTD08A210W is a high-performance single 10-A output, non-isolated digital PowerTrain module. This module is the power conversion section of a digital power system which incorporates TI's UCD7242 MOSFET/driver IC. The PTD08A210W must be used in conjunction with a digital power controller such as the UCD9240, UCD9220 or UCD9110 family. The PTD08A210W receives control signals from the digital controller and provides parametric and status information back to the digital controller. Together, PowerTrain modules and a digital power controller form a sophisticated, robust, and easily configured power management solution.

Operating from an input voltage range of 4.75 V to 14 V, the PTD08A210W provides step-down power conversion to a wide range of output voltages from, 0.7 V to 3.6 V. The wide input voltage range makes the PTD08A210W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V, 9.6-V or 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V or 12-V intermediate bus architectures.

The module incorporates output over-current and temperature monitoring which protects against most load faults. Output current and module temperature signals are provided for the digital controller to permit user defined over-current and over-temperature warning and fault scerarios.

The module uses single-sided, pin-less surface mount construction to provide a low profile and compact footprint. The package is lead (Pb) - free and RoHS compatible.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

POWERTRAIN is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Standard PTD08A210W Application
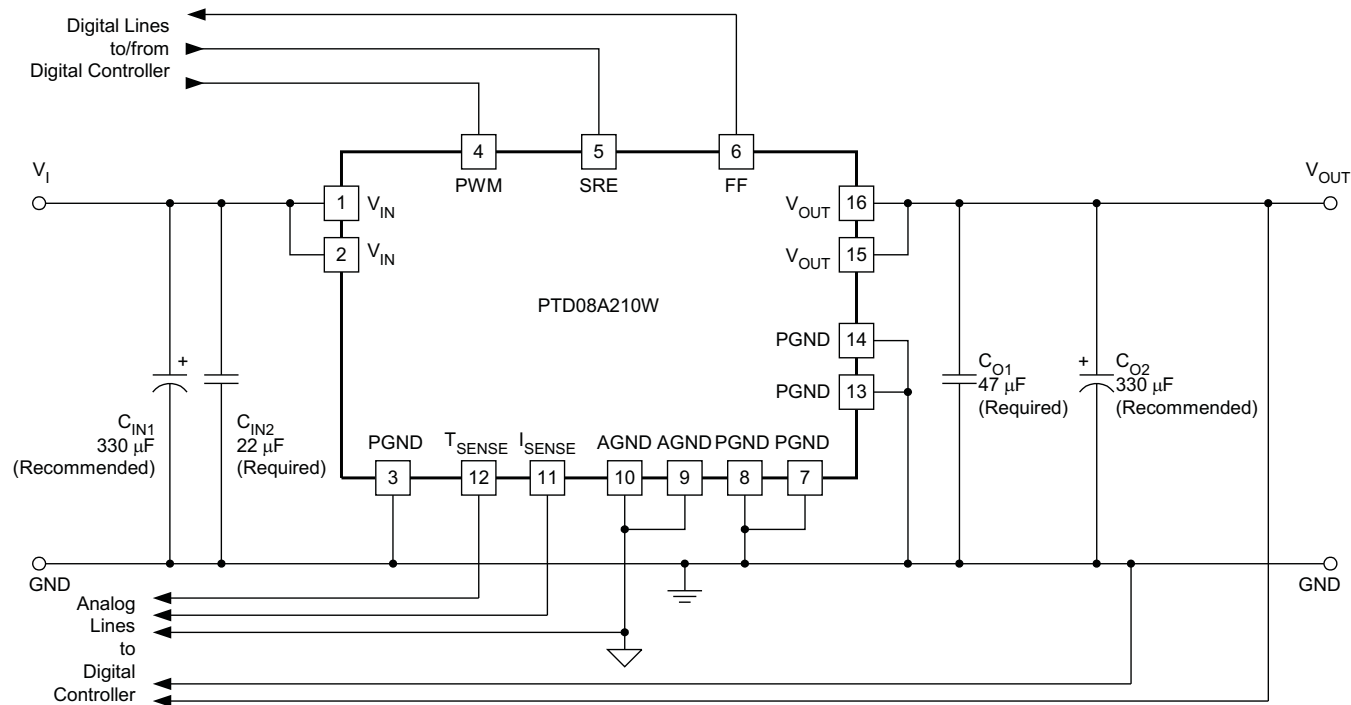
UDG-10063

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT
V_I	Input voltage		16	V
T_A	Operating temperature range	Over V_I range	−40 to 85	°C
T_{reflow}	Solder reflow temperature	Surface temperature of module body	260[1]	
T_{stg}	Storage temperature		−55 to 125	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	275	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	10	
	Weight		3.9	grams
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign	13.3	10^6 Hr
	Flammability	Meets UL94V-O		

(1)   During reflow do not elevate peak temperature of the module or internal components above the stated maximum.

PTD08A210W

ELECTRICAL CHARACTERISTICS

PTD08A210W

T_A= 25°C, F_{SW}= 750kHz, V_I= 12 V, V_O= 1.2 V, C_{IN1}= 330 µF, C_{IN2}= 22 µF ceramic, C_{O1}= 47 µF ceramic, C_{O2}= 330 µF, I_O= $I_{O(max)}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTD08A210W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection	0		10	A
V_I	Input voltage range	Over I_O range		4.75		14	V
V_{OADJ}	Output voltage adjust range	Over I_O range		0.7		3.6[1]	V
η	Efficiency	I_O = 10 A, fs = 750 kHz	V_O = 3.3 V		92.0%		
			V_O = 2.5 V		90.4%		
			V_O = 1.8 V		88.4%		
			V_O = 1.2 V		84.7%		
			V_O = 0.8 V		80.0%		
V_{OPP}	V_O Ripple (peak-to-peak)	20-MHz bandwidth			11		mV_{PP}
I_B	Bias current	PWM & SRE to AGND	Standby		6		mA
V_{IH}	High-level input voltage	SRE & PWM input levels		2.0		5.5	V
V_{IL}	Low-level input voltage					0.8	
	PWM input	Frequency range		500[1]		1000	kHz
		Pulse width limits		20			ns
	TEMP output	Range		-40		125	°C
		Accuracy, -40°C ≤ T_A ≤ 85°C		-5		5	°C
		Slope			10		mV/°C
		Offset, T_A = 25°C			720		mV
V_{OH}	FAULT output	High-level output voltage, I_{FAULT} = 4mA		2.7	3.3		V
V_{OL}		Low-level output voltage, I_{FAULT} = 4mA			0	0.6	
I_{LIM}		Overcurrent threshold; Reset, followed by auto-recovery			15[2]		A
	IOUT output	Range		0.15		3.5	V
		Gain, 3A ≤ I_O ≤ 10A		188	200	212	mV/A
		Offset, I_O = 0A, V_O = 1.2V		0	0.3	0.6	V
		Output Impedance			10		kΩ
C_I	External input capacitance	Nonceramic			330 [3]		µF
		Ceramic		22 [3]			
C_O	External output capacitance	Capacitance Value	Nonceramic		330 [4]	5000[5]	µF
			Ceramic	47 [4]			
		Equivalent series resistance (non-ceramic)		1[6]			mΩ

(1) When operating at 12V input and 500kHz, V_O is limited to ≤ 2.0V.
(2) The current limit threshold is the sum of I_O and the peak inductor ripple current.
(3) A 22 µF ceramic input capacitor is required for proper operation. An additional 330 µF bulk capacitor rated for a minimum of 500mA rms of ripple current is recommended. When operating at frequencies > 500kHz the 22 µF ceramic capacitor is only recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(4) A 47 µF ceramic output capacitor is required for basic operation. An additional 330 µF bulk capacitor is recommended for improved transient response. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(5) 5,000 µF is the calculated maximum output capacitance given a 1V/msec output voltage rise time. Additional capacitance or increasing the output voltage rise rate may trigger the overcurrent threshold at start-up. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(6) This is the minimum ESR for all non-ceramic output capacitance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_{IN}	1, 2	The positive input voltage power node to the module, which is referenced to common GND.
PGND	3, 7, 8, 13, 14	The common ground connection for the V_I and V_O power connections.
V_{OUT}	15, 16	The regulated positive power output with respect to GND.
I_{SENSE}	11	Current sense output. The voltage level on this pin represents the average output current of the module.
PWM	4	The PWM input pin. It is a high impedance digital input that accepts 3.3-V or 5-V logic level signals up to 1 MHz.
FF	6	Current limit fault flag. The Fault signal is a 3.3-V digital output which is latched high after an over-current condition. The Fault is reset after a complete PWM cycle without an over-current condition (falling edge of the PWM).
SRE	5	Synchronous Rectifier Enable. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
AGND	9, 10	Analog ground return. It is the 0 V_{dc} reference for the control inputs.
T_{SENSE}	12	Temperature sense output. The voltage level on this pin represents the temperature of the module.
Thermal Pad		This pad is electrically connected to PGND and is the primary thermal conduction cooling path for the module. This pad should be soldered to a grounded copper pad on the host board. For optimum cooling performance, the grounded copper pad should also be tied with multiple vias to the host board internal ground plane. See the Land Pattern drawing for package ECY for recommended pad dimensions.

TOP VIEW   BOTTOM VIEW
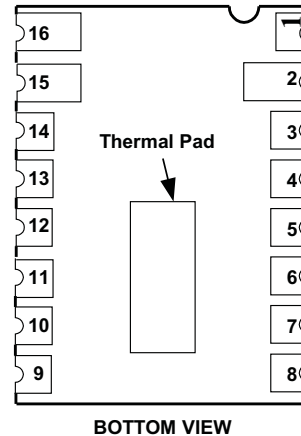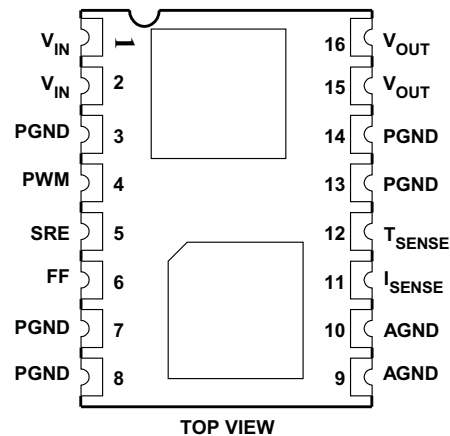
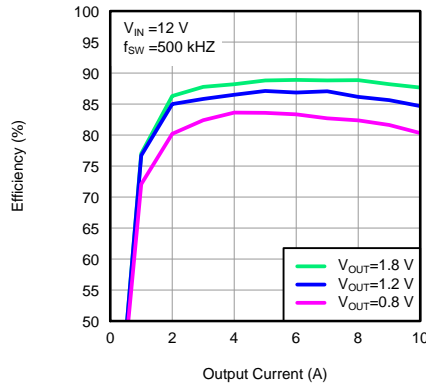# TYPICAL CHARACTERISTICS (V$_I$ = 12 V)

(1) (2)
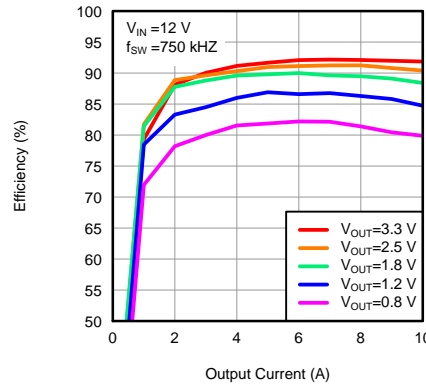

Figure 1. Efficiency

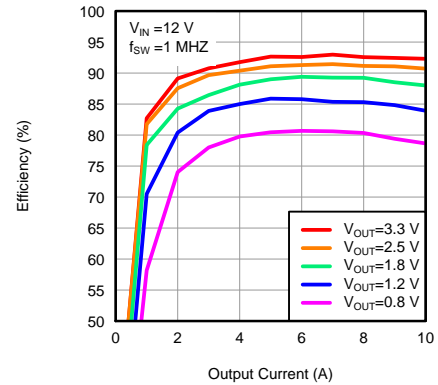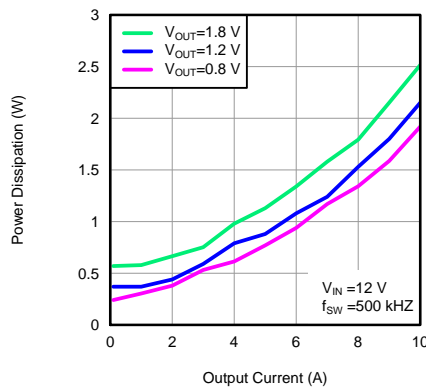
Figure 2. Efficiency

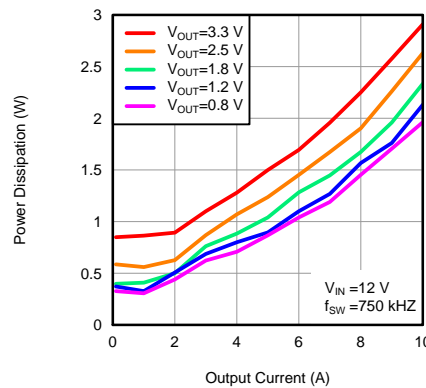Figure 3. Efficiency

Figure 4. Power Dissipation
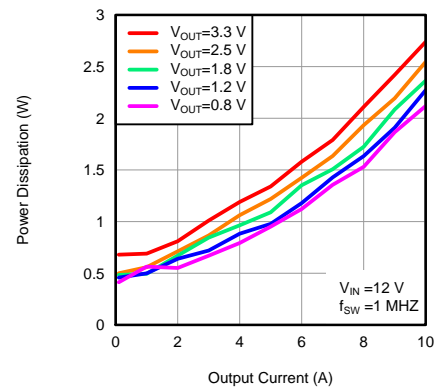

Figure 5. Power Dissipation
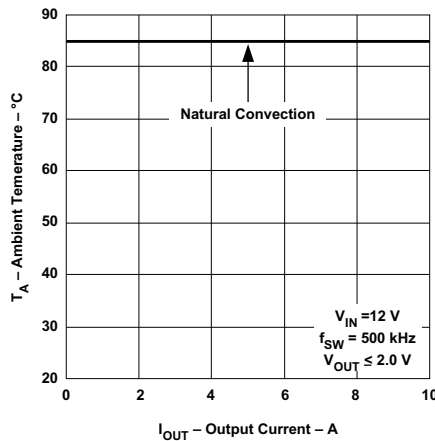

Figure 6. Power Dissipation
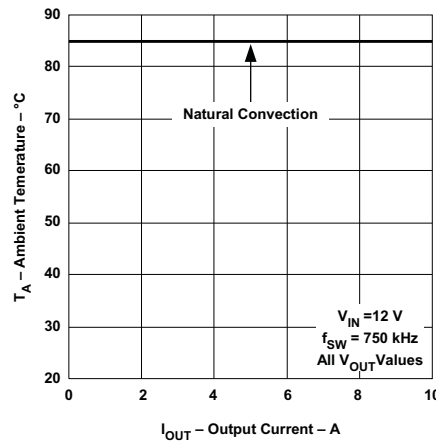

Figure 7. Safe Operating Area
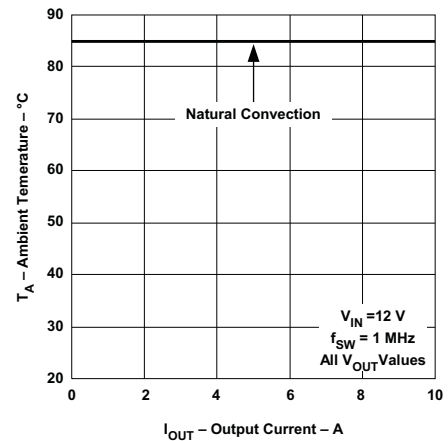

Figure 8. Safe Operating Area

Figure 9. Safe Operating Area

(1) The electrical characteristic data (Figure 1 through Figure 6) has been developed from actual products tested at 25°C. This data is considered typical for the converter.

(2) The temperature derating curves (Figure 7 through Figure 9) represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2-oz. copper. See the Safe Operating Area application section of this datasheet.

Product Folder Link(s): PTD08A210W

TYPICAL CHARACTERISTICS *(V$_I$ = 5 V)*
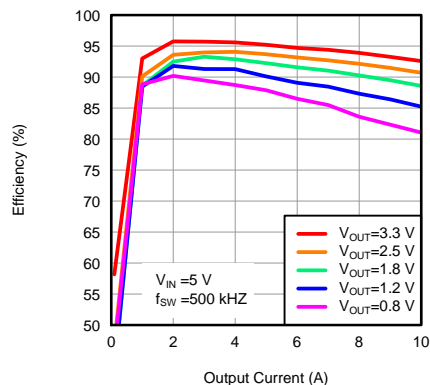
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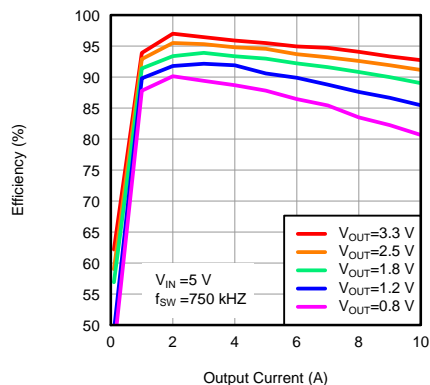

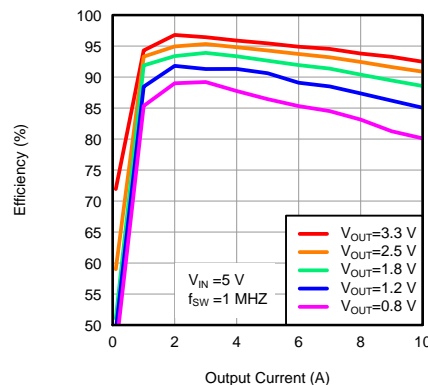**Figure 10. Efficiency**

Figure 11. Efficiency

Figure 12. Efficiency
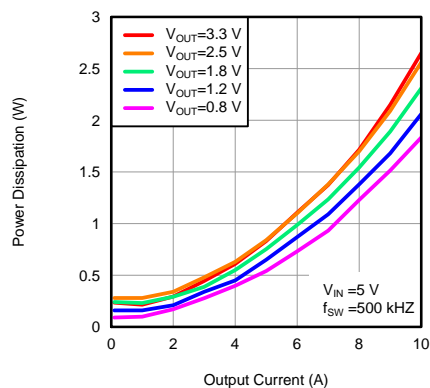
Figure 13. Power Dissipation
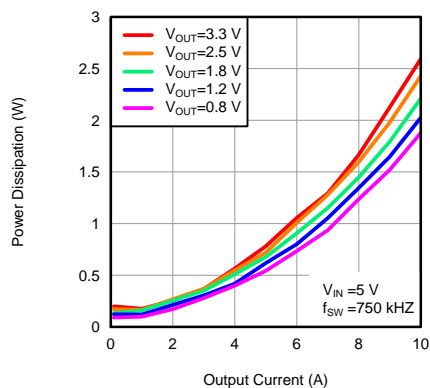
Figure 14. Power Dissipation
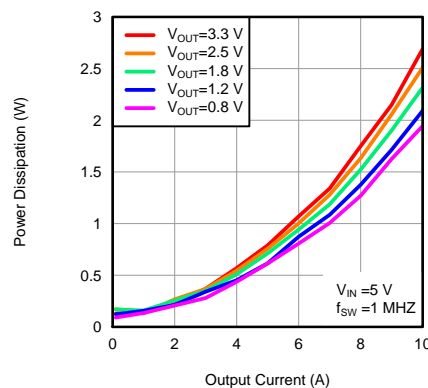
Figure 15. Power Dissipation
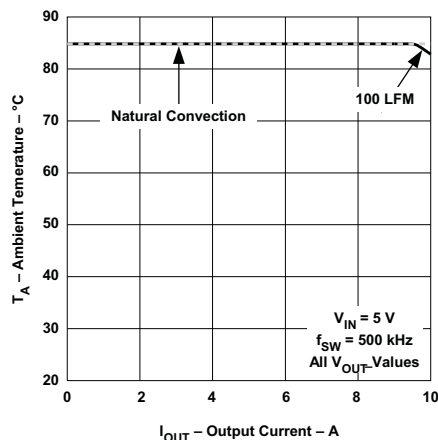
Figure 16. Safe Operating Area
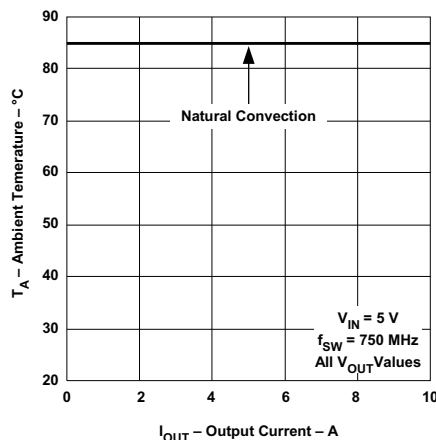
Figure 17. Safe Operating Area
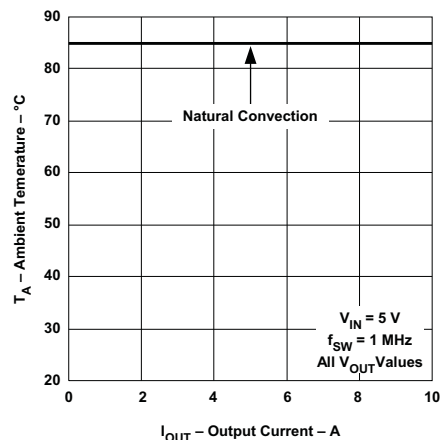
Figure 18. Safe Operating Area

(1)   The electrical characteristic data (Figure 10 through Figure 15) has been developed from actual products tested at 25°C. This data is considered typical for the converter.

(2)   The temperature derating curves (Figure 16 through Figure 18) represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2-oz. copper. See the Safe Operating Area application section of this datasheet.

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TYPICAL CHARACTERISTICS

CURRENT SENSE OUTPUT
vs
OUTPUT CURRENT

Figure 19.

CURRENT SENSE OUTPUT
vs
OUTPUT CURRENT

Figure 20.

TEMPERATURE SENSE
vs
JUNCTION TEMPERATURE
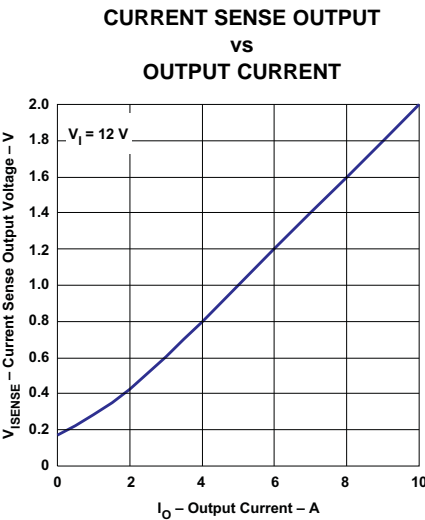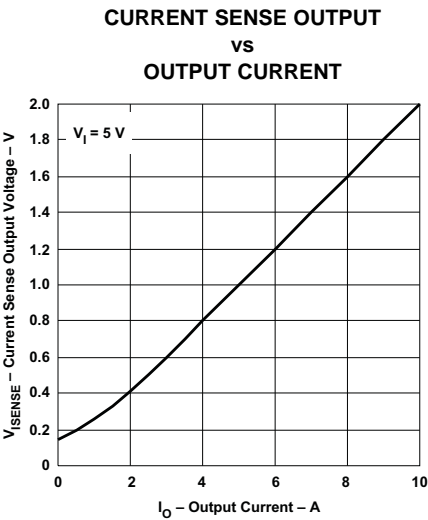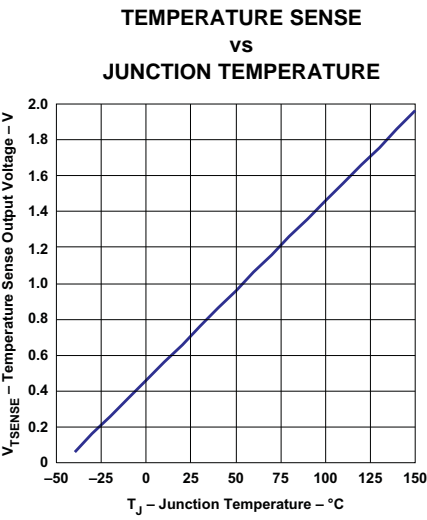
Figure 21.

PTD08A210W

APPLICATION INFORMATION

Digital Power

Figure 22 shows the UCD9220 power supply controller working with a single PTD08A210W, digital powertrain module. The loop for the power supply is created by the voltage output feeding into the Error ADC differential inputs, and completed by the DPWM output feeding the PTD08A210W module. A second stand-alone power stage can be controlled by the UCD9220 controller. The PTD08A210W's output cannot be paralleled. It can only be used as a single stand-alone 10-A module.
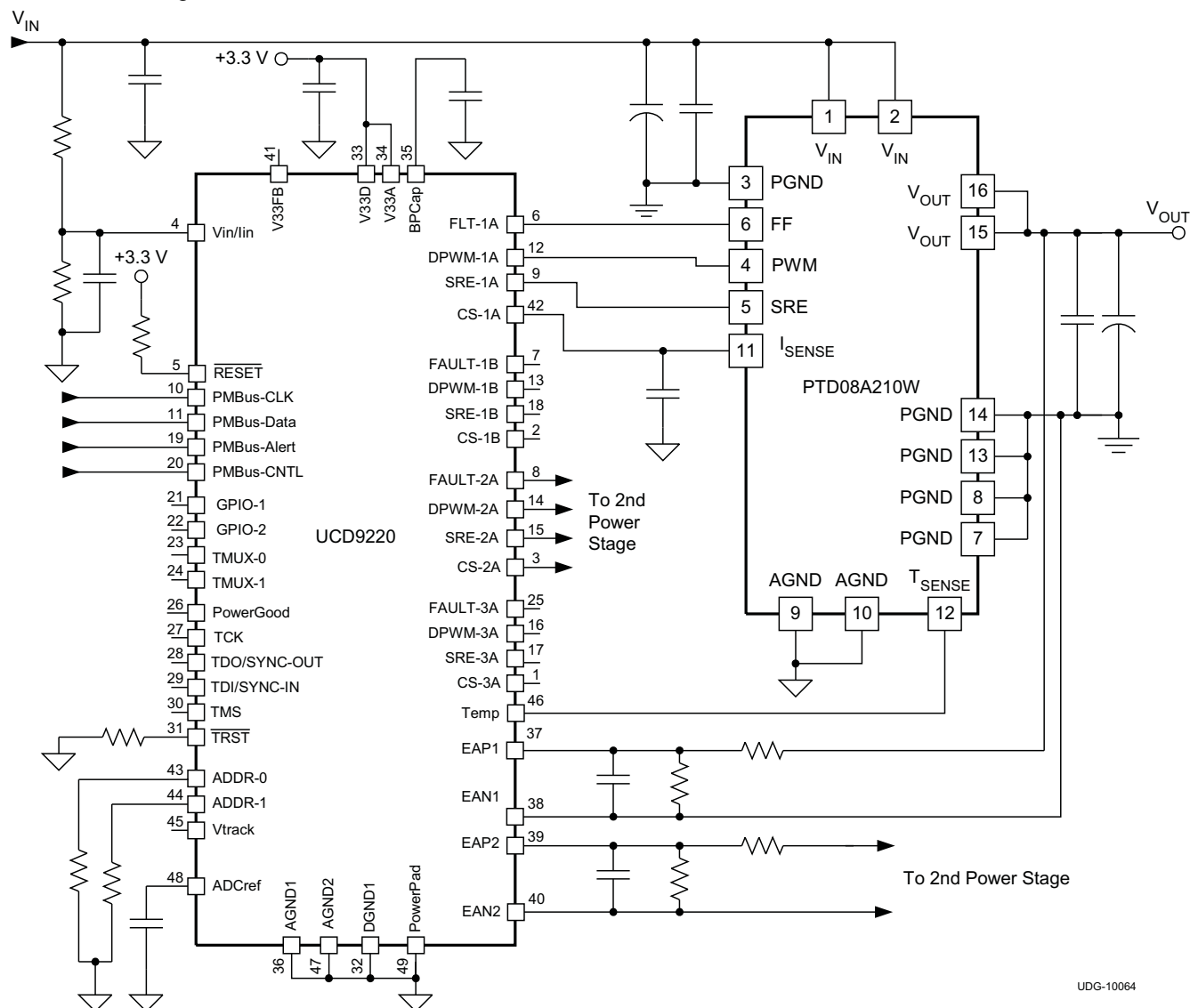
Figure 22. Typical Dual-Output Application Schematic

Note: A low dropout linear regulator such as the TI TPS715A33 can provide the 3.3-V bias power to the UCD9220.

Fusion Digital Power Graphical User Interface (GUI)

When using the UCD92x0 digital controller along with digital PowerTrain modules to design a digital power system, several internal parameters of the modules are required to run the Fusion Digital Power Designer GUI. See the plant parameters below for the PTD08A210W digital PowerTrain modules.

Table 1. PTD08A210W Plant Parameters

PTD08A210W Plant Parameters			
L (µH)	DCR (mΩ)	$R_{DS(on)}$-high (mΩ)	$R_{DS(on)}$-low (mΩ)
0.47	2.6	15.5	6.5

Internal output capacitance is present on the digital PowerTrain modules themselves. When using the GUI interface this capacitance information must be included along with any additional external capacitance. See the capacitor parameters below for the PTD08A210W digital PowerTrain modules.

Table 2. PTD08A210W Capacitor Parameters

PTD08A210W Capacitor Parameters			
C (µF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	1

Product Folder Link(s): *PTD08A210W*

TAPE & REEL

USER DIRECTION OF FEED

REEL AND TAPE ORIENTATION

4.0

2.0

24.00

1.75

"Y"

"X"

PIN 1

DEVICE SUFFIX	INFO
TAPE WIDTH	44mm (1.732")
PITCH	24mm (0.945")
REEL SIZE	13" DIA.
DEVICES/REEL	250

PTDXXXXX	"X"	"Y"
PTD08A210	0mm	25.28mm

Submit Documentation Feedback

Product Folder Link(s): PTD08A210W

TRAY

207.98
203.84

"Y" PITCH

"B"

0.000

"A"

"X" PITCH

0.000

252.43

076-00394

PETE

PICKUP AREA
SEE NOTE

PIN 1

1

NOTE: THE INDUCTOR IS USED TO PICK
AND PLACE THE MODULE. IT'S LOCATION
MAY VARY FROM PACKAGE STYLE. SEE
PRODUCT TABLE

PTDXXXXXX	"A"	"B"	"X"	"Y"
PTD08A210	31.08	26.95	33.61	29.85
ALL DIMENSIONS ARE IN MILLIMETER.				

DEVICES/TRAY	42

PACKAG

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Pea
PTD08A210WAC	ACTIVE	DIP MODULE	ECY	16	42	TBD	Call TI	Call TI
PTD08A210WACT	PREVIEW	DIP MODULE	ECY	16	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www. information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

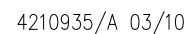**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Cu

0.800 (20,32)

0.600
(15,24)

1

0.050
(1,27)

0.100 (2,54)
7 Places

0.700 (17,78)

0.236 (6,00)
MAX.

0.320 (8,13)

0.575
(14,61)

0.075 (1,91)
9 Places

1

0.305 (7,75)

0.095 (2,41)

0.130 (3,30)
7 Places

0.050
(1,27)

0.060 (1,52)
16 Places

0.100 (2,54)
14 Places

4210935/A 03/10

NOTES: A.   All linear dimensions are in inches (mm).
         B.   This drawing is subject to change without notice.
         C.   2 place decimals are ±0.030 (±0,76mm).
         D.   3 place decimals are ±0.010 (±0,25mm).

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DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
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Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
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