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EMC OPTIMIZED CAN TRANSCEIVER

Check for Samples :SN65HVD1050-EP

FEATURES

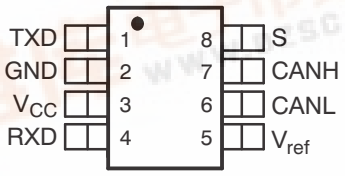
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Improved Replacement for the TJA1050**
- **High Electromagnetic Immunity (EMI)**
- **Very Low Electromagnetic Emissions (EME)**
- **Meets or Exceeds the Requirements of ISO 11898-2**
- **Bus-Fault Protection of –27 V to 40 V**
- **Dominant Time-Out Function**
- **Thermal Shutdown Protection**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance With Low V_{CC}**
  - **Monotonic Outputs During Power Cycling**

APPLICATIONS

- **Industrial Automation**
  - **DeviceNET™ Data Buses (Vendor ID #806)**
- **SAE J2284 High-Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



DESCRIPTION/ ORDERING INFORMATION

The SN65HVD1050 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a controller area network (CAN). The device is also qualified for use in automotive applications in accordance with AEC-Q100.(2)

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)(3).

Designed for operation in especially harsh environments, the SN65HVD1050 features cross-wire, overvoltage, and loss of ground protection from –27 V to 40 V, overtemperature protection, a –12-V to 12-V common-mode range, and withstands voltage transients from –200 V to 200 V, according to ISO 7637.

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

(2) The device is available with Q100 qualification as the SN65HVD1050Q (Product Preview).
(3) The signaling rate of a line is the number of voltage transitions that are made, per second, expressed in the units bps (bits per second).

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKED AS	ORDERING NUMBER
SN65HVD1050M	SOIC-8	1050EP	SN65HVD1050MDREP (reel)

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

If a high logic level is applied to the S pin of the SN65HVD1050, the device enters a listen-only silent mode, during which the driver is switched off while the receiver remains fully functional.

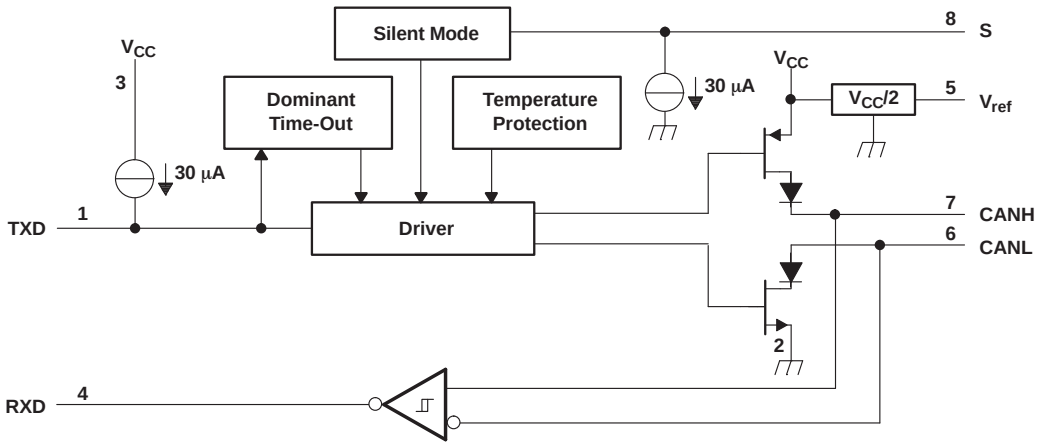
In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required, the local protocol controller reverses this low-current silent mode by placing a logic low on the S pin to resume full operation.

A dominant-time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{ref} (pin 5) is available as a $V_{CC}/2$ voltage reference.

The SN65HVD1050M is characterized for operation from –55°C to 125°C.

FUNCTION BLOCK DIAGRAM



Absolute Maximum Ratings(1)

		UNIT
V_{CC}	Supply voltage(2)	–0.3 V to 7 V
	Voltage range at any bus terminal (CANH, CANL, V_{ref})	–27 V to 40 V
I_O	Receiver output current	20 mA
V_I	Voltage input, transient pulse(3) (CANH, CANL)	–200 V to 200 V
V_I	Voltage input range (TXD, S)	–0.5 V to 6 V
T_J	Junction temperature	–55°C to 170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7

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Electrostatic Discharge Protection

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		UNIT
Electrostatic discharge(1)	Human-Body Model(2)	Bus terminals and GND	±8 kV
		All pins	±4 kV
	Charged-Device Model(3)	All pins	±1.5 kV
	Machine Model		±200 V

(1) All typical values at 25°C
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A
(3) Tested in accordance with JEDEC Standard 22, Test Method C101

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, S	2	5.25	V
V_{IL}	Low-level input voltage	TXD, S	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		2	
T_J	Junction temperature	See Thermal Characteristics table, 1-Mbps minimum signaling rate with R_L = 54 Ω		150	°C

Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	5-V supply current	Silent mode	S at V_{CC}, V_I = V_{CC}		6	10	mA
		Dominant	V_I = 0 V, 60-Ω load, S at 0 V		50	70	
		Recessive	V_I = V_{CC}, No load, S at 0 V		6	10	

Device Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	S at 0 V, See Figure 9	90	230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		90	230	

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Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2.9	3.4	4.5	V
		CANL		0.8		1.5	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, S at 0 V, See Figure 1 and Figure 2	–0.012		0.012	V
			V_I = 3 V, S at 0 V, No load	–0.5		0.05	
$V_{OC(ss)}$	Steady-state common-mode output voltage		S at 0 V, See Figure 8	2	2.3	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage				30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	μA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL open, See Figure 11	–105	–72		mA
			V_{CANH} = 12 V, CANL open, SeeFigure 11		0.36	1	
			V_{CANL} = –12 V, CANH open, See Figure 11	–1	–0.5		
			V_{CANL} = 12 V, CANH open, See Figure 11		71	105	
C_O	Output capacitance		See receiver input capacitance				

(1) All typical values are at 25°C, with a 5-V supply.

Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	S at 0 V, See Figure 4	25	65	120	ns
t_{PHL}	Propagation delay time, high- to low-level output		25	45	120	
t_r	Differential output signal rise time	S at 0 V, See Figure 4		25		ns
t_f	Differential output signal fall time			50		
t_{en}	Enable time from silent mode to dominant	See Figure 7			1	μs
$t_{(dom)}$	Dominant time-out	↓V_I, See Figure 10	300	450	700	μs

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Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0 V, See Table 3		800	900	mV
V_{IT-}	Negative-going input threshold voltage	S at 0 V, See Table 3	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 6	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 6		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5 V, Other pin at 0 V, V_{CC} at 0 V, TXD at 0 V		165	250	μA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	μA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		5		pF
R_{ID}	Differential input resistance	TXD at 3 V, S at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, S at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $[1 - (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	$V_{O(CANH)} = V_{O(CANL)}$	–3%	0%	3%	

(1) All typical values are at 25 C with a 5-V supply.

Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	S at 0 V or V_{CC}, See Figure 6	60	100	130	ns
t_{PHL}	Propagation delay time, high- to low-level output		45	70	130	
t_r	Output signal rise time	S at 0 V or V_{CC}, See Figure 6		8		ns
t_f	Output signal fall time			8		

S-Pin Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	S at 2 V	20	40	70	μA
I_{IL}	Low-level input current	S at 0.8 V	5	20	30	μA

V_{ref}-PIN Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–50 μA < I_O < 50 μA	0.4 V_{CC}	0.5 V_{CC}	0.6 V_{CC}	V

Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction to Air	Low-K thermal resistance (1)		211		°C/W
		High-K thermal resistance		131		
θ_{JB}	Junction-to-board thermal resistance			53		°C/W
θ_{JC}	Junction-to-case thermal resistance			79		°C/W

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages

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Thermal Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD a 500-kHz, 50% duty-cycle square wave, C_L at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_j = 130°C, R_L = 45 Ω, S at 0 V, Input to TXD a 500-kHz, 50% duty-cycle square wave, C_L at RXD = 15 pF			170	
Thermal shutdown temperature				190		°C

FUNCTION TABLES

Table 1. DRIVER

INPUTS		OUTPUTS		BUS STATE
TXD (1)	S (1)	CANH (1)	CANL (1)	
L	L or Open	H	L	Dominant
H	X	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	H	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 2. RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{(CANH)} - V_{(CANL)}$	OUTPUT RXD (1)	BUS STATE
$V_{ID} \geq 0.9$ V	L	Dominant
0.5 V < V_{ID} < 0.9 V	?	?
$V_{ID} \leq 0.5$ V	H	Recessive
Open	H	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate

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PARAMETER MEASUREMENT INFORMATION

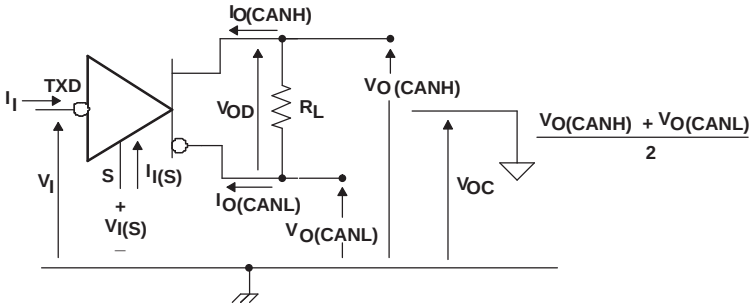

Figure 1. Driver Voltage, Current, and Test Definition

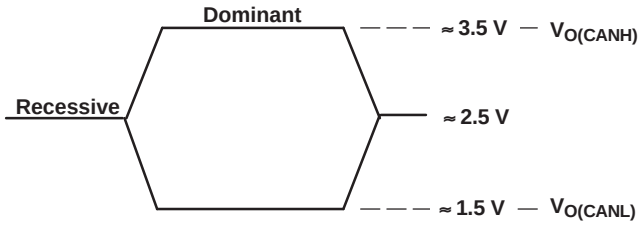

Figure 2. Bus Logic State Voltage Definitions

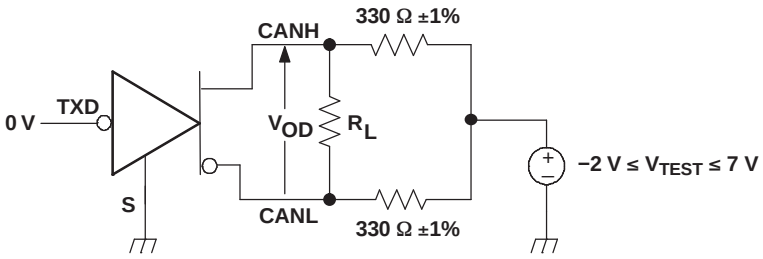

Figure 3. Driver V_{OD} Test Circuit

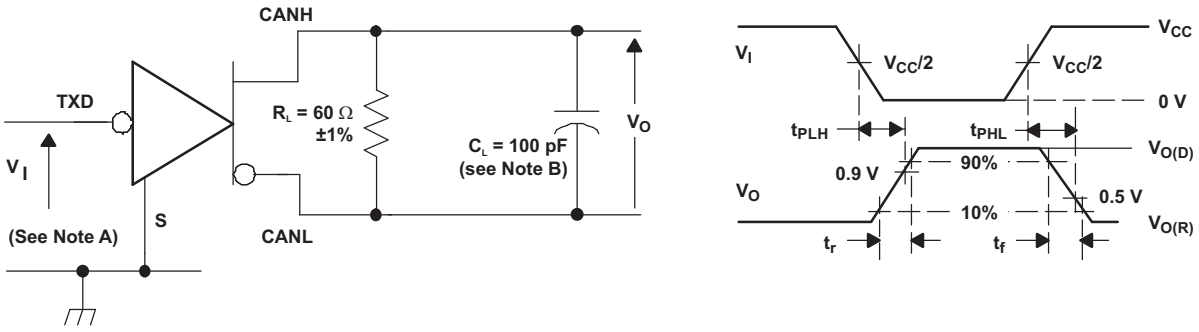

Figure 4. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)

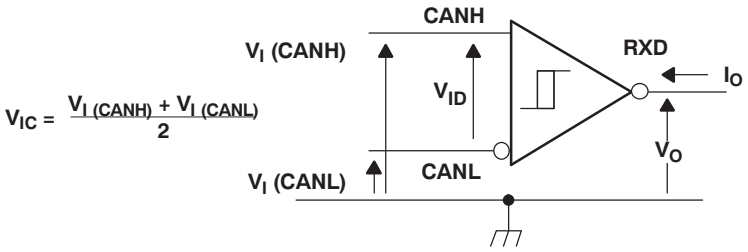
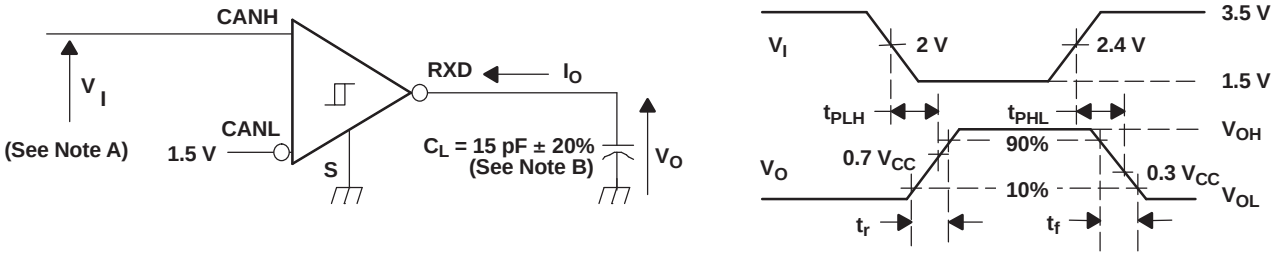


Figure 5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 3. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

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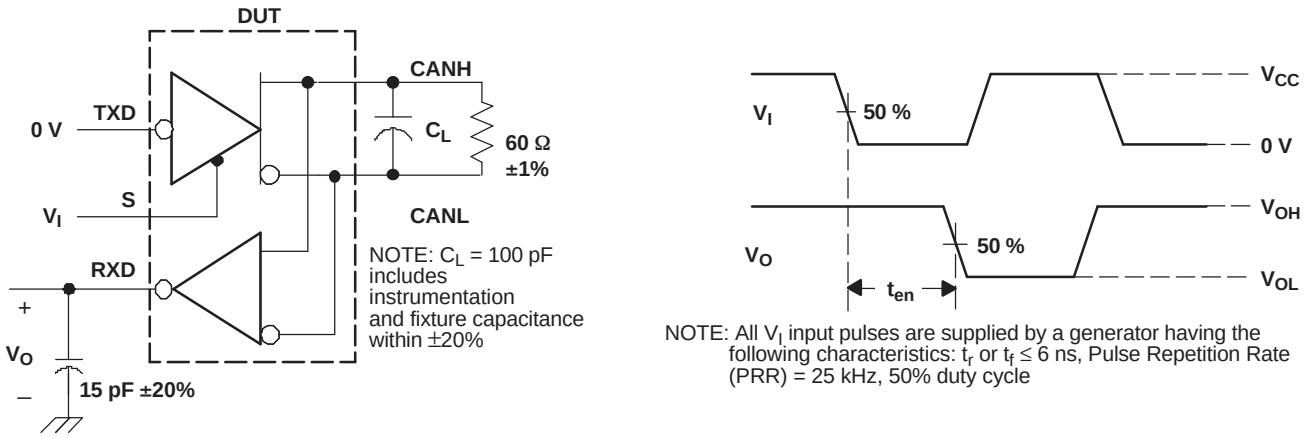
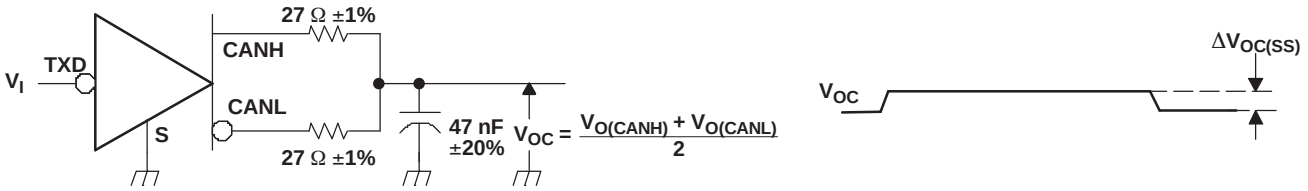
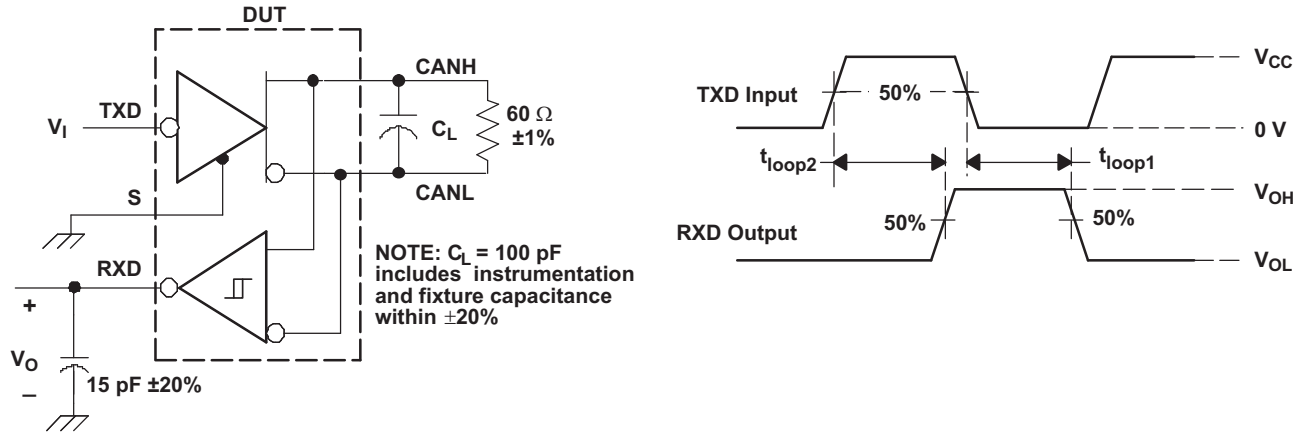


Figure 7. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common-Mode Output Voltage Test and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveform

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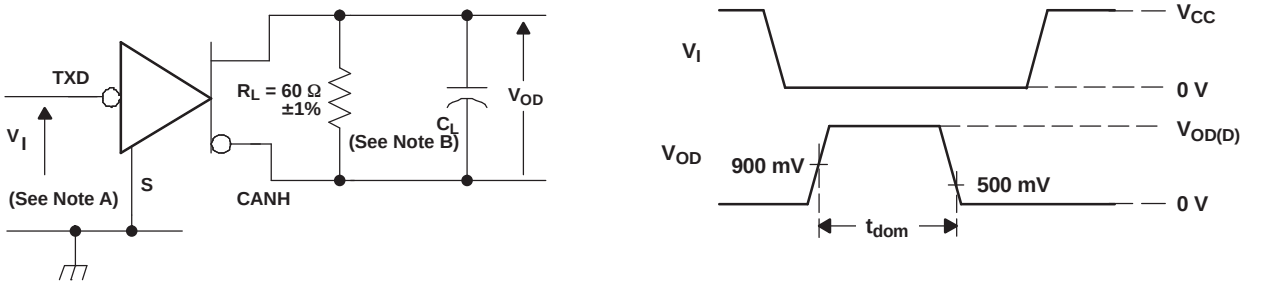

A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

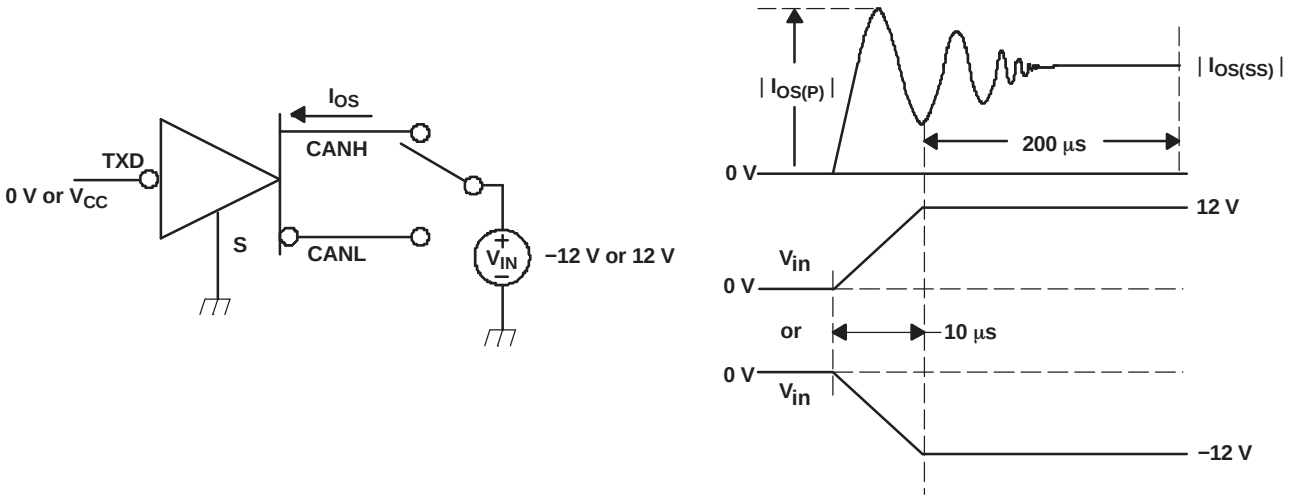

Figure 11. Driver Short-Circuit Current Test and Waveforms

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DEVICE INFORMATION

Table 4. Parametric Cross-Reference With the TJA1050

TJA1050 (1)	PARAMETER	HVD1050
Transmitter Section		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
Bus Section		
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{i(dif)(hys)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{O(dif)(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(dif)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
C_I	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
Receiver Section		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
V_{ref}-Pin Section		
V_{ref}	Reference output voltage	V_O
Timing Section		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
	$t_{d(TXD-BUSon)} + t_{d(BUSon-RXD)}$	Device t_{LOOP1}
	$t_{d(TXD-BUSoff)} + t_{d(BUSoff-RXD)}$	Device t_{LOOP2}
$t_{dom(TXD)}$	Dominant time-out	Driver $t_{(dom)}$
S-Pin Section		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1050 Product Specification, Philips Semiconductors, 2002 May 16

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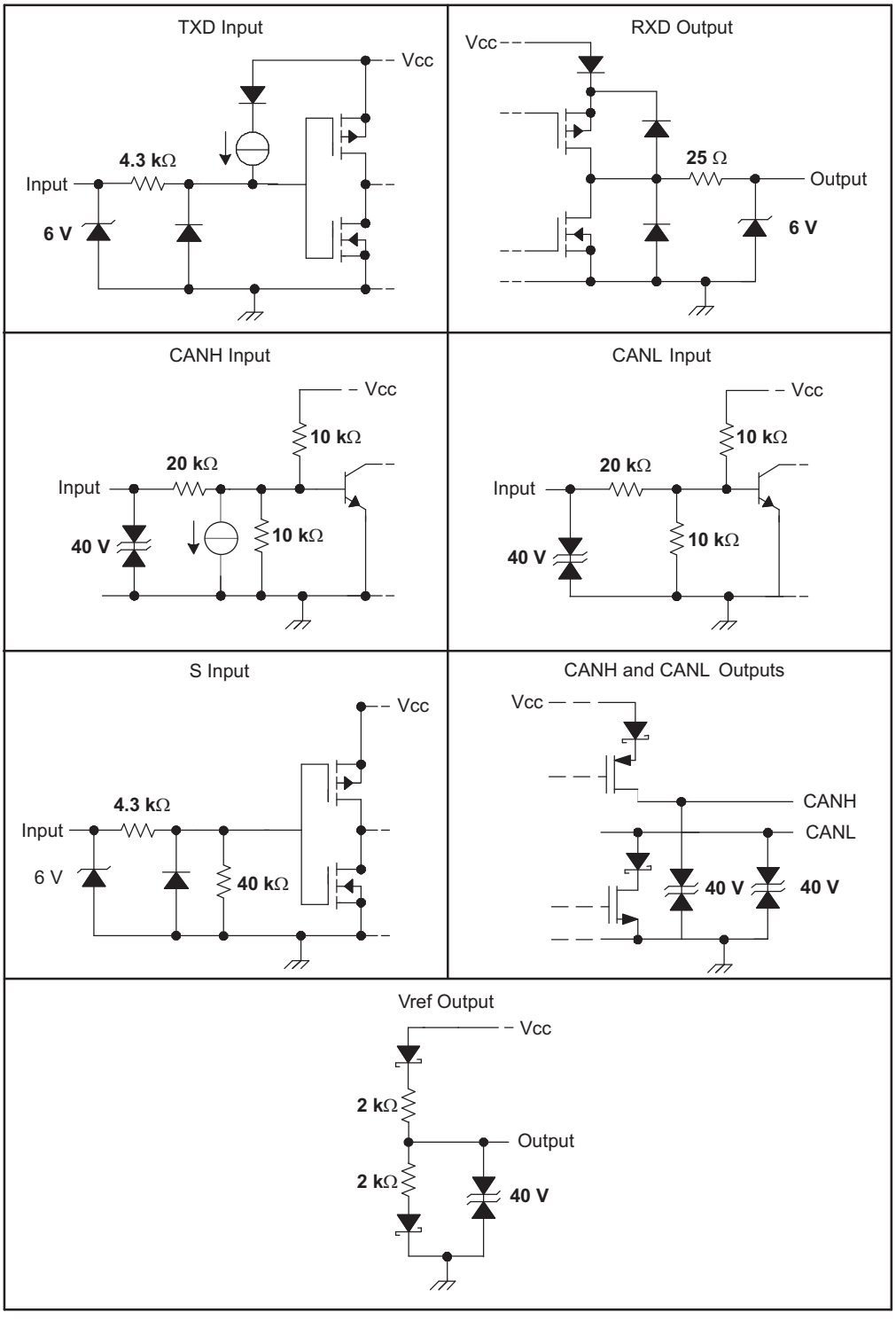
Equivalent Input and Output Schematic Diagrams



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TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (Across V_{CC})

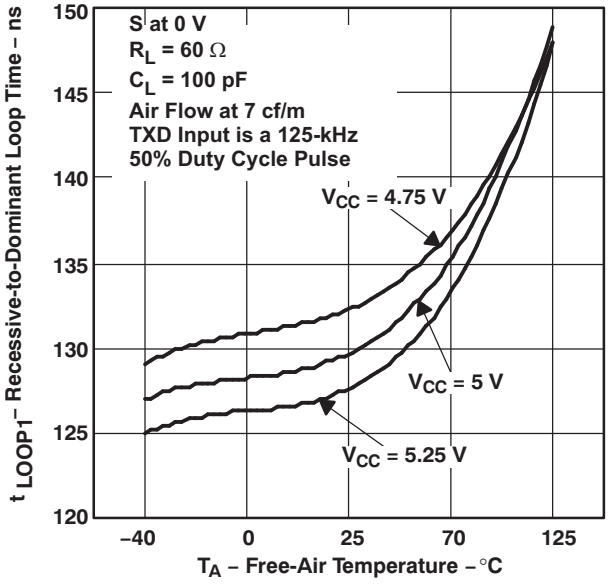

Figure 12.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (Across V_{CC})

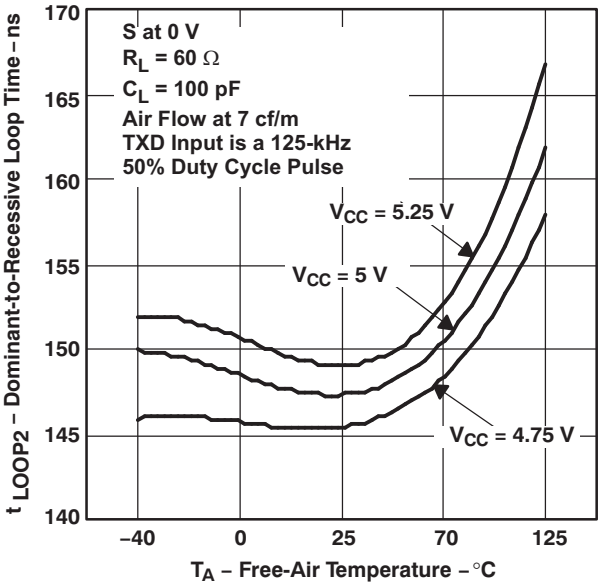

Figure 13.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE

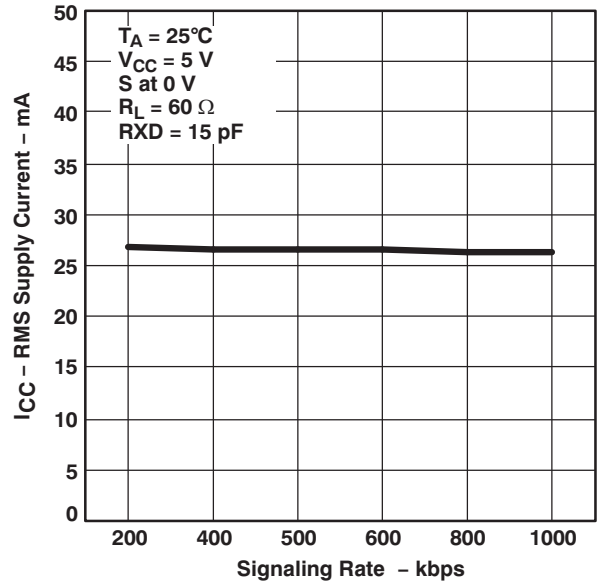

Figure 14.

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

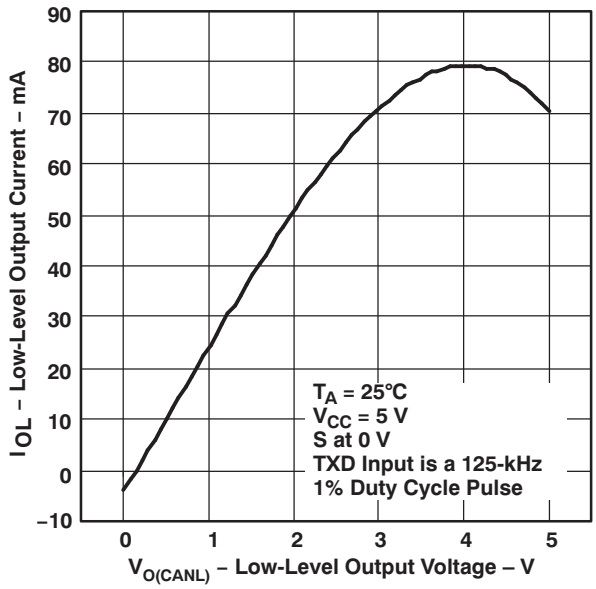

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

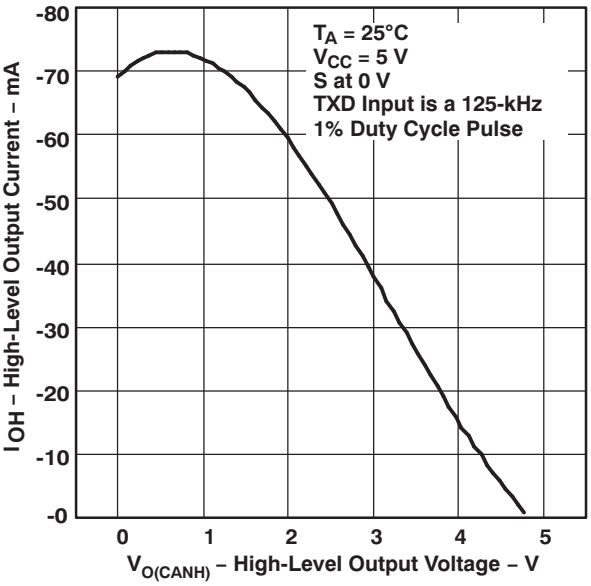

Figure 16.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE (Across V_{CC})

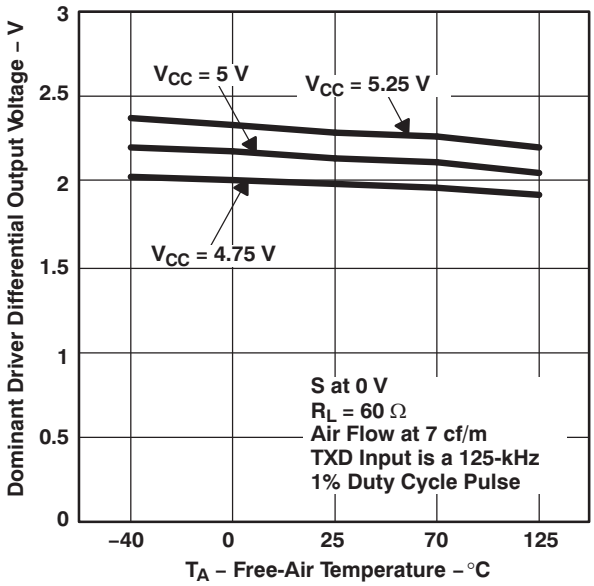

Figure 17.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

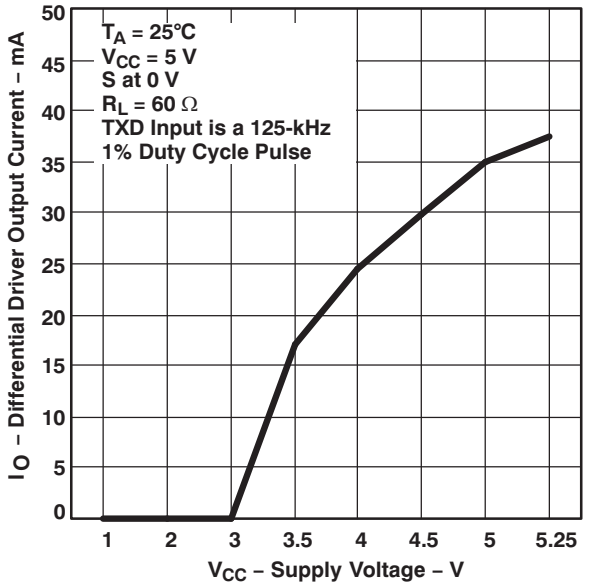

Figure 18.

RECEIVER OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

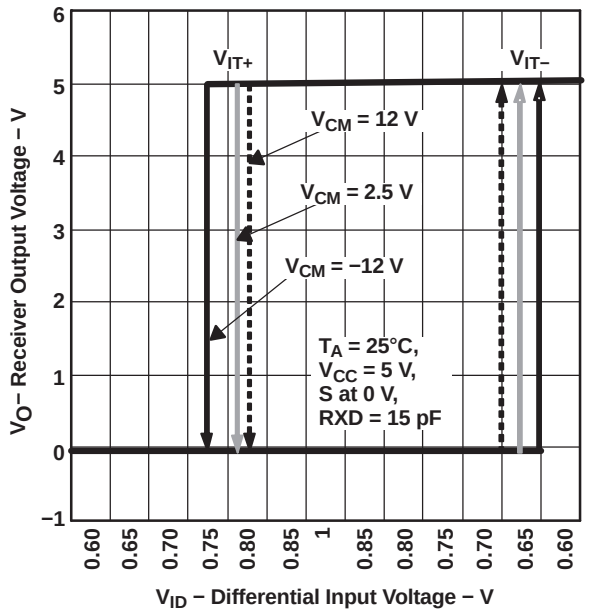

Figure 19.

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TYPICAL CHARACTERISTICS (continued)

TYPICAL ELECTROMAGNETIC EMISSIONS UP TO 50 MHZ (Peak Amplitude)

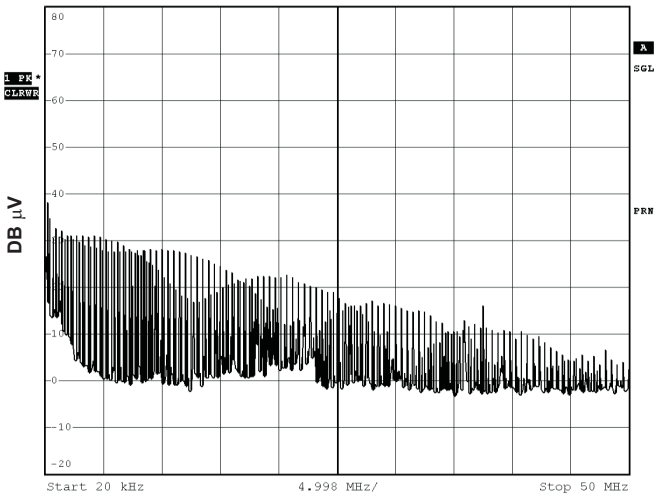

Figure 20.

TYPICAL ELECTROMAGNETIC IMMUNITY PERFORMANCE

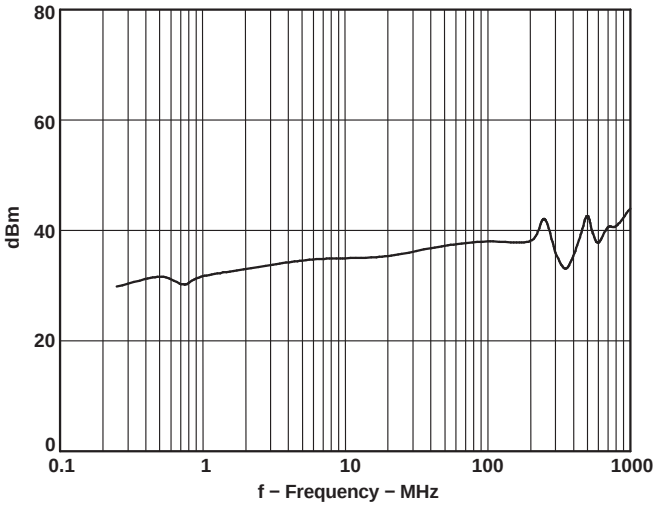

Figure 21.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1050MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1050MDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/07608-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD1050-EP :
- Catalog: SN65HVD1050
- Automotive: SN65HVD1050-Q1

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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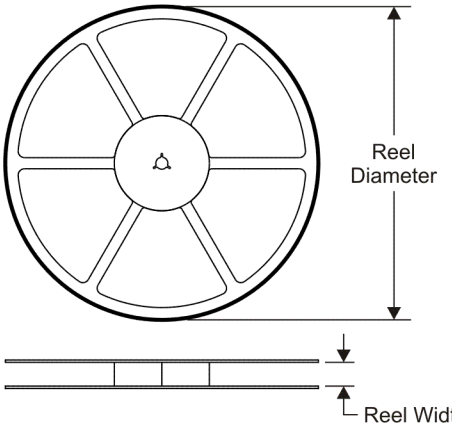
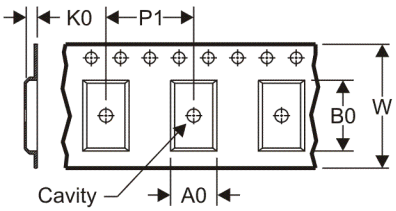
TAPE AND REEL INFORMATION

REEL DIMENSIONS

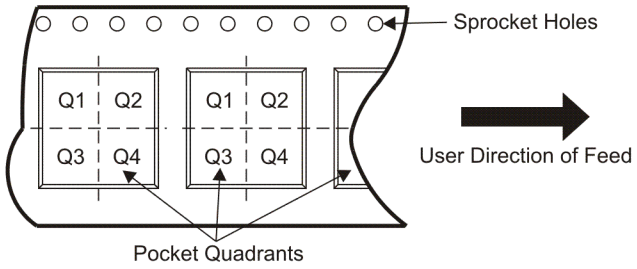


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1050MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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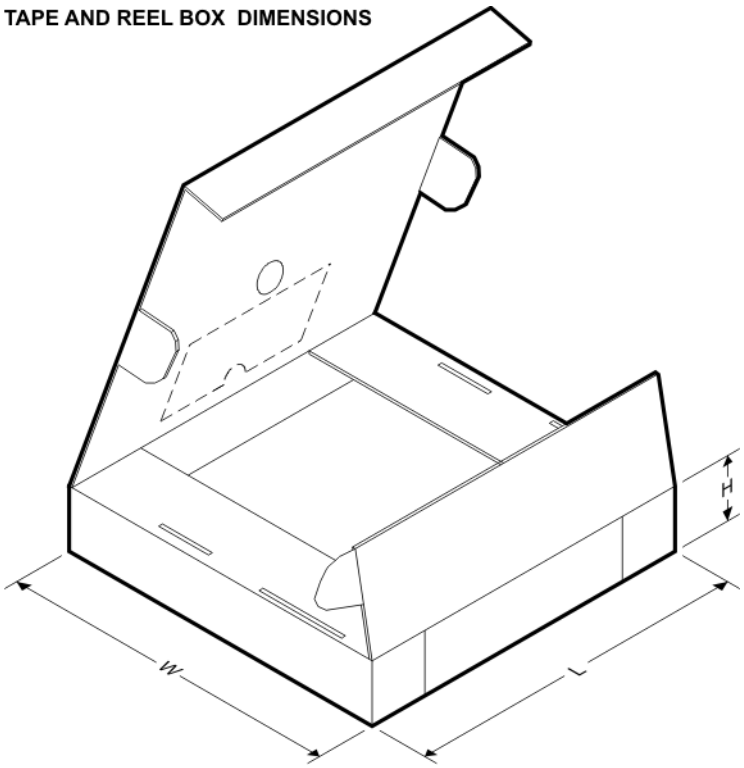
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1050MDREP	SOIC	D	8	2500	346.0	346.0	29.0

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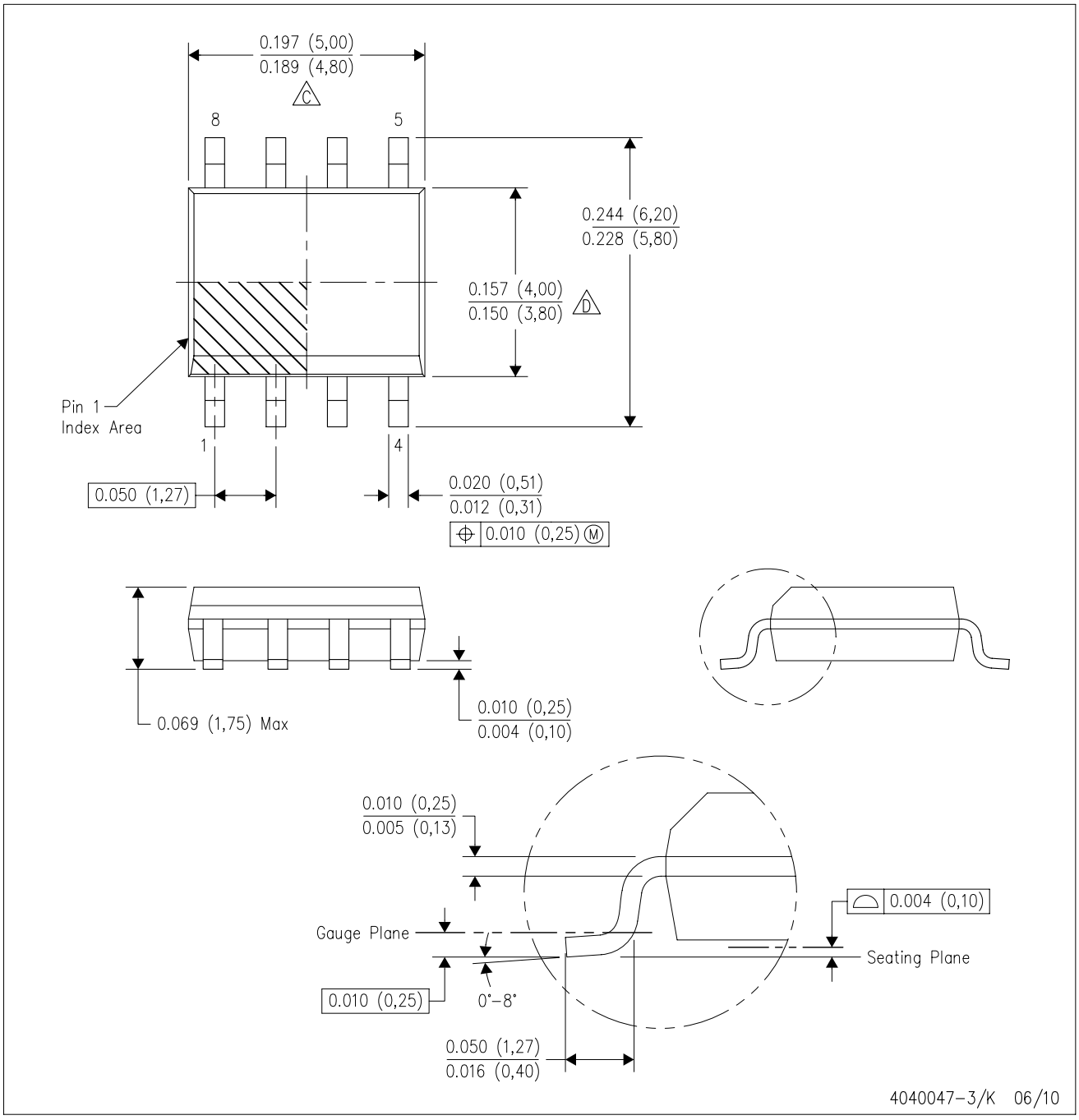
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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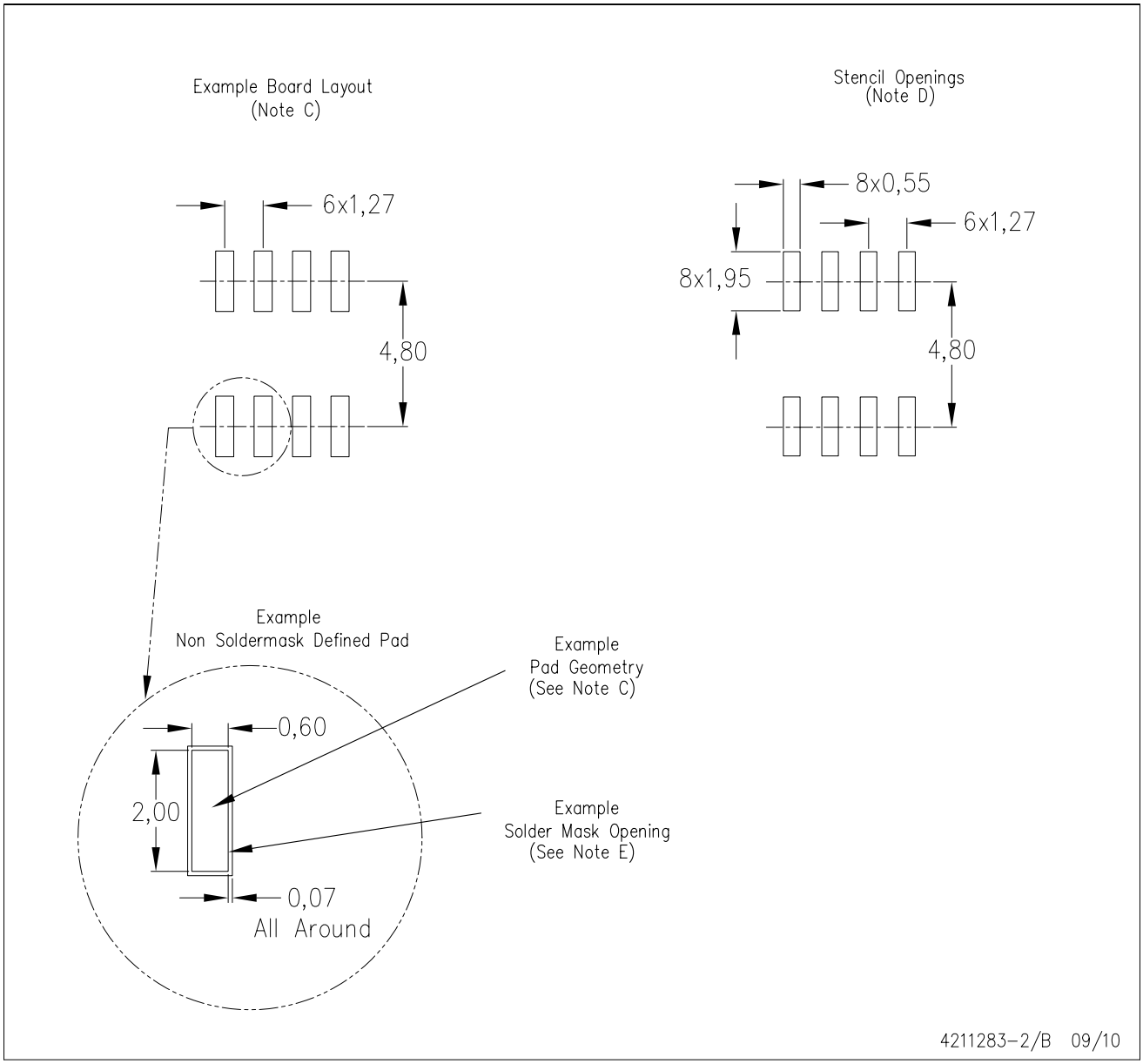
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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