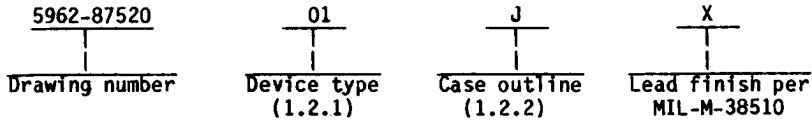




1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

| Device type | Generic number | Circuit function            |
|-------------|----------------|-----------------------------|
| 01          | 8253           | Programmable interval timer |
| 02          | 8253           | Programmable interval timer |
| 03          | 8253-5         | Programmable interval timer |

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline   |
|----------------|--|
| J              | D-3 (24-lead, 1/2" x 1-1/4"), dual-in-line package <span style="float: right;"><i>Diagram 6</i></span> |

1.3 Absolute maximum ratings.

|  |                             |
|--|-----------------------------|
| Supply voltage range - - - - -                                 | -0.5 V dc to +7.0 V dc      |
| Input voltage range with respect to ground (any pin) - - - - - | -0.5 V dc to +7.0 V dc      |
| Storage temperature range - - - - -                            | -65°C to +150°C             |
| Maximum power dissipation (P <sub>D</sub> ) - - - - -          | 1 W                         |
| Lead temperature (soldering, 10 seconds) - - - - -             | +270°C                      |
| Thermal resistance, junction-to-case (θ <sub>JC</sub> ):       |                             |
| Case J - - - - -   | See MIL-M-38510, appendix C |
| Junction temperature (T <sub>J</sub> ) - - - - -               | +150°C                      |

1.4 Recommended operation conditions.

|   |                            |
|---|----------------------------|
| Supply voltage (V <sub>CC</sub> ) - - - - -                   | 5 V dc ±10% for dc testing |
| Supply voltage (V <sub>CC</sub> ):                            |                            |
| 01 and 03 devices - - - - -                                   | 5 V dc ±10% for ac testing |
| 02 device - - - - -   | 5 V dc ±5% for ac testing  |
| Minimum high-level input voltage (V <sub>IH</sub> ) - - - - - | 2.2 V dc                   |
| Minimum low-level input voltage (V <sub>IL</sub> ) - - - - -  | -0.5 V dc                  |
| Maximum high-level input voltage (V <sub>IH</sub> ) - - - - - | V <sub>CC</sub> +0.5 V dc  |
| Maximum low-level input voltage (V <sub>IL</sub> ) - - - - -  | 0.7 V dc                   |
| Case operating temperature range (T <sub>C</sub> ) - - - - -  | -55°C to +125°C            |

|  |           |                                 |                       |
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2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table 1 and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

|  |      |                 |            |
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TABLE I. Electrical performance characteristics.

| Test                                     | Symbol           | Conditions<br>-55°C < T <sub>C</sub> < +125°C<br>unless otherwise specified  | Group A<br>subgroups | Device<br>types | Limits |     | Unit |
|--|------------------|--|----------------------|-----------------|--------|-----|------|
|  |                  |  |                      |                 | Min    | Max |      |
| Input low voltage                        | V <sub>IL</sub>  | V <sub>CC</sub> = 5 V ±10%   | 1, 2, 3              | A11             |        | .7  | V    |
| Input high voltage                       | V <sub>IH</sub>  | V <sub>CC</sub> = 5 V ±10%   | 1, 2, 3              | A11             | 2.2    |     | V    |
| Output low voltage                       | V <sub>OL</sub>  | V <sub>CC</sub> = 5 V ±10%<br>I <sub>OL</sub> = 1.6 mA   | 1, 2, 3              | A11             |        | .45 | V    |
| Output high voltage                      | V <sub>OH</sub>  | V <sub>CC</sub> = 5 V ±10%<br>I <sub>OH</sub> = -150 μA  | 1, 2, 3              | A11             | 2.4    |     | V    |
| Input load current                       | I <sub>IL</sub>  | V <sub>CC</sub> = 5.5 V<br>V <sub>IN</sub> = V <sub>CC</sub> to 0 V  | 1, 2, 3              | A11             |        | ±20 | μA   |
| Output float leakage                     | I <sub>OFL</sub> | V <sub>CC</sub> = 5.5 V<br>V <sub>OUT</sub> = V <sub>CC</sub> to 0 V   | 1, 2, 3              | A11             |        | ±20 | μA   |
| V <sub>CC</sub> supply current <u>1/</u> | I <sub>CC</sub>  | V <sub>CC</sub> = 5.5 V<br>Outputs unloaded static   | 1, 2, 3              | A11             |        | 160 | mA   |
| Input capacitance                        | C <sub>IN</sub>  | See 4.3.1d<br>F <sub>C</sub> = 1 MHz<br>T <sub>A</sub> = 25°C; V <sub>CC</sub> = GND = 0 V                                   | 4                    | A11             |        | 10  | pF   |
| Input/output capacitance                 | C <sub>I/O</sub> | Unmeasured pins returned<br>to V <sub>SS</sub><br>T <sub>A</sub> = 25°C; V <sub>CC</sub> = GND = 0 V                         | 4                    | A11             |        | 20  | pF   |
| Address stable before RD                 | t <sub>AR</sub>  | V <sub>CC</sub> = 5 V ±10% for 01 and 03 devices<br>V <sub>CC</sub> = 5 V ±5% for 02 device<br>See figures 4 and 5 <u>2/</u> | 9, 10, 11            | 01,02           | 50     |     | ns   |
|  |                  |  |                      | 03              | 30     |     | ns   |

See footnotes at end of table.

|  |           |                                 |                       |
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TABLE I. Electrical performance characteristics - Continued.

| Test  | Symbol          | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>unless otherwise specified                       | Group A<br>subgroups | Device<br>types | Limits |     | Unit |
|---|-----------------|---|----------------------|-----------------|--------|-----|------|
|   |                 |   |                      |                 | Min    | Max |      |
| Address hold<br>time for $\overline{RD}$  | t <sub>RA</sub> | V <sub>CC</sub> = 5 V ±10% for 01 and<br>03 devices<br>V <sub>CC</sub> = 5 V ±5% for 02<br>device | 9, 10, 11            | A11             | 5      |     | ns   |
| $\overline{RD}$ pulse<br>width <u>3/</u>  | t <sub>RR</sub> | See figures 4 and 5<br><br><u>2/</u>  | 9, 10, 11            | 01,02           | 400    |     | ns   |
|   |                 |   |                      | 03              | 300    |     | ns   |
| Data delay<br>from $\overline{RD}$ <u>4/</u>  | t <sub>RD</sub> |   | 9, 10, 11            | 01,02           |        | 300 | ns   |
|   |                 |   |                      | 03              |        | 200 | ns   |
| $\overline{RD}$ to data<br>floating <u>5/</u>   | t <sub>DF</sub> |   | 9, 10, 11            | 01,02           | 25     | 125 | ns   |
|   |                 |   |                      | 03              | 25     | 100 | ns   |
| Recovery time<br>between $\overline{RD}$ <u>5/</u><br>and any other<br>control signal | t <sub>RV</sub> |   | 9, 10, 11            | A11             | 1      |     | μs   |
| Address stable<br>before $\overline{WR}$  | t <sub>AW</sub> |   | 9, 10, 11            | 01,02           | 50     |     | ns   |
|   |                 |   |                      | 03              | 30     |     | ns   |
| Address hold<br>time for $\overline{WR}$  | t <sub>WA</sub> |   | 9, 10, 11            | A11             | 30     |     | ns   |
| $\overline{WR}$ pulse width<br><u>3/</u>  | t <sub>WW</sub> |   | 9, 10, 11            | 01,02           | 400    |     | ns   |
|   |                 |   |                      | 03              | 300    |     | ns   |

See footnotes at end of table.

|  |           |                                 |                       |
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TABLE I. Electrical performance characteristics - Continued.

| Test   | Symbol           | Conditions<br>-55°C < T <sub>C</sub> < +125°C<br>unless otherwise specified   | Group A<br>subgroups | Device<br>types | Limits |          | Unit |
|--|------------------|---|----------------------|-----------------|--------|----------|------|
|  |                  |   |                      |                 | Min    | Max      |      |
| Data setup<br>time for $\overline{WR}$   | t <sub>DW</sub>  | V <sub>CC</sub> = 5 V ±10% for 01 and<br>03 devices<br>V <sub>CC</sub> = 5 V ±5% for 02<br>device<br>See figures 4 and 5 2/ | 9, 10, 11            | 01,02           | 300    |          | ns   |
|  |                  |   |                      | 03              | 250    |          | ns   |
| Data hold<br>time for $\overline{WR}$  | t <sub>WD</sub>  |   | 9, 10, 11            | 01,02           | 40     |          | ns   |
|  |                  |   |                      | 03              | 30     |          | ns   |
| Recovery time<br>between $\overline{WR}$ 5/<br>and any other<br>control signal | t <sub>RV</sub>  |   | 9, 10, 11            | A11             | 1      |          | μs   |
| Clock period   | t <sub>CLK</sub> |   | 9, 10, 11            | A11             | 380    | 5/<br>DC | ns   |
| High pulse<br>width  | t <sub>PWH</sub> |   | 9, 10, 11            | A11             | 230    |          | ns   |
| Low pulse<br>width   | t <sub>PWL</sub> |   | 9, 10, 11            | A11             | 150    |          | ns   |
| Gate width<br>high   | t <sub>GW</sub>  |   | 9, 10, 11            | A11             | 150    |          | ns   |
| Gate width<br>low 5/   | t <sub>GL</sub>  |   | 9, 10, 11            | A11             | 100    |          | ns   |
| Gate setup to<br>CLK high  | t <sub>GS</sub>  |   | 9, 10, 11            | A11             | 100    |          | ns   |
| Gate hold<br>after CLK high  | t <sub>GH</sub>  |   | 9, 10, 11            | A11             | 55     |          | ns   |

See footnotes at end of table.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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TABLE I. Electrical performance characteristics - Continued.

| Test                                | Symbol           | Conditions<br>-55°C < T <sub>C</sub> < +125°C<br>unless otherwise specified                       | Group A<br>subgroups | Device<br>types | Limits |     | Unit |
|-------------------------------------|------------------|---|----------------------|-----------------|--------|-----|------|
|                                     |                  |   |                      |                 | Min    | Max |      |
| 4/<br>Output delay<br>from CLK low  | t <sub>OD</sub>  | V <sub>CC</sub> = 5 V ±10% for 01 and<br>03 devices<br>V <sub>CC</sub> = 5 V ±5% for 02<br>device | 9, 10, 11            | All             |        | 400 | ns   |
| 4/<br>Output delay<br>from gate low | t <sub>ODG</sub> | See figures 4 and 5<br>2/   | 9, 10, 11            | All             |        | 300 | ns   |

1/ I<sub>CC</sub> is measured in a static condition with no output loads applied.

2/ Test conditions: V<sub>IL</sub> = 0.45 V V<sub>IH</sub> = 2.4 V  
V<sub>OL</sub> = 0.8 V V<sub>OH</sub> = 2.2 V

3/ If clock low occurs less than 100 ns after the rising edge of READ or WRITE, the counter selected during the READ or WRITE could be affected.

4/ Test condition: C<sub>L</sub> = 100 pF.

5/ Guaranteed, if not tested.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

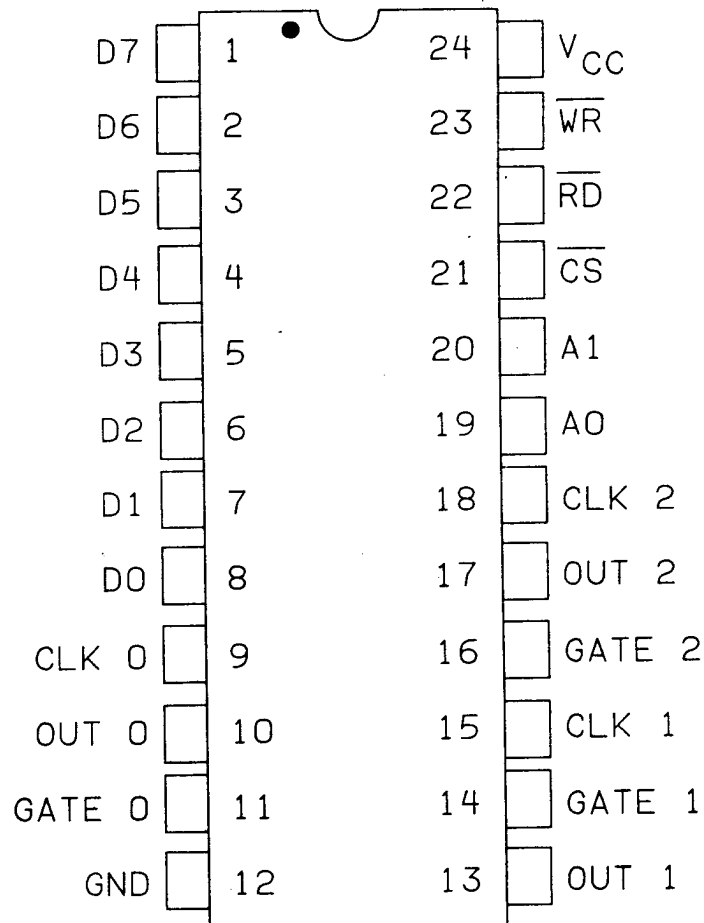
3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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Note: Pin 1 is marked for orientation

FIGURE 1. Terminal connections.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 |                      |
|-----------------|-----------------|-----------------|----|----|----------------------|
| 0               | 1               | 0               | 0  | 0  | Load counter no. 0   |
| 0               | 1               | 0               | 0  | 1  | Load counter no. 1   |
| 0               | 1               | 0               | 1  | 0  | Load counter no. 2   |
| 0               | 1               | 0               | 1  | 1  | Write mode word      |
| 0               | 0               | 1               | 0  | 0  | Read counter no. 0   |
| 0               | 0               | 1               | 0  | 1  | Read counter no. 1   |
| 0               | 0               | 1               | 1  | 0  | Read counter no. 2   |
| 0               | 0               | 1               | 1  | 1  | No-operation 3-state |
| 1               | X               | X               | X  | X  | Disable 3-state      |
| 0               | 1               | 1               | X  | X  | No-operation 3-state |

Control word format

| D7  | D6  | D5  | D4  | D3 | D2 | D1 | D0  |
|-----|-----|-----|-----|----|----|----|-----|
| SC1 | SC0 | RL1 | RLO | M2 | M1 | MO | BCD |

Definition of control

SC - Select counter:

SC1 SC0

|   |   |                  |
|---|---|------------------|
| 0 | 0 | Select counter 0 |
| 0 | 1 | Select counter 1 |
| 1 | 0 | Select counter 2 |
| 1 | 1 | Illegal          |

RL1 RLO

|   |   |   |
|---|---|---|
| 0 | 0 | Counter latching operation  |
| 1 | 0 | Read/load most significant byte only.                               |
| 0 | 1 | Read/load least significant byte only.                              |
| 1 | 1 | Read/load least significant byte first, then most significant byte. |

Mode register for latching count  
A0, A1 = 11

D7 D6 D5 D4 D3 D2 D1 D0

|     |     |   |   |   |   |   |   |
|-----|-----|---|---|---|---|---|---|
| SC1 | SC0 | 0 | 0 | X | X | X | X |
|-----|-----|---|---|---|---|---|---|

- SC1, SC0 - Specify counter to be latched.
- D5, D4 - 00 designates counter latching operation.
- X - Don't care

FIGURE 2. Truth tables.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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Gate pin operations summary

| Modes | Signal status   |  |                  |
|-------|---|--|------------------|
|       | Low or going low  | Rising   | High             |
| 0     | Disables counting                                       | -  | Enables counting |
| 1     | -   | 1) Initiates counting<br>2) Resets output after next clock | -                |
| 2     | 1) Disables counting<br>2) Sets output immediately high | 1) Reloads counter<br>2) Initiates counting                | Enables counting |
| 3     | 1) Disables counting<br>2) Sets output immediately high | Initiates counting   | Enables counting |
| 4     | Disables counting                                       | -  | Enables counting |
| 5     | -   | Initiates counting   | -                |

M- Mode:

| M2 | M1 | M0 |        |
|----|----|----|--------|
| 0  | 0  | 0  | Mode 0 |
| 0  | 0  | 1  | Mode 1 |
| X  | 1  | 0  | Mode 2 |
| X  | 1  | 1  | Mode 3 |
| 1  | 0  | 0  | Mode 4 |
| 1  | 0  | 1  | Mode 5 |

BCD:

|   |   |
|---|---|
| 0 | Binary counter 16-bits                        |
| 1 | Binary code decimal (BCD) counter (4 decades) |

FIGURE 2. Truth tables - Continued.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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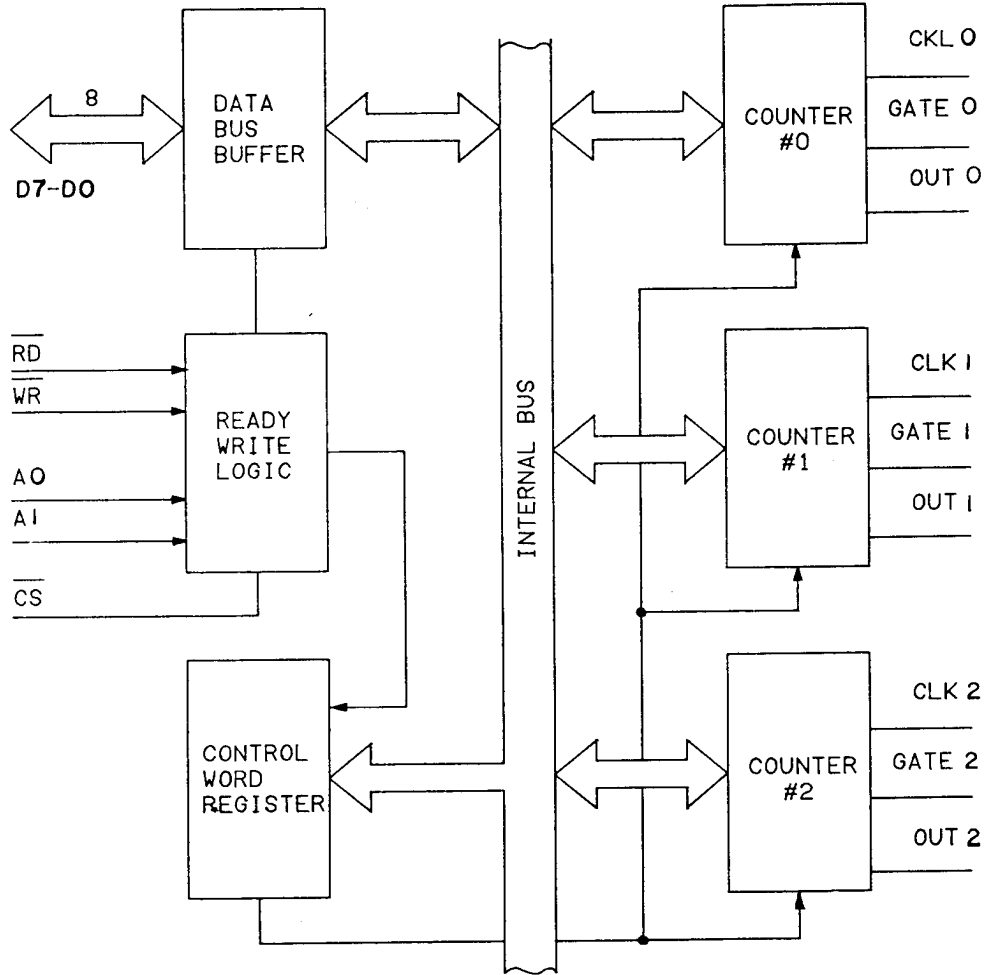


FIGURE 3. Block diagram.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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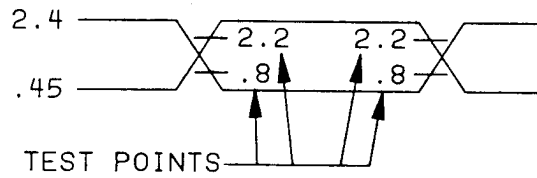


FIGURE 4. Switching test input waveform.

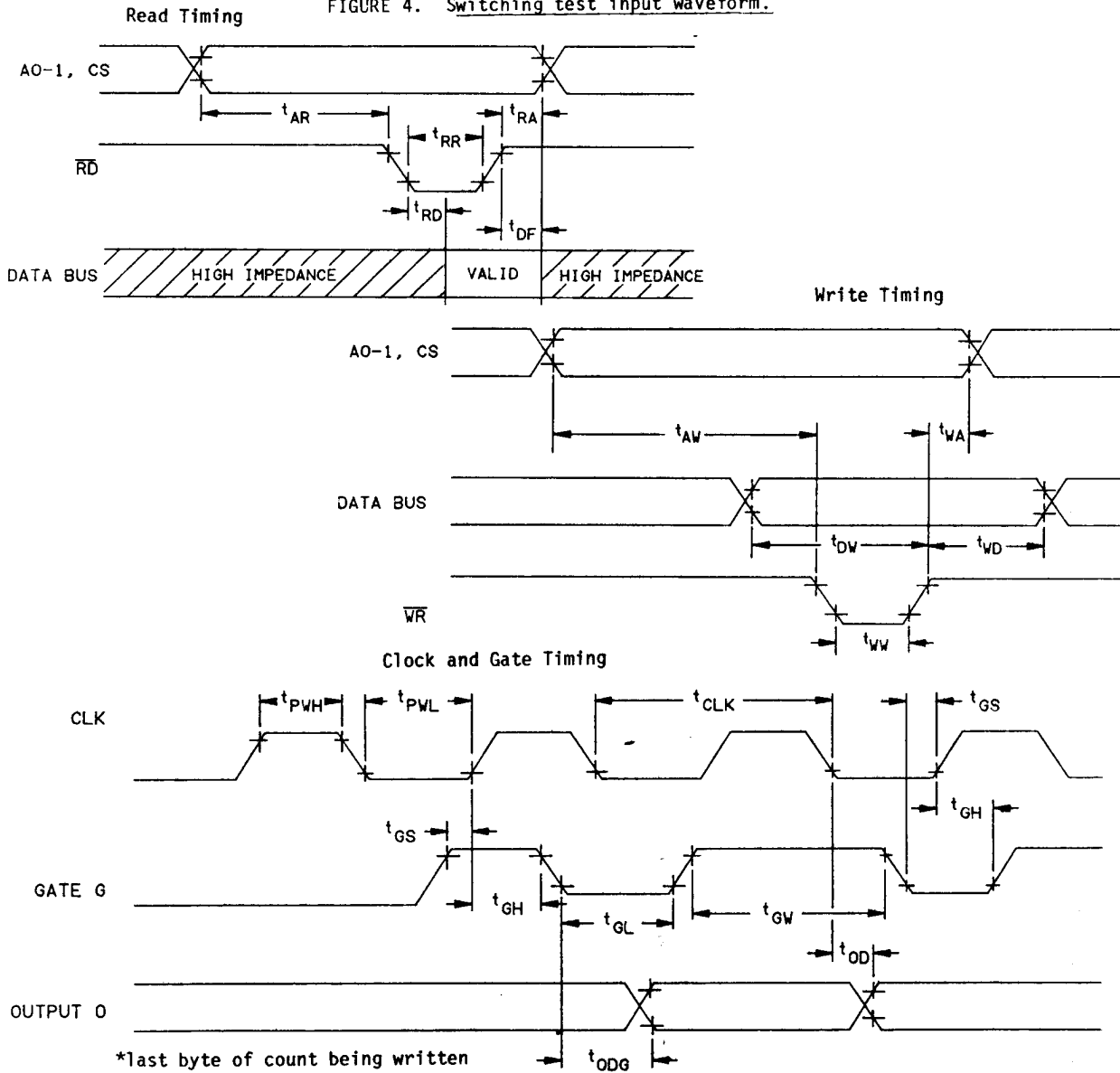


FIGURE 5. Timing waveforms.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
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4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
  - (1) Test condition D using the circuit submitted with with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 are verified by testing to the truth tables of figure 2.
- d. Subgroup 4 ( $C_{IN}$  and  $C_{I/O}$  measurements) shall be measured initially and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
  - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

|  |           |                                 |                       |
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TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements  | Subgroups<br>(per method<br>5005, table I) |
|--|--|
| Initial electrical parameters<br>(method 5004)                         | ---  |
| Final electrical test parameters<br>(method 5004)                      | 1*, 2, 3, 7,<br>8, 9, 10, and 11           |
| Group A test requirements<br>(method 5005)                             | 1*, 2, 3, 7,<br>8, 9, 10, and 11           |
| Groups C and D end-point<br>electrical parameters<br>(method 5005)     | 1, 2, 3<br>or<br>2, 8(hot), and 10         |
| Additional electrical subgroups<br>for group C periodic<br>inspections | ---  |

\* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

|  |           |                                 |                       |
|--|-----------|---------------------------------|-----------------------|
| <b>MILITARY DRAWING</b><br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO | SIZE<br>A | CODE IDENT. NO.<br><b>14933</b> | DWG NO.<br>5962-87520 |
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6.3 Pin description.

| Pin number | Name            | I/O | Description           |
|------------|-----------------|-----|-----------------------|
| 1-8        | D7-D0           | I/O | Data bus (8-bit)      |
| 9, 15, 18  | CLK N           | I   | Counter clock inputs  |
| 11, 14, 16 | GATE N          | I   | Counter gate inputs   |
| 10, 13, 17 | OUT N           | O   | Counter outputs       |
| 22         | $\overline{RD}$ | I   | Read counter          |
| 23         | $\overline{WR}$ | I   | Write command or data |
| 21         | $\overline{CS}$ | I   | Chip select           |
| 19, 20     | A0-A1           | I   | Counter select        |
| 24         | V <sub>CC</sub> |     | +5 volts              |
| 12         | GND             |     | Ground                |

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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查询"5962-8752001JA"供应商



6.5 Approved source of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

| Military drawing part number | Vendor CAGE number | Vendor similar part number <u>1/</u> | Replacement military specification part number |
|------------------------------|--------------------|--------------------------------------|--|
| 5962-8752001JX               | 34335              | 8253/BJA                             |  |
| 5962-8752002JX               | 34649              | M08253/B                             |  |
| 5962-8752003JX               | 34335              | 8253-5/BJA                           |  |

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

34335

Advanced Micro Devices, Inc.  
901 Thompson Place  
P.O. Box 3453  
Sunnyvale, CA 94088

34649

Intel Corporation  
5000 W Williams Field Road  
Chandler, AZ 85224

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