HAT3018R, HAT3018RJ

Silicon N/P Channel Power MOS FET
High Speed Power Switching

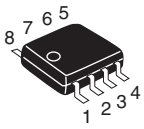
REJ03G0127-0100Z
Rev.1.00
Oct.20.2003

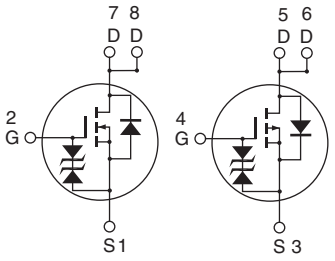
Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- "J" is for Automotive application
  High temperature D-S leakage guarantee
  Avalanche rating

Outline

SOP-8





1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings				Unit
		HAT3018R		HAT3018RJ		
		Nch	Pch	Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	±20	±20	V
Drain current	I_D	6	–5	6	–5	A
Drain peak current	I_D (pulse)[Note1]	48	–40	48	–40	A
Avalanche current	I_{AP}[Note4]	—	—	6	–5	A
Avalanche energy	E_{AR}[Note4]	—	—	3.08	2.14	mJ
Channel dissipation	Pch[Note2]	2	2	2	2	W
Channel dissipation	Pch[Note3]	3	3	3	3	W
Channel temperature	Tch	150	150	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10µs, duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
3. 2 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

• **N Channel**

(Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to Source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current		I_{DSS}	—	—	1	µA	V_{DS} = 60 V, V_{GS} = 0
Zero gate voltage drain current	HAT3018R	I_{DSS}	—	—	—	µA	V_{DS} = 48 V, V_{GS} = 0
	HAT3018RJ	I_{DSS}	—	—	10	µA	Ta = 125°C
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	1.5	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance		$\|y_{fs}\|$	6	9.5	—	S	I_D = 3 A[Note 5], V_{DS} = 10 V
Static drain to source on state resistance		$R_{DS(on)}$	—	28	35	mΩ	I_D = 3 A[Note 5], V_{GS} = 10 V
		$R_{DS(on)}$	—	40	50	mΩ	I_D = 3 A[Note 5], V_{GS} = 4.5 V
Input capacitance		Ciss	—	1000	—	pF	V_{DS} = 10 V, V_{GS} = 0
Output capacitance		Coss	—	145	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	85	—	pF	
Total gate charge		Qg	—	15	—	nC	V_{DD} = 25 V
Gate to source charge		Qgs	—	2	—	nC	V_{GS} = 10 V
Gate to drain charge		Qgd	—	3	—	nC	I_D = 6 A
Turn-on delay time		td(on)	—	12	—	ns	V_{GS} = 10 V, I_D= 3 A
Rise time		tr	—	10	—	ns	V_{DD} ≅ 30 V
Turn-off delay time		td(off)	—	60	—	ns	R_L = 10 Ω
Fall time		tf	—	11	—	ns	R_G = 4.7 Ω
Body-drain diode forward voltage		V_{DF}	—	0.82	1.07	V	I_F = 6 A, V_{GS} = 0[Note 5]
Body-drain diode reverse recovery time		trr	—	40	—	ns	I_F = 6 A, V_{GS} = 0 diF/dt = 100A/ µs

Notes: 5. Pulse test

● **P Channel**

(Ta = 25°C)

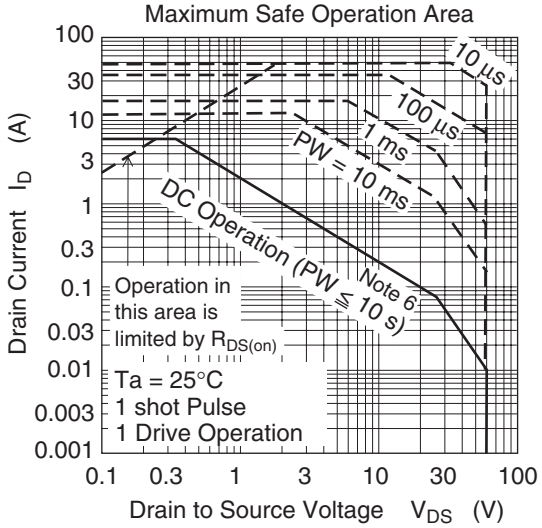
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to Source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current		I_{DSS}	—	—	–1	µA	V_{DS} = –60 V, V_{GS} = 0
Zero gate voltage drain current	HAT3018R	I_{DSS}	—	—	—	µA	V_{DS} = –48 V, V_{GS} = 0
	HAT3018RJ	I_{DSS}	—	—	–10	µA	Ta = 125°C
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = 1 mA
Forward transfer admittance		$\|y_{fs}\|$	3	5	—	S	I_D = –2.5 A[Note 5], V_{DS} = –10 V
Static drain to source on state resistance		$R_{DS(on)}$	—	60	76	mΩ	I_D = –2.5 A[Note 5], V_{GS} = –10 V
		$R_{DS(on)}$	—	90	130	mΩ	I_D = –2.5 A[Note 5], V_{GS} = –4.5V
Input capacitance		Ciss	—	1350	—	pF	V_{DS} = –10 V, V_{GS} = 0
Output capacitance		Coss	—	135	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	85	—	pF	
Total gate charge		Qg	—	21	—	nC	V_{DD} = –25 V
Gate to source charge		Qgs	—	3	—	nC	V_{GS} = –10 V
Gate to drain charge		Qgd	—	4	—	nC	I_D = –5 A
Turn-on delay time		td(on)	—	20	—	ns	V_{GS} = –10 V, I_D= –2.5 A
Rise time		tr	—	15	—	ns	V_{DD} ≅ –30 V
Turn-off delay time		td(off)	—	55	—	ns	R_L = 12 Ω
Fall time		tf	—	10	—	ns	R_G = 4.7 Ω
Body-drain diode forward voltage		V_{DF}	—	–0.85	–1.10	V	I_F = –5 A, V_{GS} = 0[Note 5]
Body-drain diode reverse recovery time		trr	—	25	—	ns	I_F = –5 A, V_{GS} = 0 diF/dt = 100A/ µs

Notes: 5. Pulse test

Main Characteristics

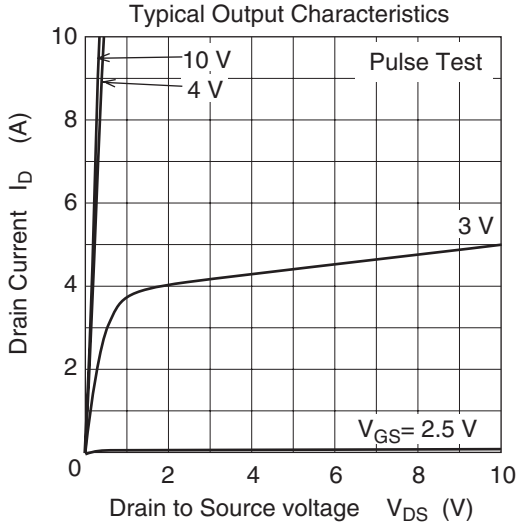
• **N Channel**

Maximum Safe Operation Area

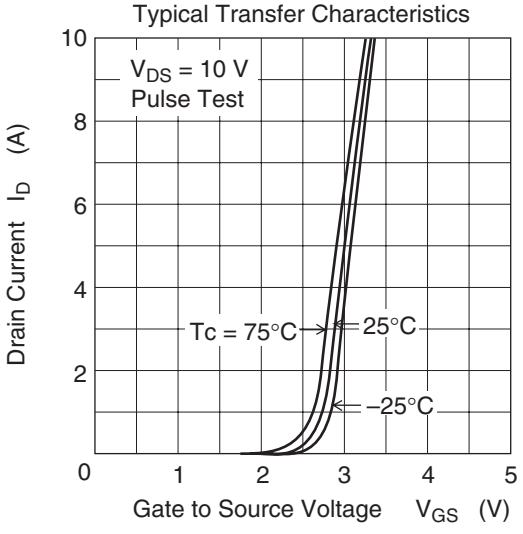


Note 6: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

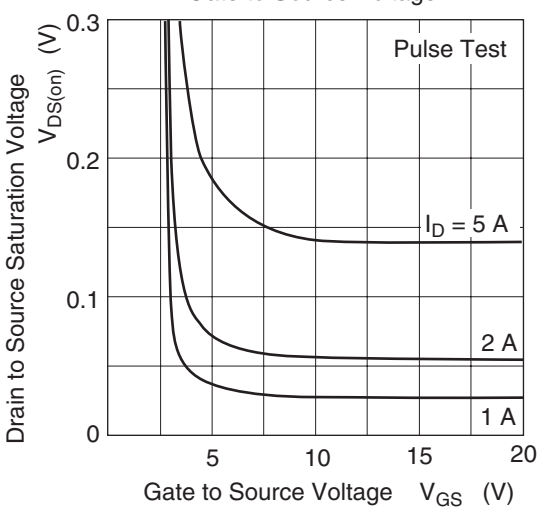
Typical Output Characteristics



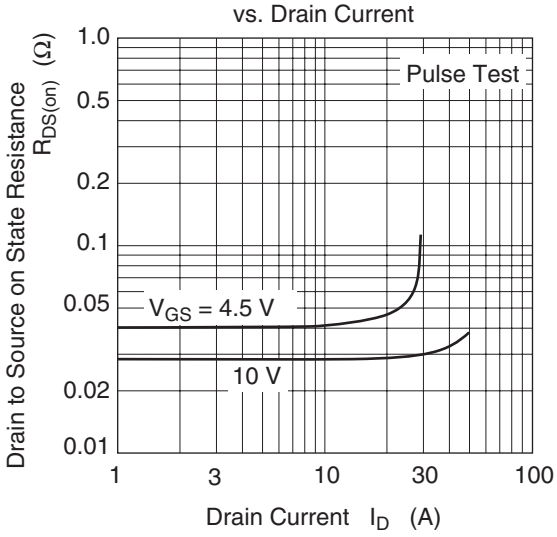
Typical Transfer Characteristics



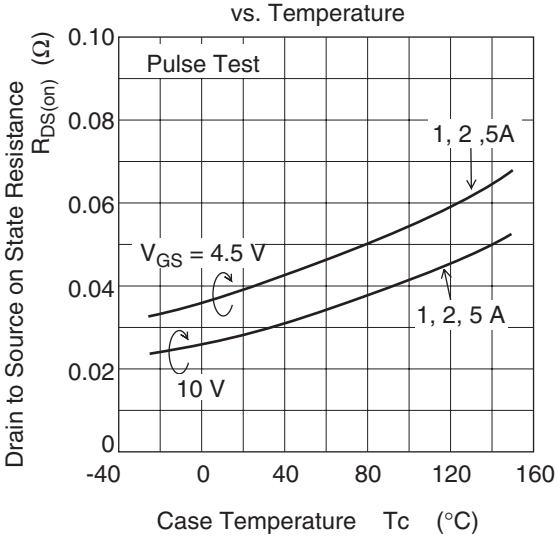
Drain to Source Saturation Voltage vs. Gate to Source Voltage



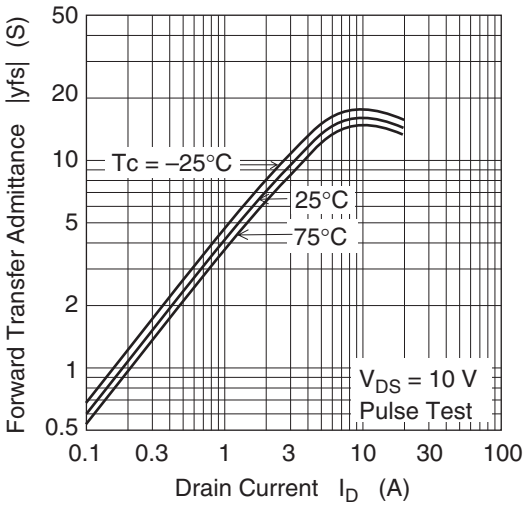
Static Drain to Source on State Resistance vs. Drain Current



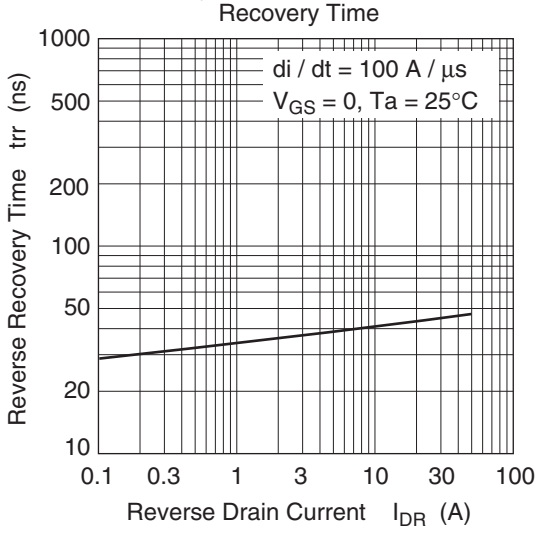
Static Drain to Source on State Resistance vs. Temperature



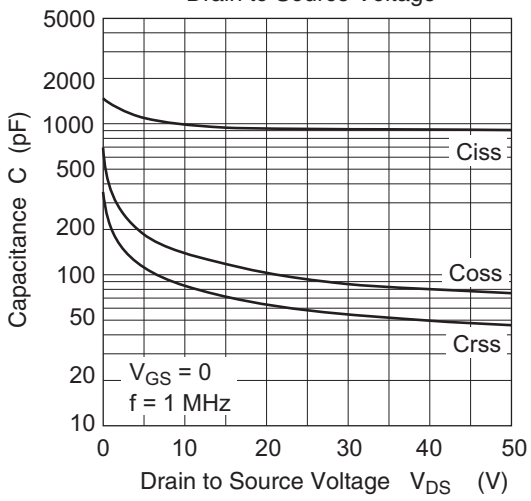
Forward Transfer Admittance vs. Drain Current



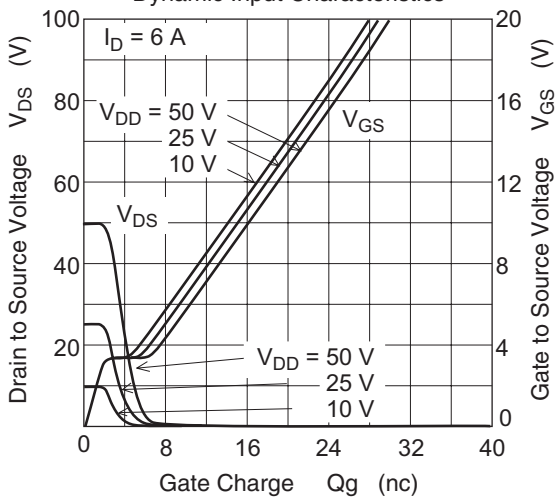
Body-Drain Diode Reverse Recovery Time



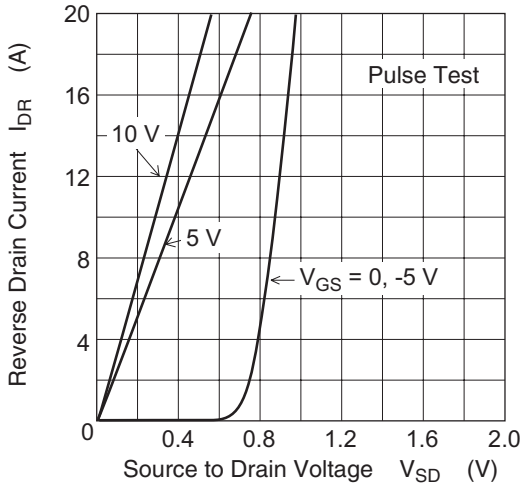
Typical Capacitance vs.
Drain to Source Voltage



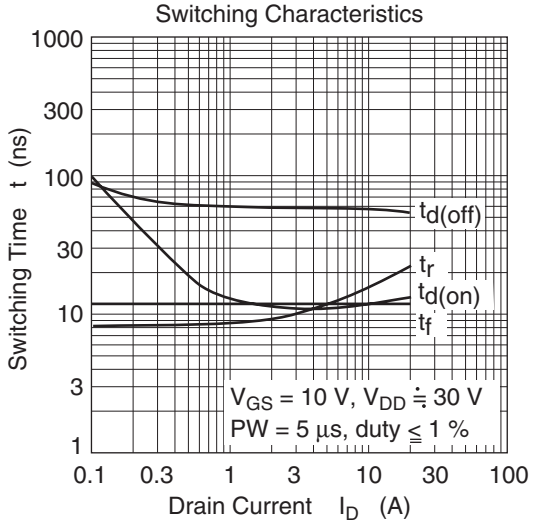
Dynamic Input Characteristics



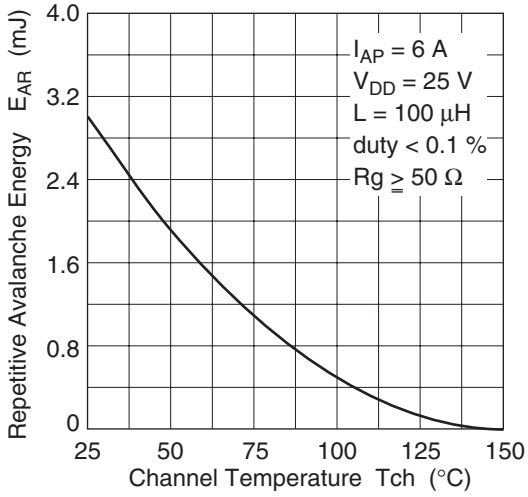
Reverse Drain Current vs.
Source to Drain Voltage



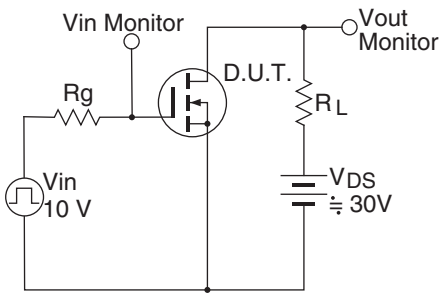
Switching Characteristics



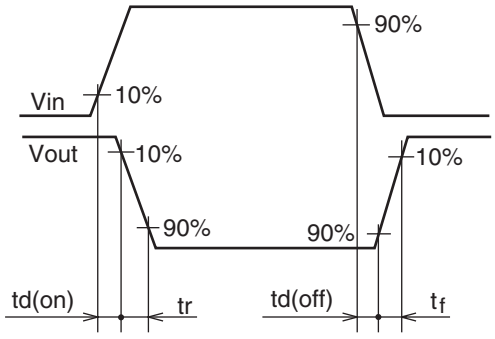
Maximum Avalanche Energy vs. Channel Temperature Derating



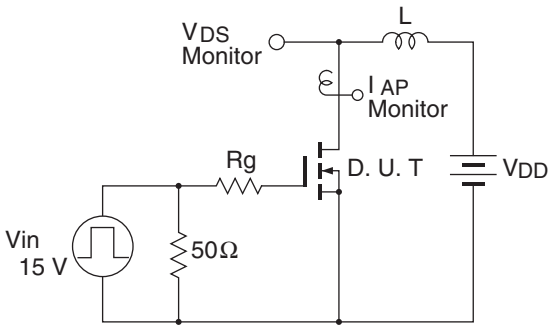
Switching Time Test Circuit



Switching Time Waveform

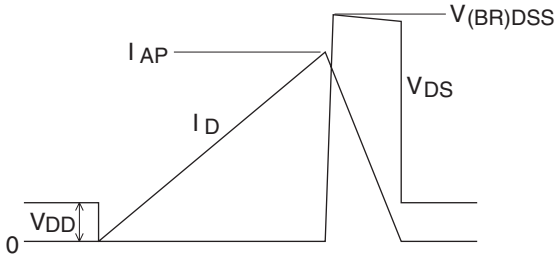


Avalanche Test Circuit

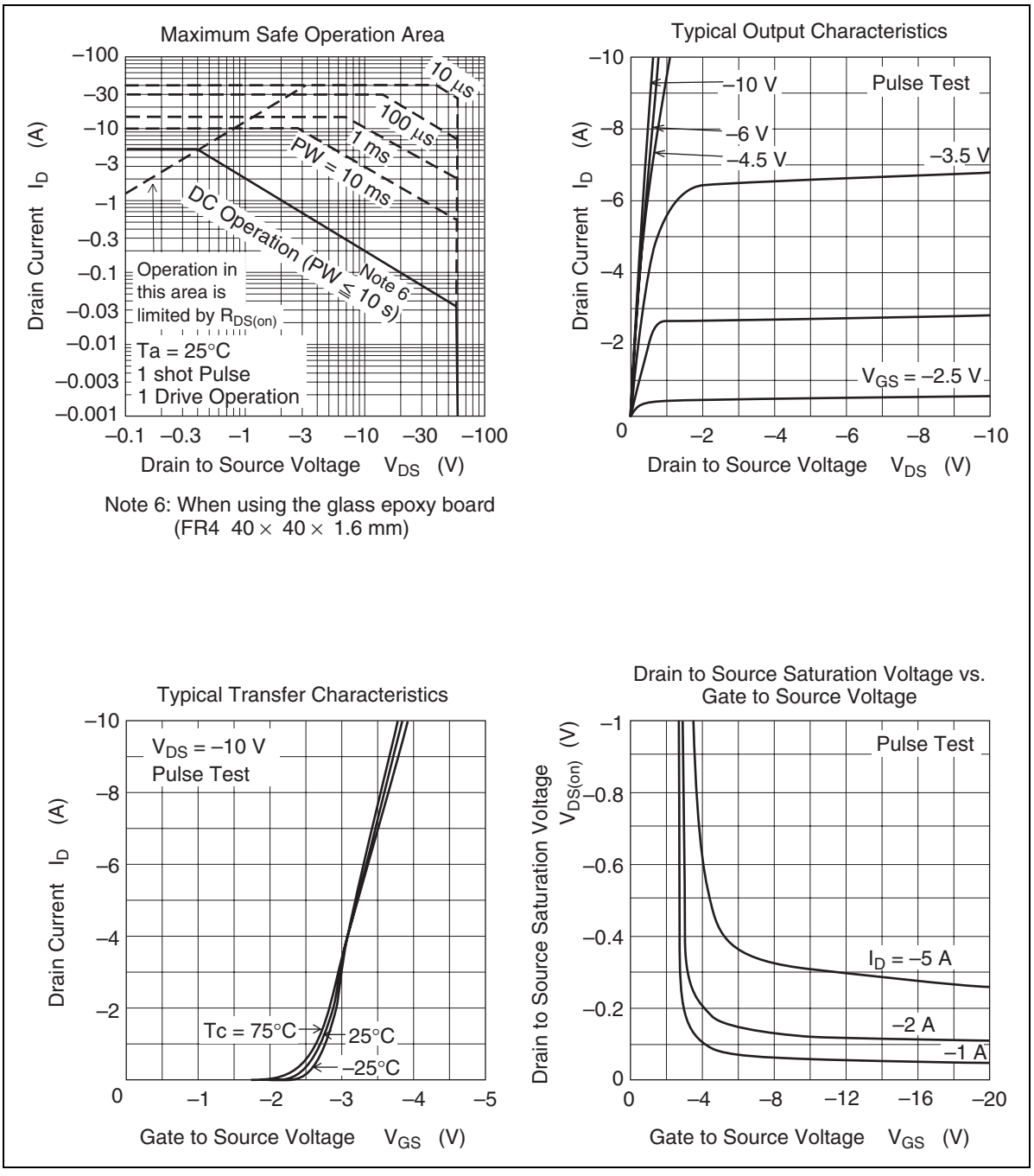


Avalanche Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

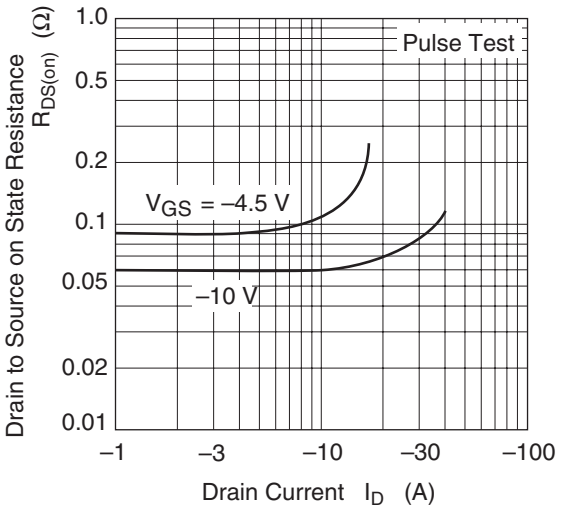


• **P Channel**

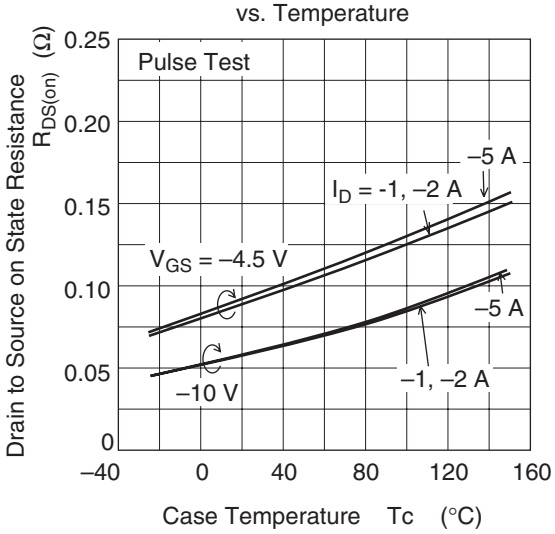


Note 6: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

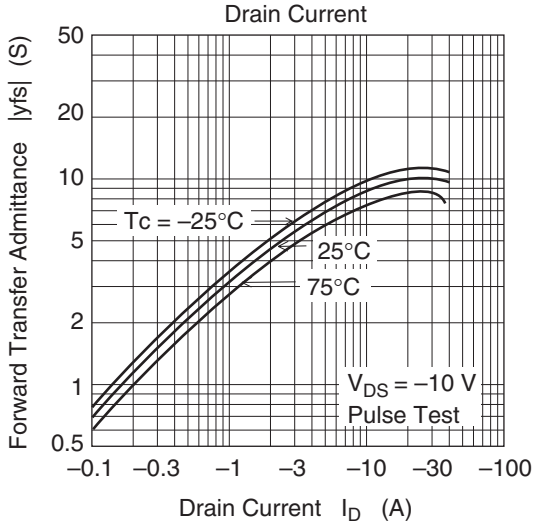
Static Drain to Source on State Resistance vs. Drain Current



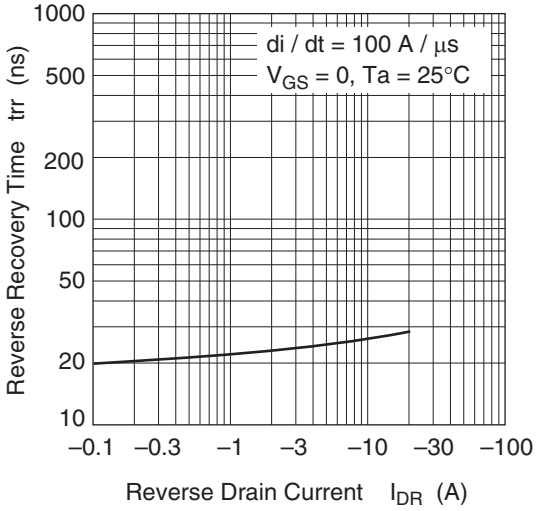
Static Drain to Source on State Resistance vs. Temperature



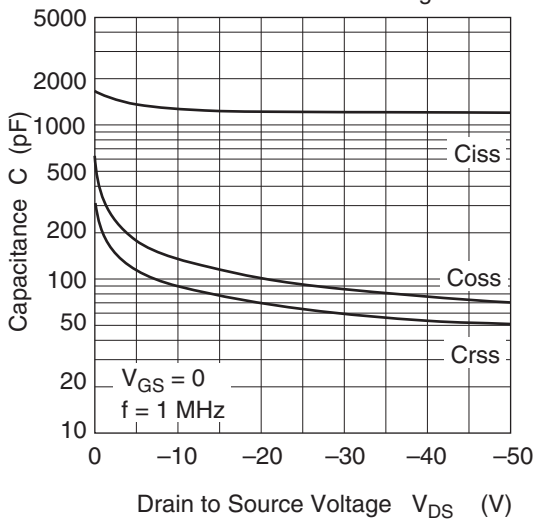
Forward Transfer Admittance vs. Drain Current



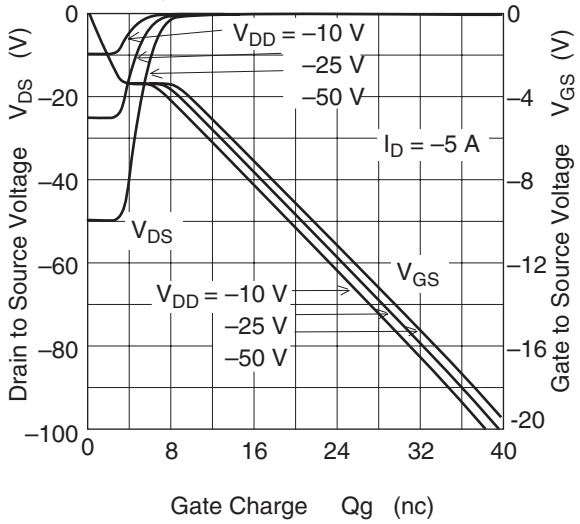
Body-Drain Diode Reverse Recovery Time



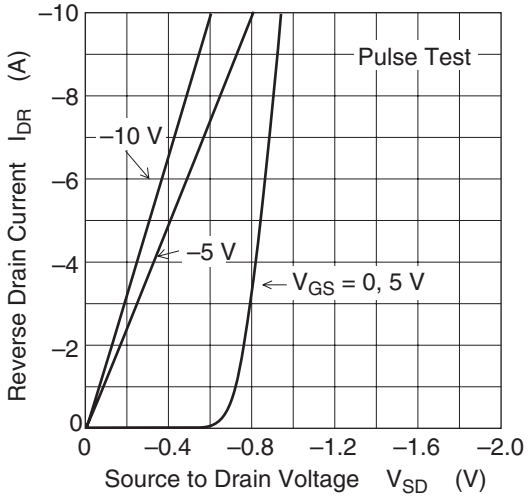
Typical Capacitance vs.
Drain to Source Voltage



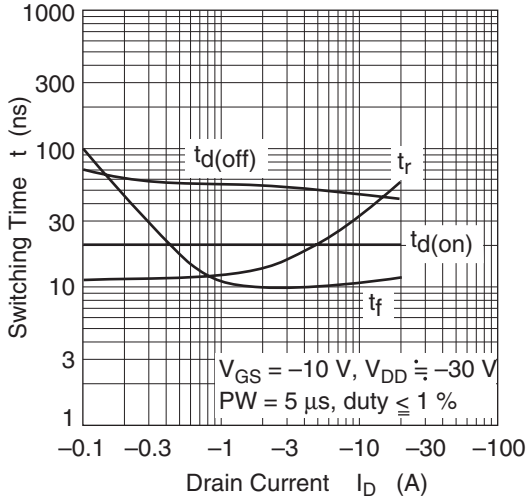
Dynamic Input Characteristics



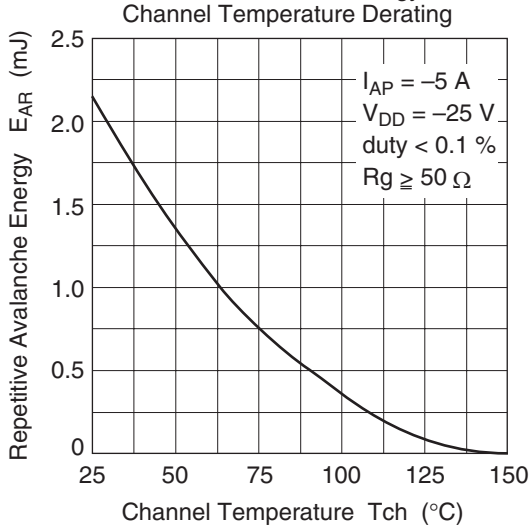
Reverse Drain Current vs.
Source to Drain Voltage



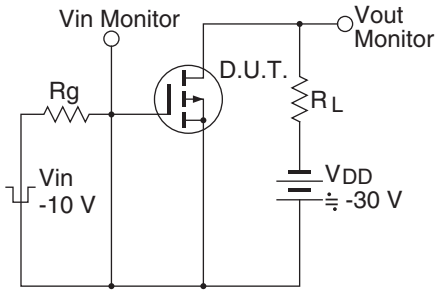
Switching Characteristics



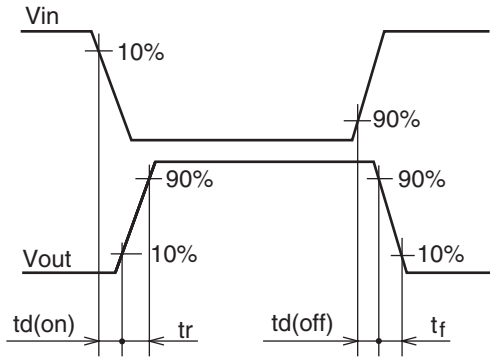
Maximum Avalanche Energy vs. Channel Temperature Derating



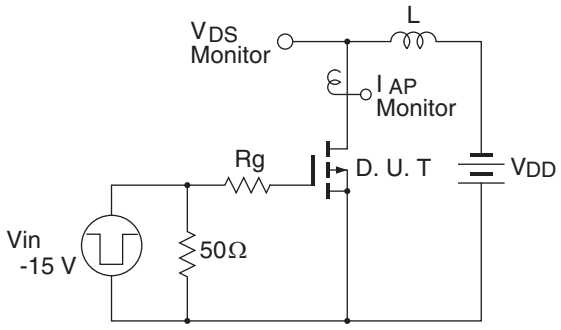
Switching Time Test Circuit



Switching Time Waveform

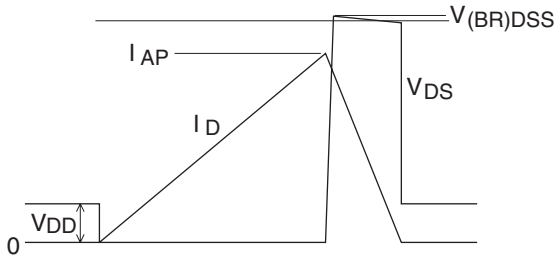


Avalanche Test Circuit

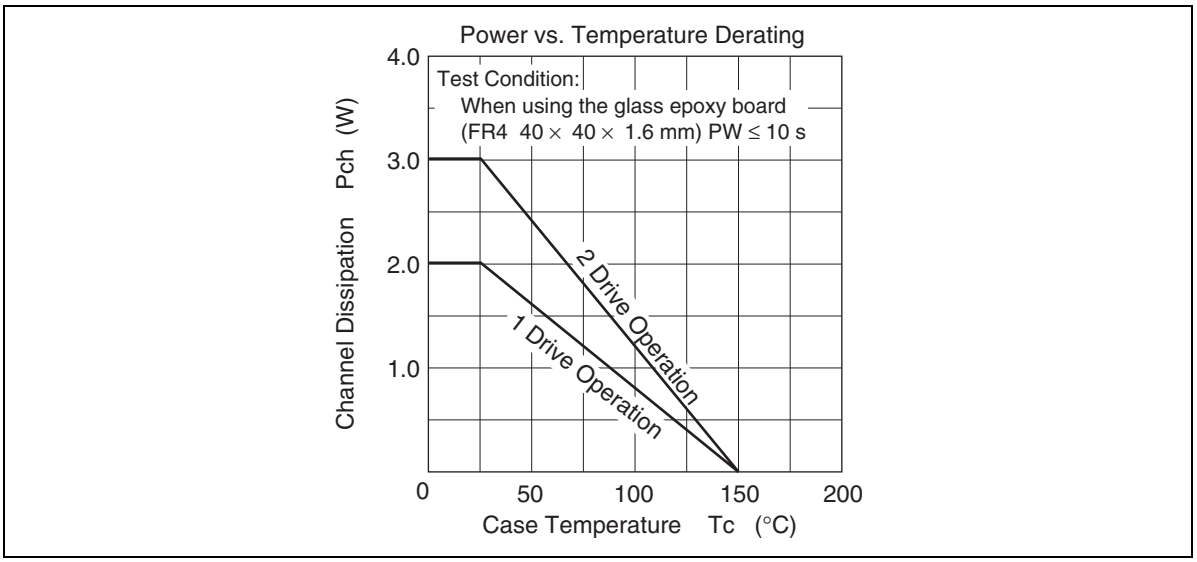


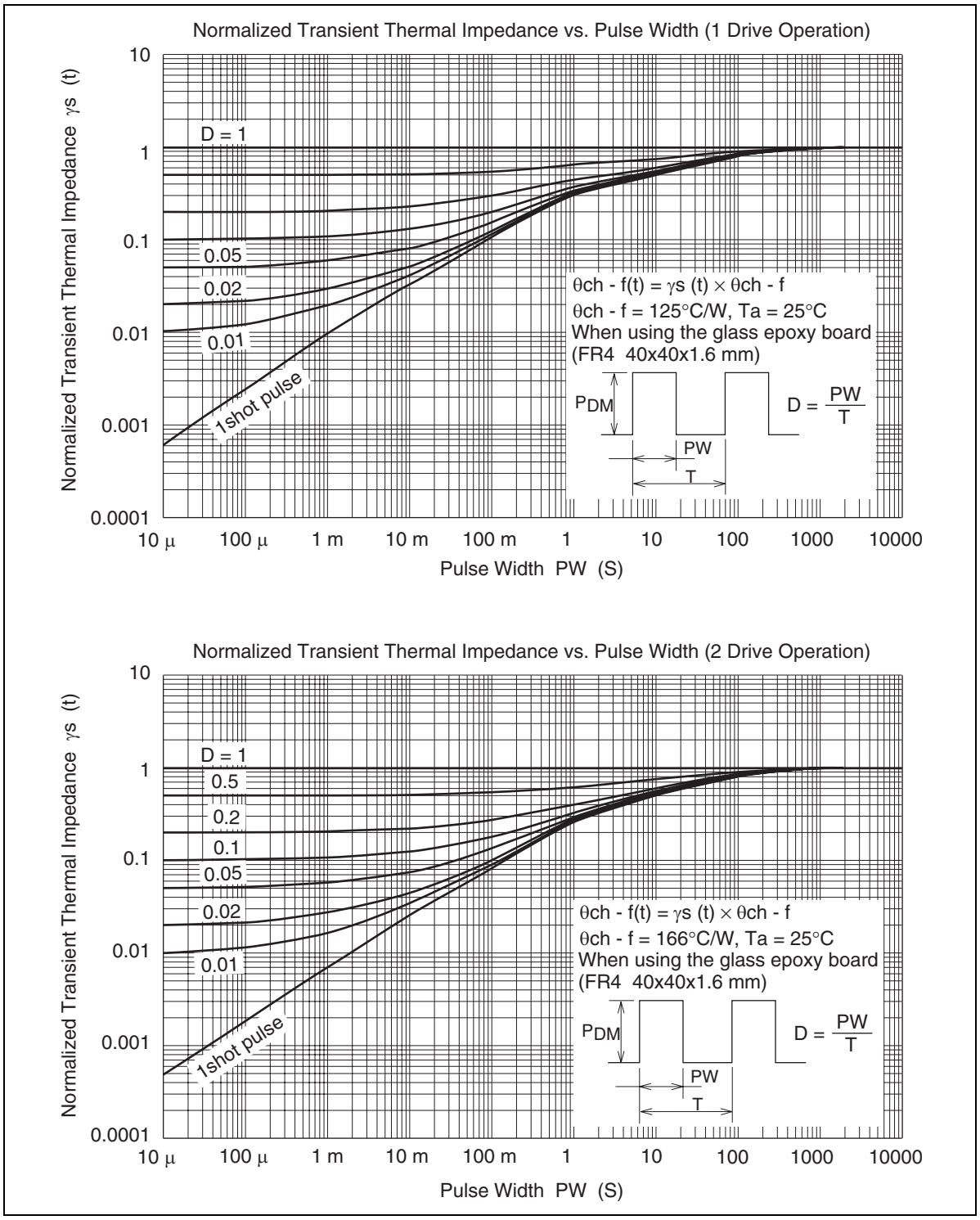
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



● **In common**

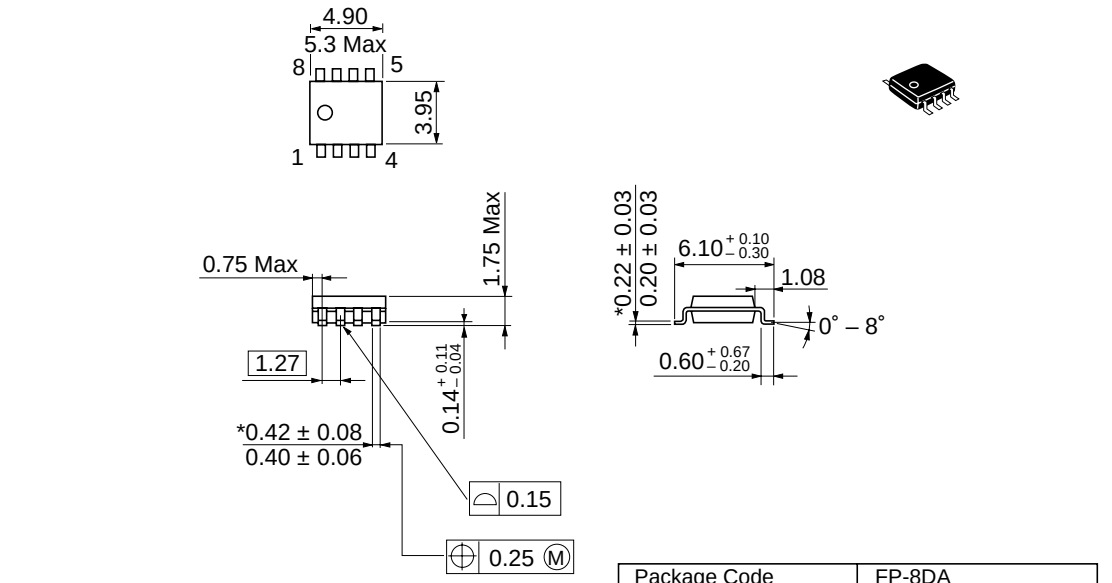

Power vs. Temperature Derating
Test Condition:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm) PW ≤ 10 s
Channel Dissipation Pch (W)
4.0
3.0
2.0
1.0
0
50
100
150
200
Case Temperature Tc (°C)
2 Drive Operation
1 Drive Operation


Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) × θch - f
θch - f = 125°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
D = PW/T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)
Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) × θch - f
θch - f = 166°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
D = PW/T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

Package Dimensions

As of January, 2003

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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