



November 1988  
Revised August 2000

## 74AC273 • 74ACT273 Octal D-Type Flip-Flop

### General Description

The AC273 and ACT273 have eight edge-triggered D-type flip-flops with individual D-type inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D-type input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

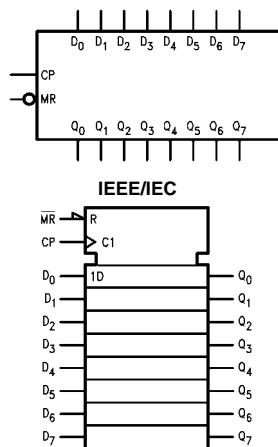
- Ideal buffer for microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See 377 for clock enable version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- Outputs source/sink 24 mA
- 74ACT273 has TTL-compatible inputs

### Ordering Code:

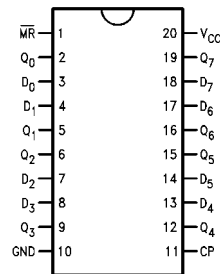
Order Number	Package Number	Package Description
74AC273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74AC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



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### Pin Descriptions

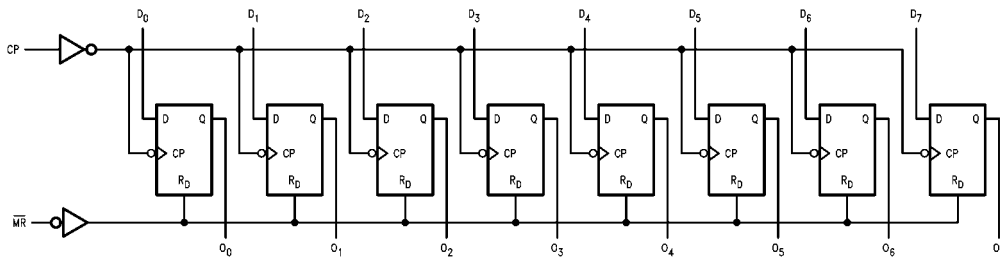
Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
$\overline{\text{MR}}$	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

### Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{\text{MR}}$	CP	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↗	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	AC 2.0V to 6.0V
DC Input Diode Current ( $I_{IK}$ )		ACT 4.5V to 5.5V	
$V_I = -0.5V$	-20 mA	Input Voltage ( $V_I$ )	0V to $V_{CC}$
$V_I = V_{CC} + 0.5V$	+20 mA	Output Voltage ( $V_O$ )	0V to $V_{CC}$
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Diode Current ( $I_{OK}$ )		Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_O = -0.5V$	-20 mA	AC Devices	
$V_O = V_{CC} + 0.5V$	+20 mA	$V_{IN}$ from 30% to 70% of $V_{CC}$	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$	$V_{CC}$ @ 3.3V, 4.5V, 5.5V for AC	125 mV/ns
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA	ACT Devices	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	$V_{IN}$ from 0.8V to 2.0V	
Junction Temperature ( $T_J$ ) (PDIP)	140°C	$V_{CC}$ @ 4.5V, 5.5V for ACT	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

### DC Electrical Characteristics for AC

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions	
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
			4.5		3.86	3.76		
			5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
			4.5		0.36	0.44		
			5.5		0.36	0.44		
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OLD}$	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Maximum Quiescent Supply Current	5.5		4.0	40.0	mA	$V_{OHD} = 3.85V$ Min	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.  
**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.  
**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

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AC Electrical Characteristics for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3	90	125		75	MHz	
		5.0	140	175		125		
t <sub>PLH</sub>	Propagation Delay Clock to Output	3.3	4.0	7.0	12.5	3.0	14.0	ns
		5.0	3.0	5.5	9.0	2.5	10.0	
t <sub>PHL</sub>	Propagation Delay Clock to Output	3.3	4.0	7.0	13.0	3.5	14.5	ns
		5.0	3.0	5.0	10.0	2.5	11.0	
t <sub>PHL</sub>	Propagation Delay MR to Output	3.3	4.0	7.0	13.0	3.5	14.0	ns
		5.0	3.0	5.0	10.0	2.5	10.5	

Note 5: Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC							
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW Data to CP	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		
t <sub>H</sub>	Hold Time, HIGH or LOW Data to CP	3.3	-2.0	0	0		ns
		5.0	-1.0	1.0	1.0		
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		
t <sub>W</sub>	MR Pulse Width HIGH or LOW	3.3	2.0	5.5	6.0		ns
		5.0	1.5	4.0	4.5		
t <sub>rec</sub>	Recovery Time MR to CP	3.3	1.5	3.5	4.5		ns
		5.0	1.0	2.0	3.0		

Note 6: Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0		2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0		2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8		0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8		0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4		4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4		5.4		
		4.5		3.86		3.76		
		5.5		4.86		4.76		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 7)
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1		0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1		0.1		
		4.5		0.36		0.44		
		5.5		0.36		0.44		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 7)
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1		±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6			1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic	5.5				75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 8)	5.5				-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
<p><b>Note 7:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 8:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p>								
AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	2.0	125	189		110		MHz
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	5.0	1.5	6.5	8.5	1.5	9.0	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	5.0	1.5	7.0	9.0	1.5	8.5	ns
<p><b>Note 9:</b> Voltage Range 5.0 is 5.0V ± 0.5V</p>								

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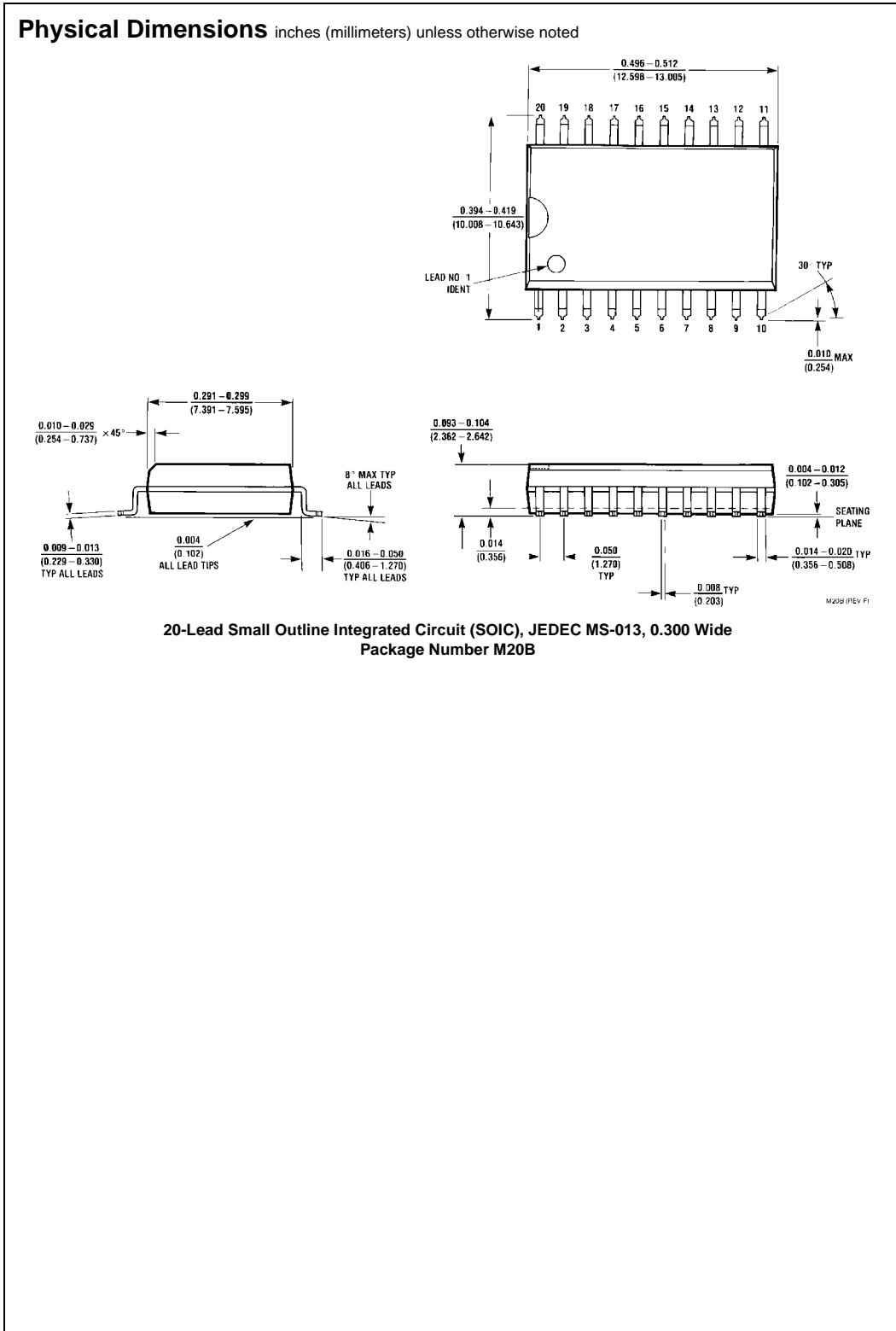
**AC Operating Requirements for ACT**

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.0	3.5	3.5	ns	
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	-0.5	1.5	1.5	ns	
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	5.0	2.0	4.0	4.0	ns	
t <sub>W</sub>	$\overline{\text{MR}}$ Pulse Width HIGH or LOW	5.0	1.5	4.0	4.0	ns	
t <sub>W</sub>	Recovery Time $\overline{\text{MR}}$ to CP	5.0	0.5	3.0	3.0	ns	

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

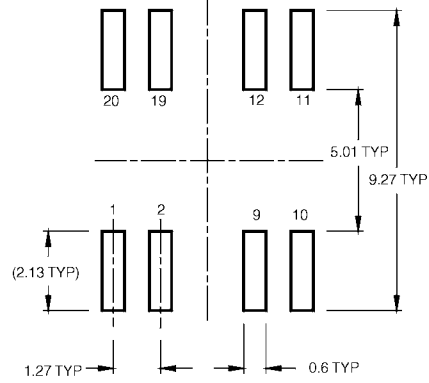
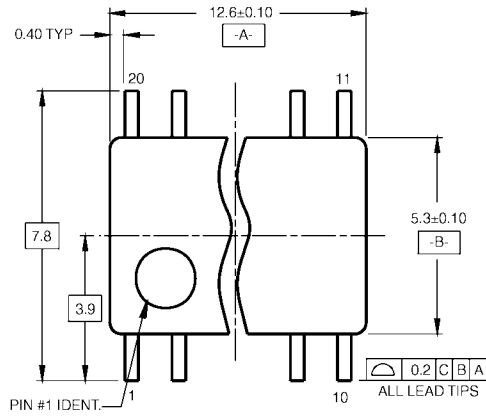
**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance for AC Power Dissipation Capacitance for ACT	50.0 40.0	pF	V <sub>CC</sub> = 5.0V

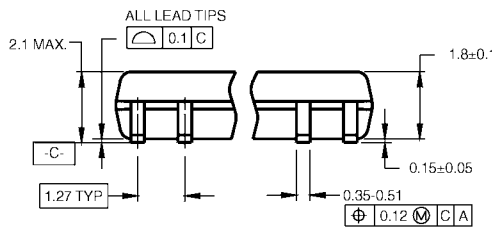


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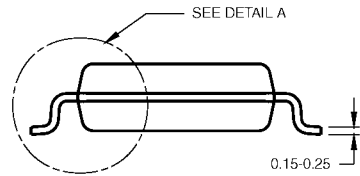
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



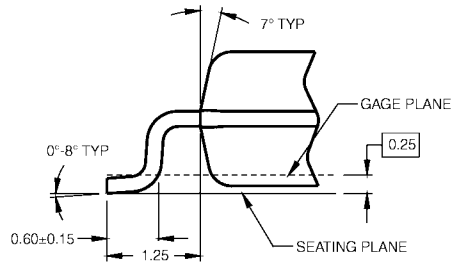
DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

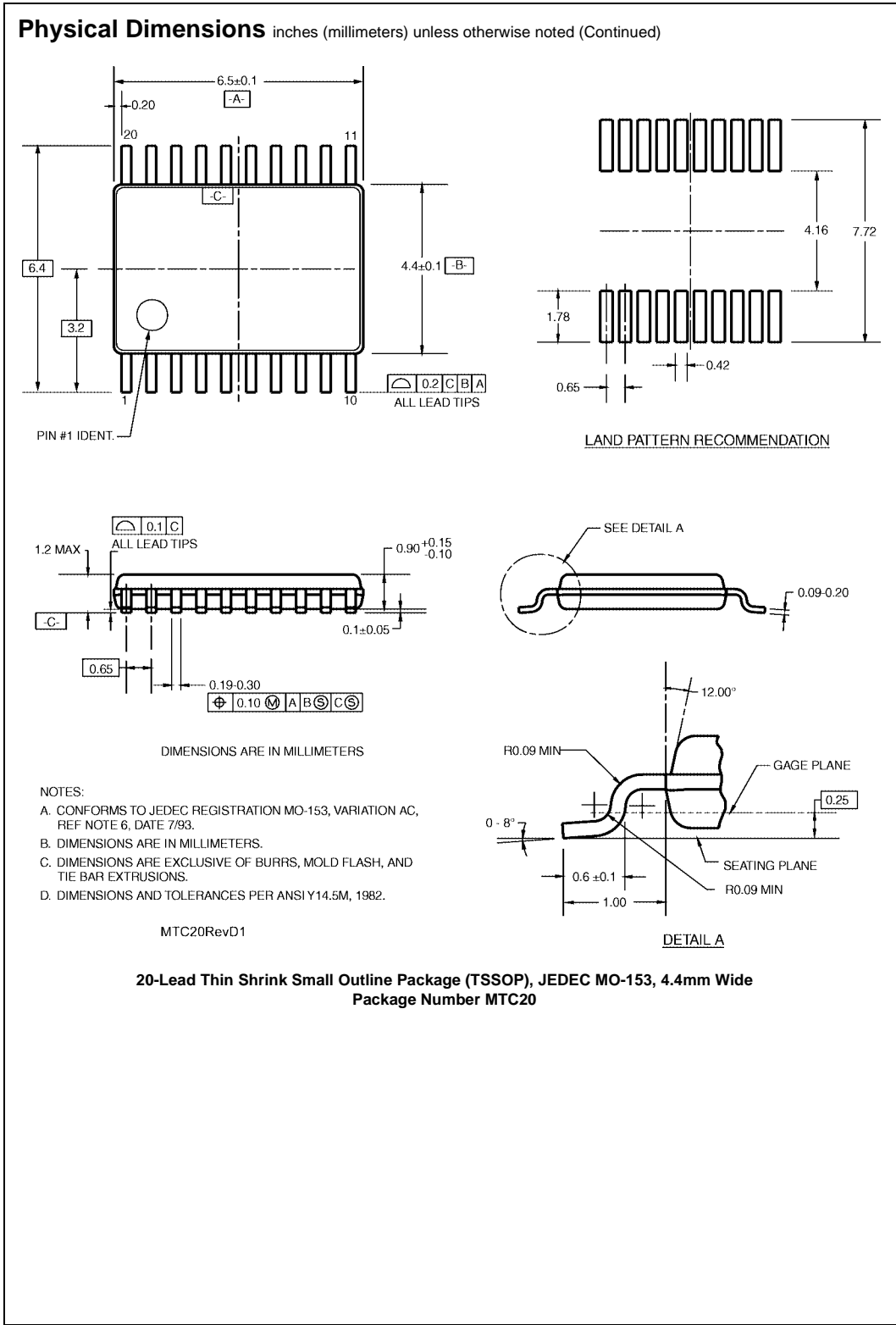
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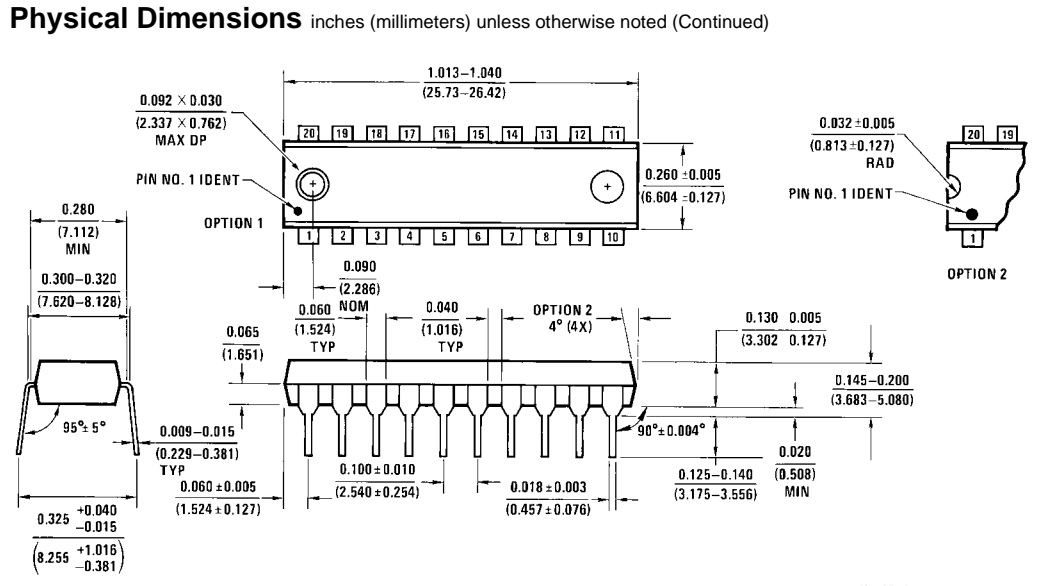
DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**





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20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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