

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments (TI) Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture**
- **Extends Scan Access From Board Level to Higher Levels of System Integration**
- **Promotes Reuse of Lower-Level (Chip/Board) Tests in System Environment**
- **While Powered at 3.3 V, Both the Primary and Secondary TAPs Are Fully 5-V Tolerant for Interfacing to 5-V and/or 3.3-V Masters and Targets**
- **Switch-Based Architecture Allows Direct Connect of Primary TAP to Secondary TAP**
- **Primary TAP Is Multidrop for Minimal Use of Backplane Wiring Channels**
- **Shadow Protocols Can Occur in Any of Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR TAP States to Provide for Board-to-Board Test and Built-In Self-Test**
- **Simple Addressing (Shadow) Protocol Is Received/Acknowledged on Primary TAP**
- **10-Bit Address Space Provides for up to 1021 User-Specified Board Addresses**
- **Bypass ($\overline{\text{BYP}}$) Pin Forces Primary-to-Secondary Connection Without Use of Shadow Protocols**
- **Connect ($\overline{\text{CON}}$) Pin Provides Indication of Primary-to-Secondary Connection**
- **High-Drive Outputs ($-32\text{-mA } I_{\text{OH}}$, $64\text{-mA } I_{\text{OL}}$) Support Backplane Interface at Primary and High Fanout at Secondary**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

PW PACKAGE
(TOP VIEW)

A4	1	24	A5
A3	2	23	A6
A2	3	22	A7
A1	4	21	A8
A0	5	20	A9
$\overline{\text{BYP}}$	6	19	V_{CC}
GND	7	18	$\overline{\text{CON}}$
PTDO	8	17	STDI
PTCK	9	16	STCK
PTMS	10	15	STMS
PTDI	11	14	STDO
PTRST	12	13	STRST

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74LVT8996 10-bit addressable scan port (ASP) is a member of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most SCOPE™ devices, the ASP is not a boundary-scannable device, rather, it applies TI's addressable-shadow-port technology to the IEEE Std 1149.1-1990 (JTAG) test access port (TAP) to extend scan access beyond the board level.

This device is functionally equivalent to the 'ABT8996 ASPs. Additionally, it is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to interface to 5-V masters and/or targets.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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† Package drawings standard

description (continued)

Alternatively, primary-to-secondary connection can be selected by assertion of a low level at the bypass ($\overline{\text{BYP}}$) input. This operation is asynchronous to PTCK and is independent of $\overline{\text{PTRST}}$ and/or power-up reset. This bypassing feature is especially useful in the board-test environment, since it allows the board-level automated test equipment (ATE) to treat the ASP as a simple transceiver. When the $\overline{\text{BYP}}$ input is high, the ASP is free to respond to shadow protocols. Otherwise, when $\overline{\text{BYP}}$ is low, shadow protocols are ignored.

Whether the connected status is achieved by use of shadow protocol or by use of $\overline{\text{BYP}}$, this status is indicated by a low level at the connect (CON) output. Likewise, when the secondary TAP is disconnected from the primary TAP, the CON output is high.

FUNCTION TABLE

INPUTS		SHADOW-PROTOCOL RESULT†	OUTPUTS						PRIMARY-TO-SECONDARY CONNECT STATUS
$\overline{\text{BYP}}$	$\overline{\text{PTRST}}$		$\overline{\text{STRST}}$	STCK	STMS	STDO	PTDO	$\overline{\text{CON}}$	
L	L	—	L	PTCK	H‡	PTDI	STDI	L	BYP/TRST‡
L	H	—	H	PTCK	PTMS	PTDI	STDI	L	BYP
H	L	—	L	PTCK	H	Z	Z	H	TRST
H	H	RESET	H	PTCK	H	Z	Z	H	RESET
H	H	MATCH	H	PTCK	PTMS	PTDI	STDI	L	ON
H	H	NO MATCH	H	PTCK	STMS₀§	Z	Z	H	OFF
H	H	HARD ERROR¶	H	PTCK	STMS₀§	Z	Z	H	OFF
H	H	DISCONNECT	H	PTCK	STMS₀§	Z	Z	H	OFF
H	H	TEST SYNCHRONIZATION	H	PTCK	PTMS	PTDI	Z	L	MULTICAST

† Shadow protocols are received serially via PTCK and PTDI and acknowledged serially via PTCK and PTDO under certain conditions in which PTMS is static low or static high (see shadow protocol). The result shown here follows any required acknowledgment.

‡ In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of $\overline{\text{TRST}}$. The BYP/TRST connect status ensures that this condition is met at STMS regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of 5 PTCK cycles following assertion of $\overline{\text{PTRST}}$, either by maintaining $\overline{\text{PTRST}}$ low or by setting PTMS high. This ensures that ICs both with and without $\overline{\text{TRST}}$ inputs are moved to their Test-Logic-Reset TAP states. It is expected that in normal application, this condition occurs only when $\overline{\text{BYP}}$ is fixed at the low state. In such case, upon release of $\overline{\text{PTRST}}$, the ASP immediately resumes the BYP connect status.

§ STMS level before indicated steady-state conditions were established

¶ The shadow protocol is well defined. Some variations in the protocol are tolerated (see protocol errors). Those that are not tolerated produce protocol result HARD ERROR and cause disconnect as indicated.

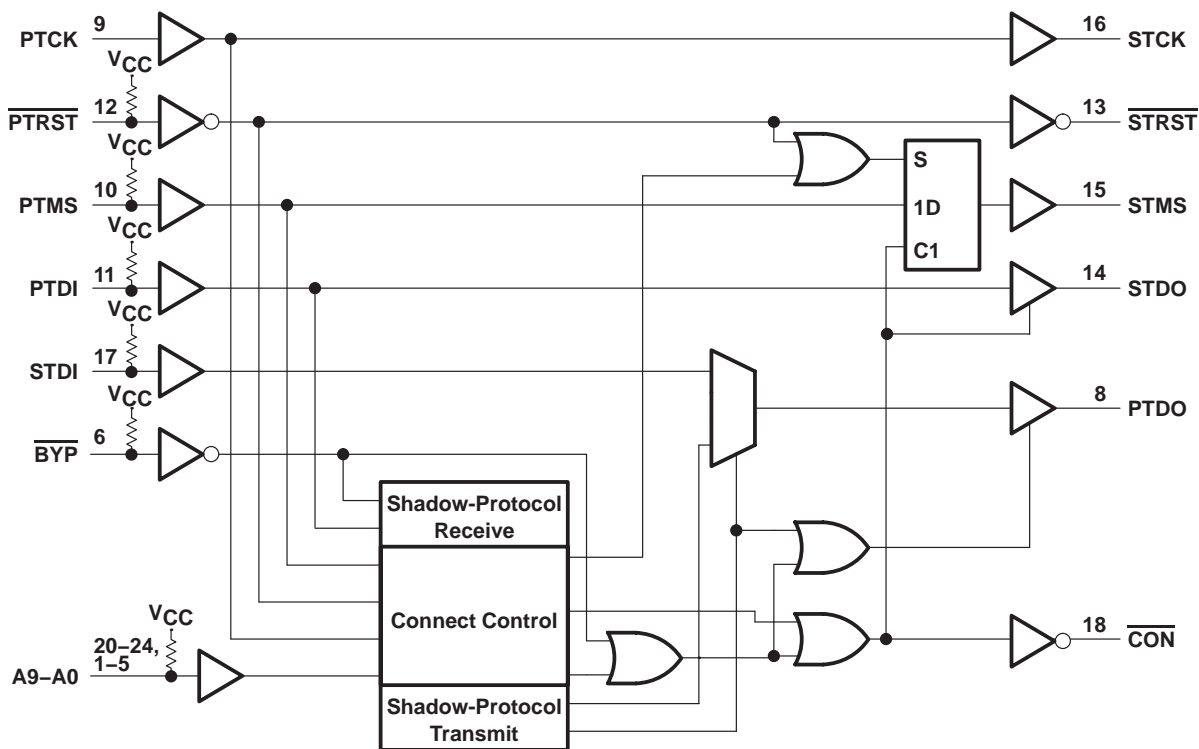
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3.3-V 10-BIT ADDRESSABLE SCAN PORT

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functional block diagram



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Terminal Functions

TERMINAL NAME	DESCRIPTION
A9–A0	Address inputs. The ASP compares addresses received via shadow protocol against the value at A9–A0 to determine address match. The bit order is from most significant to least significant. An internal pullup at each A9–A0 terminal forces the terminal to a high level if it has no external connection.
$\overline{\text{BYP}}$	Bypass input. A low input at $\overline{\text{BYP}}$ forces the ASP into $\overline{\text{BYP}}$ or $\overline{\text{BYP/TRST}}$ status, depending on $\overline{\text{PTRST}}$ being high or low, respectively. While $\overline{\text{BYP}}$ is low, shadow protocols are ignored. Otherwise, while $\overline{\text{BYP}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{BYP}}$ to a high level if it has no external connection.
$\overline{\text{CON}}$	Connect indicator (output). The ASP indicates secondary-scan-port activity (resulting from $\overline{\text{BYP}}$, $\overline{\text{BYP/TRST}}$, MULTICAST, or ON status) by forcing $\overline{\text{CON}}$ to be low. Inactivity (resulting from OFF, RESET, or TRST status) is indicated when $\overline{\text{CON}}$ is high.
GND	Ground
PTCK	Primary test clock. PTCK receives the TCK signal required by IEEE Std 1149.1-1990. The ASP always buffers PTCK to STCK. Shadow protocols are received/acknowledged synchronously to PTCK and connect-status changes invoked by shadow protocol are made synchronously to PTCK.
PTDI	Primary test data input. PTDI receives the TDI signal required by IEEE Std 1149.1-1990. During appropriate TAP states, the ASP monitors PTDI for shadow protocols. During shadow protocols, data at PTDI is captured on the rising edge of PTCK. When a valid shadow protocol is received in this fashion, the ASP compares the received address against the A9–A0 inputs. If the ASP detects a match, it outputs an acknowledgment and then connects its primary TAP terminals to its secondary TAP terminals. Under $\overline{\text{BYP}}$, $\overline{\text{BYP/TRST}}$, MULTICAST or ON status, the ASP buffers the PTDI signal to STDO. An internal pullup forces PTDI to a high level if it has no external connection.
PTDO	Primary test data output. PTDO transmits the TDO signal required by IEEE Std 1149.1-1990. During shadow protocols, the ASP transmits any required acknowledgment via the PTDO. The acknowledgment data output at PTDO changes on the falling edge of PTCK. Under $\overline{\text{BYP}}$, $\overline{\text{BYP/TRST}}$, or ON status, the ASP buffers the PTDO signal from STDI. Under OFF, MULTICAST, RESET, or TRST status, PTDO is at high impedance.
PTMS	Primary test mode select. PTMS receives the TMS signal required by IEEE Std 1149.1-1990. The ASP monitors the PTMS to determine the TAP-controller state. During stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test-Idle, Pause-DR, Pause-IR) the ASP can respond to shadow protocols. Under $\overline{\text{BYP}}$, MULTICAST, or ON status, the ASP buffers the PTMS signal to STMS. An internal pullup forces PTMS to a high level if it has no external connection.
$\overline{\text{PTRST}}$	Primary test reset. $\overline{\text{PTRST}}$ receives the $\overline{\text{TRST}}$ signal allowed by IEEE Std 1149.1-1990. The ASP always buffers $\overline{\text{PTRST}}$ to $\overline{\text{STRST}}$. A low input at $\overline{\text{PTRST}}$ forces the ASP to assume TRST or $\overline{\text{BYP/TRST}}$ status, depending on $\overline{\text{BYP}}$ being high or low, respectively. Such operation also asynchronously resets the internal ASP state to its power-up condition. Otherwise, while $\overline{\text{PTRST}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{PTRST}}$ to a high level if it has no external connection.
STCK	Secondary test clock. STCK retransmits the TCK signal required by IEEE Std 1149.1-1990. The ASP always buffers STCK from PTCK.
STDI	Secondary test data input. STDI receives the TDI signal required by IEEE Std 1149.1-1990. Under $\overline{\text{BYP}}$, $\overline{\text{BYP/TRST}}$, or ON status, the ASP buffers STDI to PTDO. An internal pullup forces STDI to a high level if it has no external connection.
STDO	Secondary test data output. STDO transmits the TDO signal required by IEEE Std 1149.1-1990. Under $\overline{\text{BYP}}$, $\overline{\text{BYP/TRST}}$, MULTICAST, or ON status, the ASP buffers STDO from PTDI. Under OFF, RESET, or TRST status, STDO is at high impedance.
STMS	Secondary test mode select. STMS retransmits the TMS signal required by IEEE Std 1149.1-1990. Under $\overline{\text{BYP}}$, MULTICAST, or ON status, the ASP buffers STMS from PTMS. When disconnected (as a result of OFF status), STMS maintains its last valid state until the ASP assumes $\overline{\text{BYP/TRST}}$, RESET, or TRST status (upon which it is forced high) or the ASP again assumes $\overline{\text{BYP}}$, MULTICAST, or ON status.
$\overline{\text{STRST}}$	Secondary test reset. $\overline{\text{STRST}}$ retransmits the $\overline{\text{TRST}}$ signal allowed by IEEE Std 1149.1-1990. The ASP always buffers $\overline{\text{STRST}}$ from $\overline{\text{PTRST}}$.
VCC	Supply voltage



application information

In application, the ASP is used at each of several (serially-chained) groups of IEEE Std 1149.1-compliant devices. The ASP for each such group is assigned an address (via inputs A9–A0) that is unique from that assigned to ASPs for the remaining groups. Each ASP is wired at its primary TAP to common (multidrop) TAP signals (sourced from a central IEEE Std 1149.1 bus master) and fans out its secondary TAP signals to the specific group of IEEE Std 1149.1-compliant devices with which it is associated. An example is shown in Figure 1.

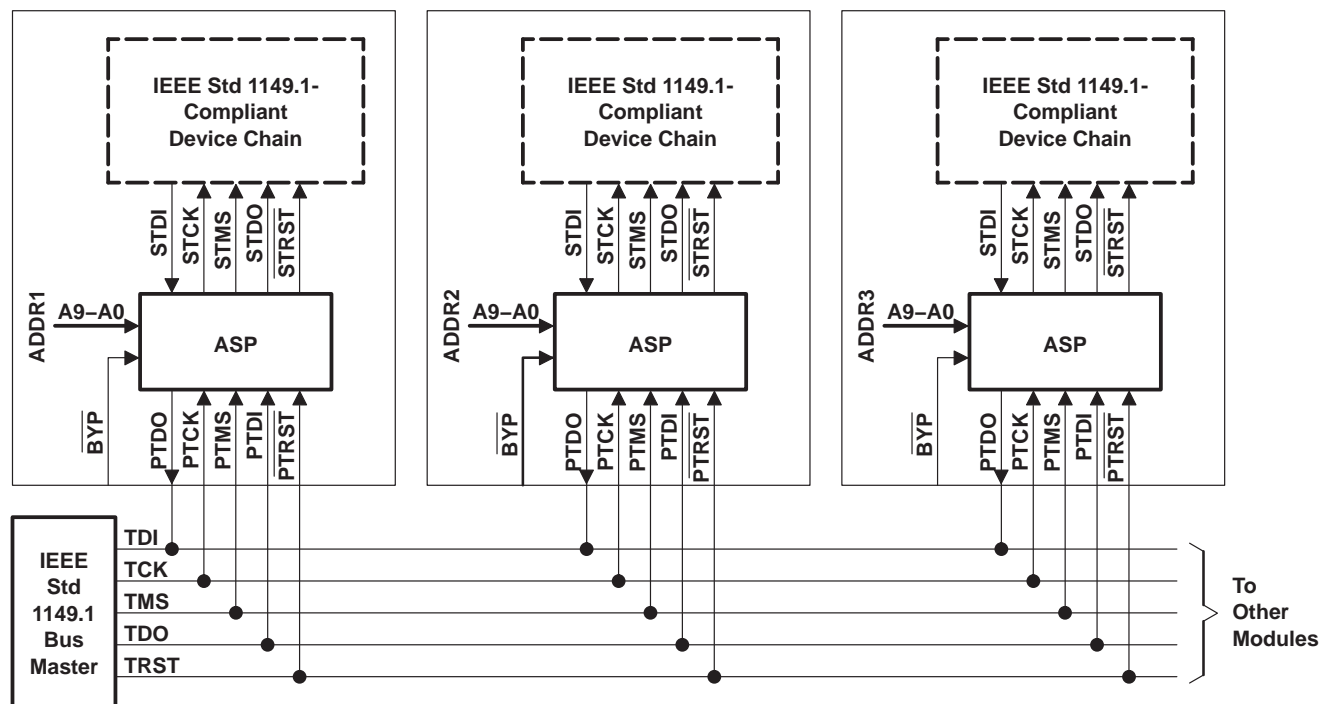


Figure 1. ASP Application

This application allows the ASP to be wired to a 4- or 5-wire multidrop test access bus, such as might be found on a backplane. Each ASP would then be located on a module, for example a printed-circuit board (PCB), that contains a serial chain of IEEE Std 1149.1-compliant devices and that would plug into the module-to-module bus (e.g., backplane). In the complete system, the ASP shadow protocols would allow the selection of the scan chain on a single module. The selected scan chain could then be controlled, via the multidrop TAP, as if it were the only scan chain in the system. Normal IR and DR scans can then be performed to accomplish the module test objectives.

Once scan operations to a given module are complete, another module can be selected in the same fashion, at which time the ASP-based connection to the first module is dissolved. This procedure can be continued progressively for each module to be tested. Finally, one of two global addresses can be issued to either leave all modules unselected (disconnect address, DSA) or to deselect and reset scan chains for all modules (reset address, RSA).

Additionally, in Pause-DR and Pause-IR TAP states, a third global address (test-synchronization address, TSA) can be invoked to allow simultaneous TAP-state changes and multicast scan-in operations to selected modules. This is especially useful in the former case, for allowing selected modules to be moved simultaneously to the Run-Test-Idle TAP state for module-level or module-to-module built-in self-test (BIST) functions, which operate synchronously to TCK in that TAP state, and in the latter case, for scanning common test setup/data into multiple like modules.

architecture

Conceptually, the ASP can be viewed as a bank of switches that can connect or isolate a module-level TAP to/from a higher-level (e.g., module-to-module) TAP. This is shown in Figure 2. The state of the switches (open versus closed) is based on shadow protocols, which are received on PTDI and are synchronous to PTCK.

The simple architecture of the ASP allows the system designer to overcome the limitations of IEEE Std 1149.1 *ring* and *star* configurations. Ring configurations (in which each module's TDO is chained to the next module's TDI) are of limited use in backplane environments, since removal of a module breaks the scan chain and prevents test of the remainder of the system. Star configurations (in which all module TDOs and TDIs are connected in parallel) are suited to the backplane environment, but, since each module must receive its own TMS, are costly in terms of backplane routing channels. By comparison, use of the ASP allows all five IEEE Std 1149.1 signals to be routed in multidrop fashion.

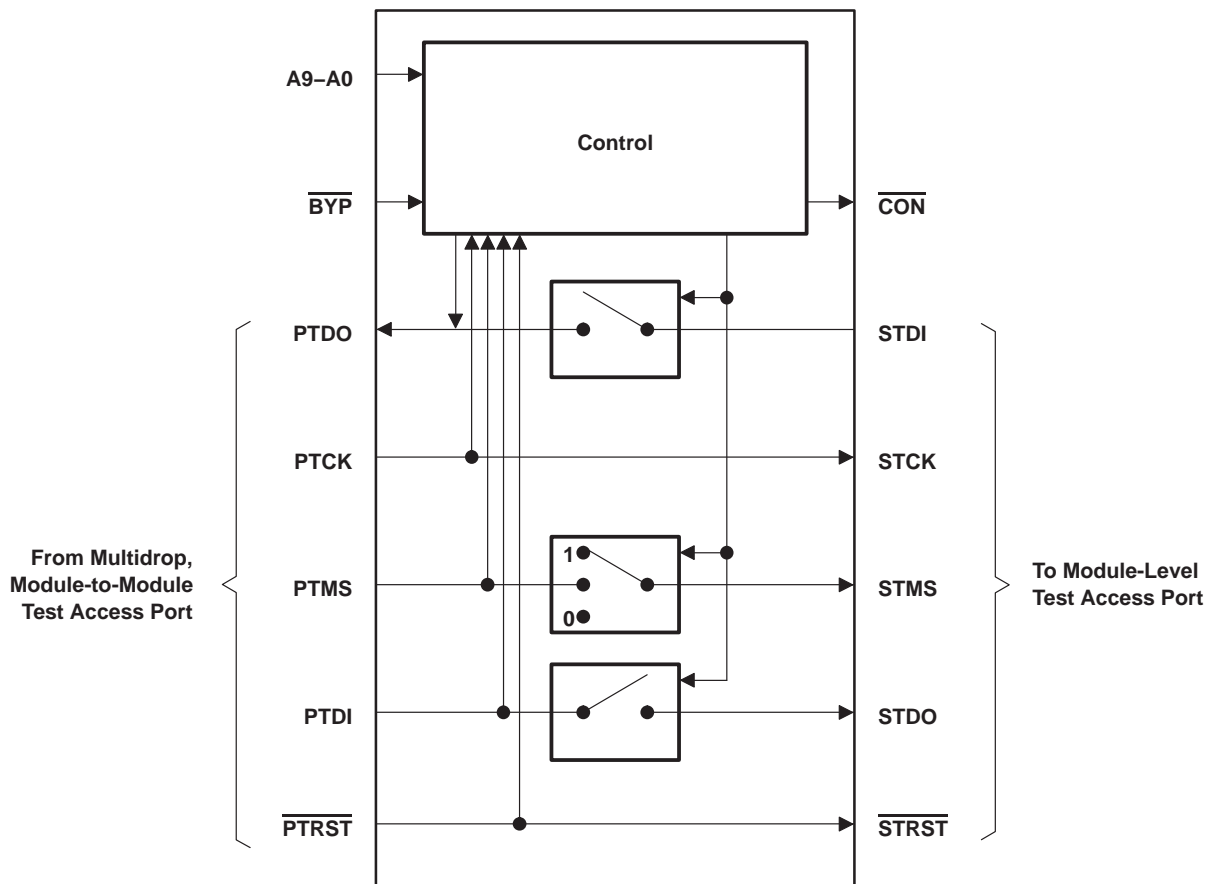


Figure 2. ASP Conceptual Model

As shown in the functional block diagram, the ASP comprises three major logic blocks. Blocks for shadow-protocol receive and shadow-protocol transmit are responsible for receipt of select protocol and transmission of acknowledge protocol, respectively. The connect-control block is responsible for TAP-state monitor and address matching.

Some additional logic is illustrated outside of these major blocks. This additional logic is responsible for controlling the activity of the ASP outputs based on the shadow-protocol result and/or protocol bypass [as selected by an active (low) $\overline{\text{BYP}}$ input].

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shadow protocol

Addressing of an ASP in system is accomplished by shadow protocols, which are received at PTDI synchronously to PTCK. Shadow protocols can occur only in the following stable TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. Shadow protocols never occur in Shift-DR or Shift-IR states to prevent contention on the signal bus to which PTDO is wired. Additionally, the ASP PTMS must be held at a constant low or high level throughout a shadow protocol. If TAP-state changes occur in the midst of a shadow protocol, the shadow protocol is aborted and the select-protocol state machine returns to its initial state.

The shadow protocol is based on a serial bit-pair signaling scheme in which two bit-pair combinations (data one, data zero) are used to represent address data and the other two bit-pair combinations (select, idle) are used for framing – that is, to indicate where address data begins and ends.

These bit pairs are received serially at PTDI (or transmitted serially at PTDO) synchronously to PTCK as follows:

- The idle bit pair (I) is represented as two consecutive high signals.
- The select bit pair (S) is represented as two consecutive low signals.
- The data-one bit pair (D) is represented as a low signal followed by a high signal.
- The data-zero bit pair (D) is represented as a high signal followed by a low signal.

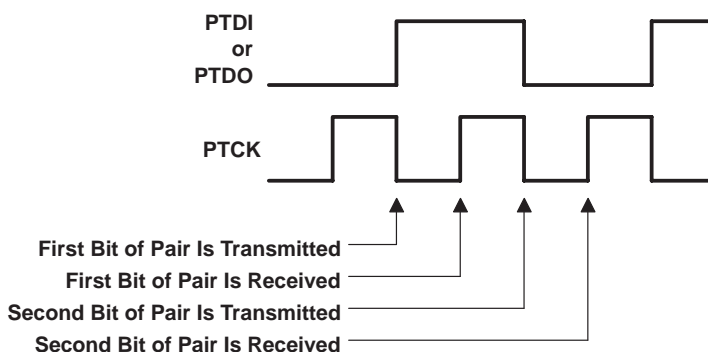


Figure 3. Bit-Pair Timing (Data Zero Shown)

A complete shadow protocol is composed of the receipt of a select protocol followed, if applicable, by the transmission of an acknowledge protocol (which is issued from PTDO only if the received address matches that at the A9–A0 inputs). Both of these subprotocols are composed of ten data bit pairs framed at the beginning by idle and select bit pairs and at the end by select and idle bit pairs. This is represented in an abbreviated fashion as follows: ISDDDDDDDDDSI. Figure 4 shows a complete shadow protocol (the symbol T is used to represent a high-impedance condition on the associated signal line – since the high-impedance state at PTDI is logically high due to pullup, it maps onto the idle bit pair).

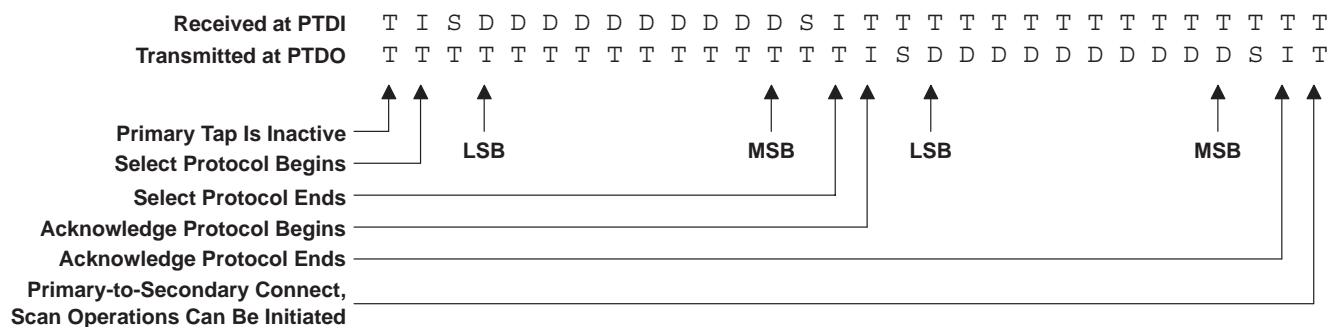


Figure 4. Complete Shadow Protocol

select protocol

The select protocol is the ASP's means of receiving (at PTDI) address information from an IEEE Std 1149.1 bus master. It follows the ISDDDDDDDDDSI sequence described previously. A 10-bit address value is decoded from the received data-one and/or data-zero bit pairs. These bit pairs are interpreted in least-significant-bit-first order (that is, the first data bit pair received is considered to correspond to A0).

acknowledge protocol

Following the receipt of a complete select-protocol sequence, the protocol result provisionally is set to NO MATCH and the connect status set to OFF. The received address is then compared to that at the ASP address inputs (A9–A0). If these address values match, the ASP immediately (with no delay) responds with an acknowledge protocol transmitted from PTDO. This protocol follows the ISDDDDDDDDDSI sequence described previously. The transmitted address represents the address of the selected ASP which, by definition, is the same address the ASP received in the select protocol. The 10-bit address value is encoded into data-one and/or data-zero bit pairs. The bit pairs are to be interpreted in least-significant-bit-first order (that is, the first data bit pair transmitted is to be considered to correspond to A0). If the received address does not match that at the A9–A0 inputs, no acknowledge protocol is transmitted and the shadow protocol is considered complete.

protocol errors

Protocol errors occur when bit pairs are received out of sequence. Some of these sequencing errors can be tolerated and produce protocol result SOFT ERROR – no specific action occurs as a result. Other errors represent cases where the addressing information could be incorrectly received and produce protocol result HARD ERROR – these are characterized by sequences in which at least one bit of address data has been properly transmitted, followed by a sequencing error; when protocol result HARD ERROR occurs, any connection to an ASP is dissolved.

Table 1 lists the bit-pair sequences that produce protocol results SOFT ERROR and HARD ERROR. A hard error also results when the primary TAP state changes during select protocol following the proper transmission of at least one bit of address data. Figures 16 and 17 show shadow-protocol timing in case of protocol result HARD ERROR while Figure 18 shows shadow-protocol timing in case of protocol result SOFT ERROR.

Table 1. Shadow-Protocol Errors[†]

SOFT ERROR	HARD ERROR
I(D)I	
I(D)(S)I	
I(D)(S)(D)I	IS(D)I
I(S)I	IS(D)S(D)I
IS(S)(D)I	IS(D)S(S)I
IS(S)(D)(S)I	

[†] A bit-pair token in parentheses represents one or more instances.

long address

Receipt of an address longer than ten bits produces protocol result HARD ERROR and the ASP assumes OFF status. The sole exceptions are when all data ones are received or all data zeros are received. In these special cases, the global addresses represented by these bit sequences are observed and appropriate action taken. That is, in the case that only data ones (ten or more) are received, the shadow-protocol result is TEST SYNCHRONIZATION (if the primary TAP state is Pause-DR or Pause-IR), and in the case that only data zeros (ten or more) are received, the shadow-protocol result is RESET (see test-synchronization address and reset address).

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short address

In all cases, receipt of an address shorter than ten bits produces protocol result HARD ERROR and the ASP assumes OFF status.

connect control

The connect-control block monitors the primary TAP state to enable receipt/acknowledge of shadow protocols in appropriate states (namely, the stable, non-Shift TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR). Upon receipt of a valid shadow protocol, this block performs the address matching required to compute the shadow-protocol result.

TAP-state monitor

The TAP-state monitor is a synchronous finite-state machine that monitors the primary TAP state. The state diagram is shown in Figure 5 and mirrors that specified by IEEE Std 1149.1-1990. The TAP-state monitor proceeds through its states based on the level of PTMS at the rising edge of PTCK. Each state is described both in terms of its significance for ASP devices and for connected IEEE Std 1149.1-compliant devices (called targets). However, the monitor state (primary TAP) can be different from that of disconnected scan chains (secondary TAP).

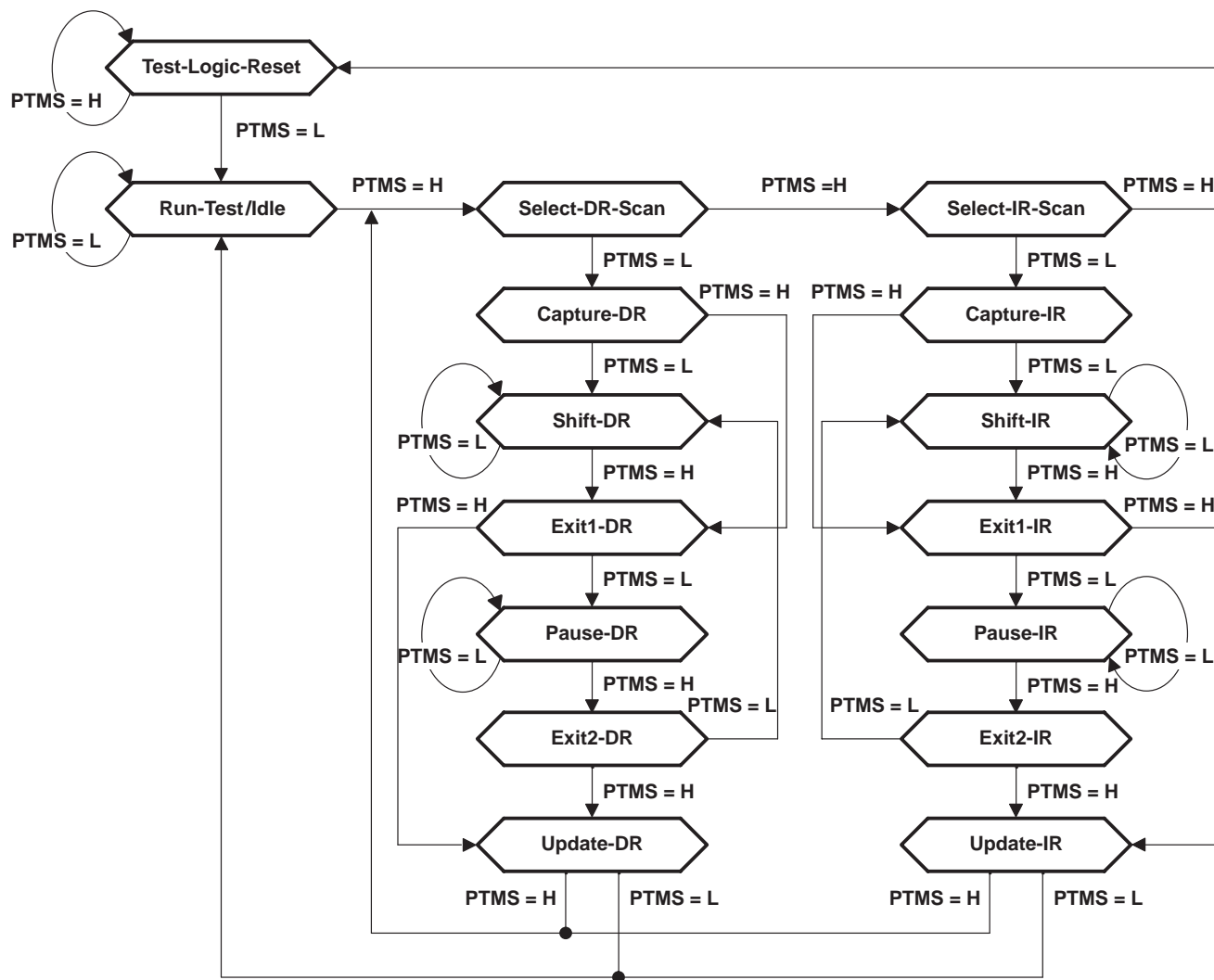


Figure 5. TAP-Monitor State Diagram

Test-Logic-Reset

The ASP TAP-state monitor powers up in the Test-Logic-Reset state. Alternatively, the ASP can be forced asynchronously to this state by assertion of its `PTRST` input. In the stable Test-Logic-Reset state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

Run-Test/Idle

In the stable Run-Test/Idle state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

Select-DR-Scan, Select-IR-Scan

The ASP is not enabled to receive and respond to shadow protocols in the Select-DR-Scan and Select-IR-Scan states.

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

The ASP is not enabled to receive and respond to shadow protocols in the Capture-DR state.

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

Shift-DR

The ASP is not enabled to receive and respond to shadow protocols in the Shift-DR state.

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

Exit1-DR, Exit2-DR

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-DR and Exit2-DR states.

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

In the stable Pause-DR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

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Update-DR

The ASP is not enabled to receive and respond to shadow protocols in the Update-DR state.

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

The ASP is not enabled to receive and respond to shadow protocols in the Capture-IR state.

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.

Shift-IR

The ASP is not enabled to receive and respond to shadow protocols in the Shift-IR state.

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

Exit1-IR, Exit2-IR

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-IR and Exit2-IR states.

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

In the stable Pause-IR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

The ASP is not enabled to receive and respond to shadow protocols in the Update-IR state.

For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

address matching

Connect status of the ASP is computed by a match of the address received in the last valid shadow protocol against that at the address inputs (A9–A0) as well as against the three dedicated addresses that are internal to the ASP (DSA, RSA, and TSA). The address map is shown in Table 2.

Table 2. Address Map

ADDRESS NAME	BINARY CODE	HEX CODE	SHADOW-PROTOCOL RESULT	RESULTANT PRIMARY-TO-SECONDARY CONNECT STATUS
Reset Address (RSA)	0000000000	000	RESET	RESET
Matching Address	A9–A0	A9–A0	MATCH	ON
Disconnect Address (DSA)	1111111110	3FE	DISCONNECT	OFF
Test Synchronization Address (TSA)	1111111111	3FF	TEST SYNCHRONIZATION	MULTICAST
All Other Addresses	All others	All others	NO MATCH	OFF

If the shadow-protocol address matches the address inputs (A9–A0), then the ASP responds by transmitting an acknowledge protocol. Following the complete transmission of the acknowledge protocol, the ASP assumes ON status (in which PTDI, PTDO, and PTMS are connected to STDO, STDI, and STMS, respectively). The ON status allows the scan chain associated with the ASP's secondary TAP to be controlled from the multidrop primary TAP as if it were directly wired as such. Figures 6 and 7 show the shadow-protocol timing for MATCH result when the prior ASP connect status is ON and OFF, respectively.

If the shadow-protocol address does not match the address inputs (A9–A0), then (unless the address is one of the three dedicated global addresses described below) the ASP responds immediately by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 8 and 9 show the shadow-protocol timing for NO MATCH result when the prior ASP connect status is ON and OFF, respectively.

disconnect address

The disconnect address (DSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the DSA, it immediately responds by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 10 and 11 show the shadow-protocol timing for DISCONNECT result when the prior ASP connect status is ON and OFF, respectively.

The same result occurs when a nonmatching address is received. No specific action to disconnect an ASP is required, as a given ASP is disconnected by the address that connects another. The dedicated DSA ensures that at least one address is available for the purpose of disconnecting all receiving ASPs. It is especially useful when the currently selected scan chain is in a different TAP state than that to be selected. In such a case, the DSA is used to leave the former scan chain in the proper state, after which the primary TAP state is moved to that needed to select the latter scan chain.

reset address

The reset address (RSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the RSA, it immediately responds by assuming the RESET status (in which PTDO and STDO are high impedance and STMS is forced to the high level). This has the effect of deselecting and resetting (to Test-Logic-Reset state) the scan chain associated with the ASP secondary TAP. No acknowledge protocol is sent. Figures 12 and 13 show the shadow-protocol timing for RESET result when the prior ASP connect status is ON and OFF, respectively.

test synchronization address

The test synchronization address (TSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the TSA while its secondary TAP state is Pause-DR or Pause-IR, it immediately responds by assuming the MULTICAST status (in which PTDI and PTMS are connected to STDO and STMS respectively, while PTDO is high impedance). No acknowledge protocol is sent. The TSA is valid only when the TAP state of both primary and secondary is Pause-DR or Pause-IR. If the TSA is received when the TAP state of either primary or secondary is Test-Logic-Reset or Run-Test-Idle, the shadow-protocol result is considered to be DISCONNECT. Figures 14 and 15 show the shadow-protocol timing for TEST SYNCHRONIZATION result when the prior ASP connect status is ON and OFF, respectively.

The TSA allows simultaneous operation of the scan chains of all selected ASPs, either for global TAP-state movement or for scan input of common serial test data via PTDI. This is especially useful in the former case, to simultaneously move such scan chains into the Run-Test/Idle state in which module-level or module-to-module BIST operations can operate synchronous to TCK in that TAP state, and in the later case, to scan common test setup/data into multiple like modules.

protocol bypass

Protocol bypass is selected by a low $\overline{\text{BYP}}$ input. This protocol-bypass mode forces the ASP into BYP status (primary TAP signals are connected to secondary TAP signals) regardless of previous shadow-protocol results. The $\overline{\text{CON}}$ output is made active (low). Receipt of shadow protocols is disabled.

When $\overline{\text{BYP}}$ is taken low, the primary TAP serial data signals (PTDI, PTDO) are immediately (asynchronously to PTCK) connected to their respective secondary TAP signals (STDO, STDI). The primary TAP mode-select signal (PTMS) is also connected to its respective secondary TAP signal (STMS) unless $\overline{\text{PTRST}}$ is low, in which case STMS remains high until $\overline{\text{PTRST}}$ is released. Also, the shadow-protocol-receive block is reset to its power-up state and is held in this state such that select protocols appearing at the primary TAP are ignored.

When the $\overline{\text{BYP}}$ input is released (taken high), the ASP immediately (asynchronously to PTCK) resumes the connect status selected by the last valid shadow protocol. The shadow-protocol-receive block is again enabled to respond to select protocols.

Figures 19 and 20 show protocol-bypass timing when the ASP connect status before $\overline{\text{BYP}}$ active is ON and OFF, respectively.

asynchronous reset

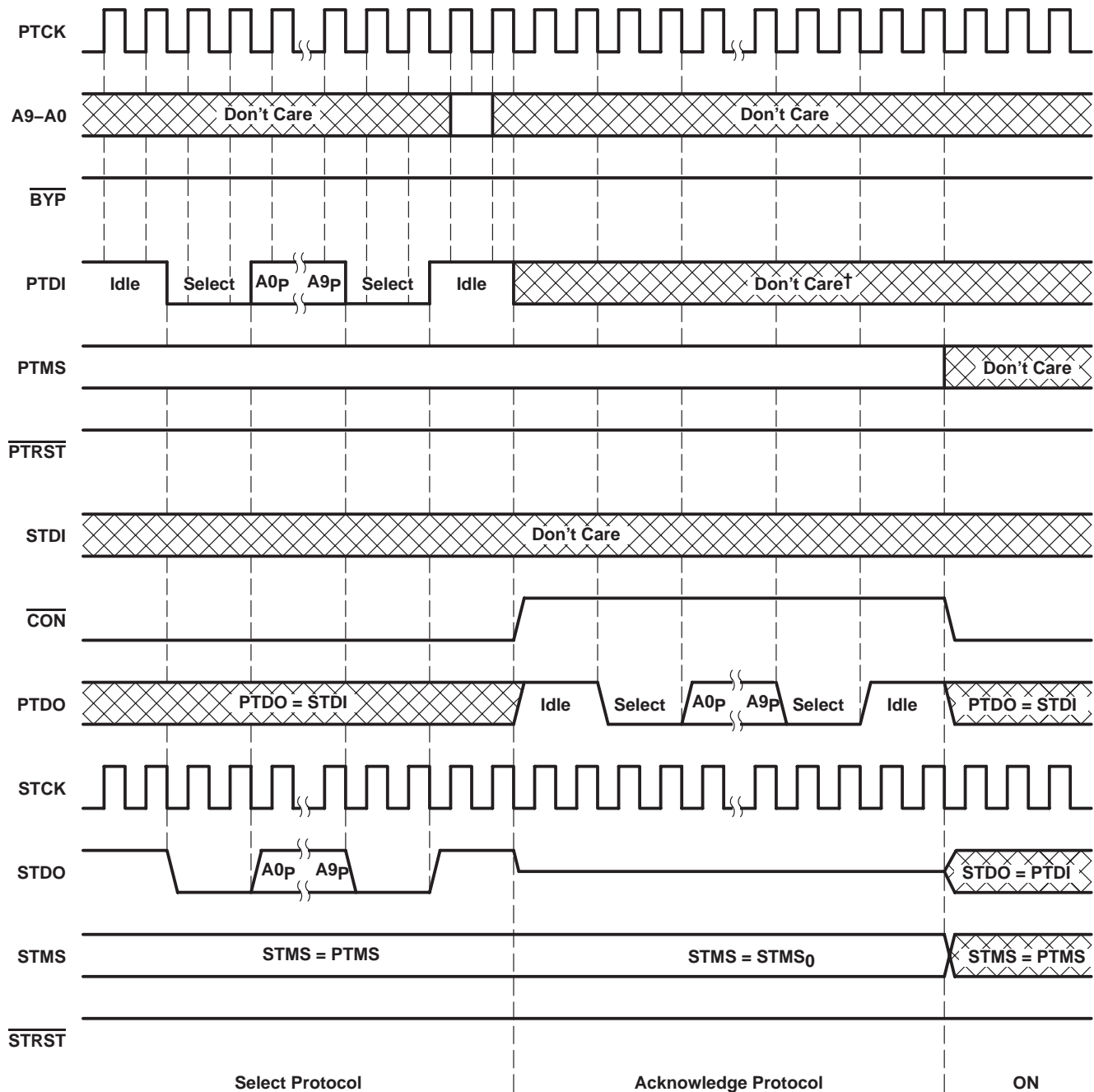
While the $\overline{\text{PTRST}}$ input is always buffered directly to the $\overline{\text{STRST}}$ output, it also serves as an asynchronous reset for the ASP. Given that $\overline{\text{BYP}}$ is high, when $\overline{\text{PTRST}}$ goes low, the ASP immediately assumes TRST status, in which $\overline{\text{CON}}$ is high and PTDO and STDO are at high impedance. Otherwise, if $\overline{\text{BYP}}$ is low, the ASP assumes BYP/TRST status. In either case, STMS is set high so that connected IEEE Std 1149.1-compliant devices can be synchronously driven to their Test-Logic-Reset states. While $\overline{\text{PTRST}}$ is low, receipt of shadow protocols is disabled.

Figures 21 and 22 show asynchronous reset timing when the ASP connect status before $\overline{\text{PTRST}}$ active is ON and OFF, respectively. Figure 23 shows asynchronous reset timing when $\overline{\text{BYP}}$ is low.

connect indicator

The $\overline{\text{CON}}$ output indicates secondary-scan-port activity (STDO, STMS active) regardless of whether such activity is achieved via protocol bypass or shadow protocol. If the $\overline{\text{BYP}}$ input is low, the $\overline{\text{CON}}$ output is low. Otherwise, if the $\overline{\text{BYP}}$ input is high, the $\overline{\text{CON}}$ output is low if the result of the last valid shadow protocol is MATCH or TEST SYNCHRONIZATION. In all other cases, and while acknowledge protocol is in progress, the $\overline{\text{CON}}$ output is high.

shadow-protocol timing

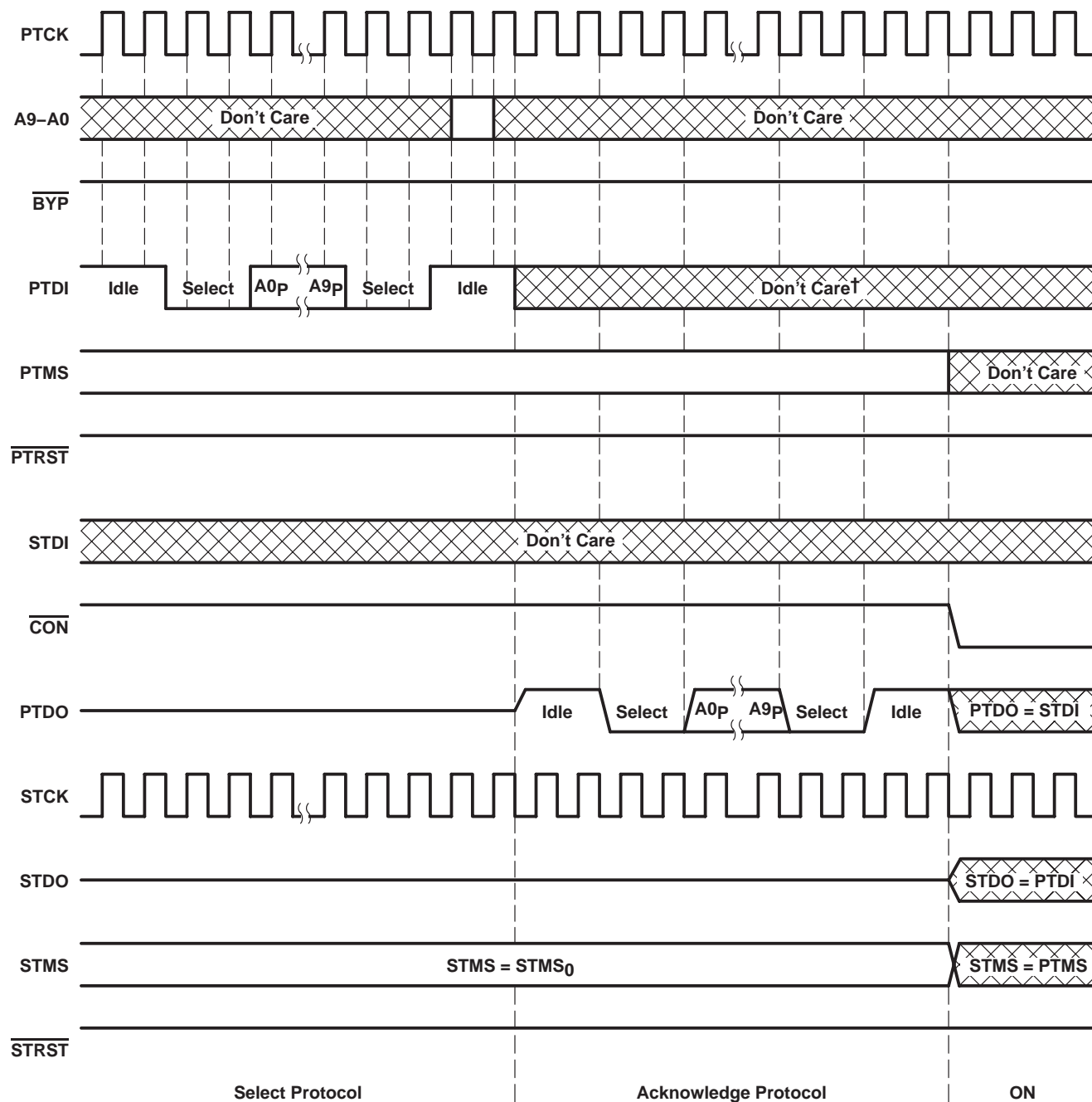


† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent another valid select protocol or produce protocol result HARD ERROR.

Figure 6. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = ON

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† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent another valid select protocol or produce protocol result HARD ERROR.

Figure 7. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = OFF

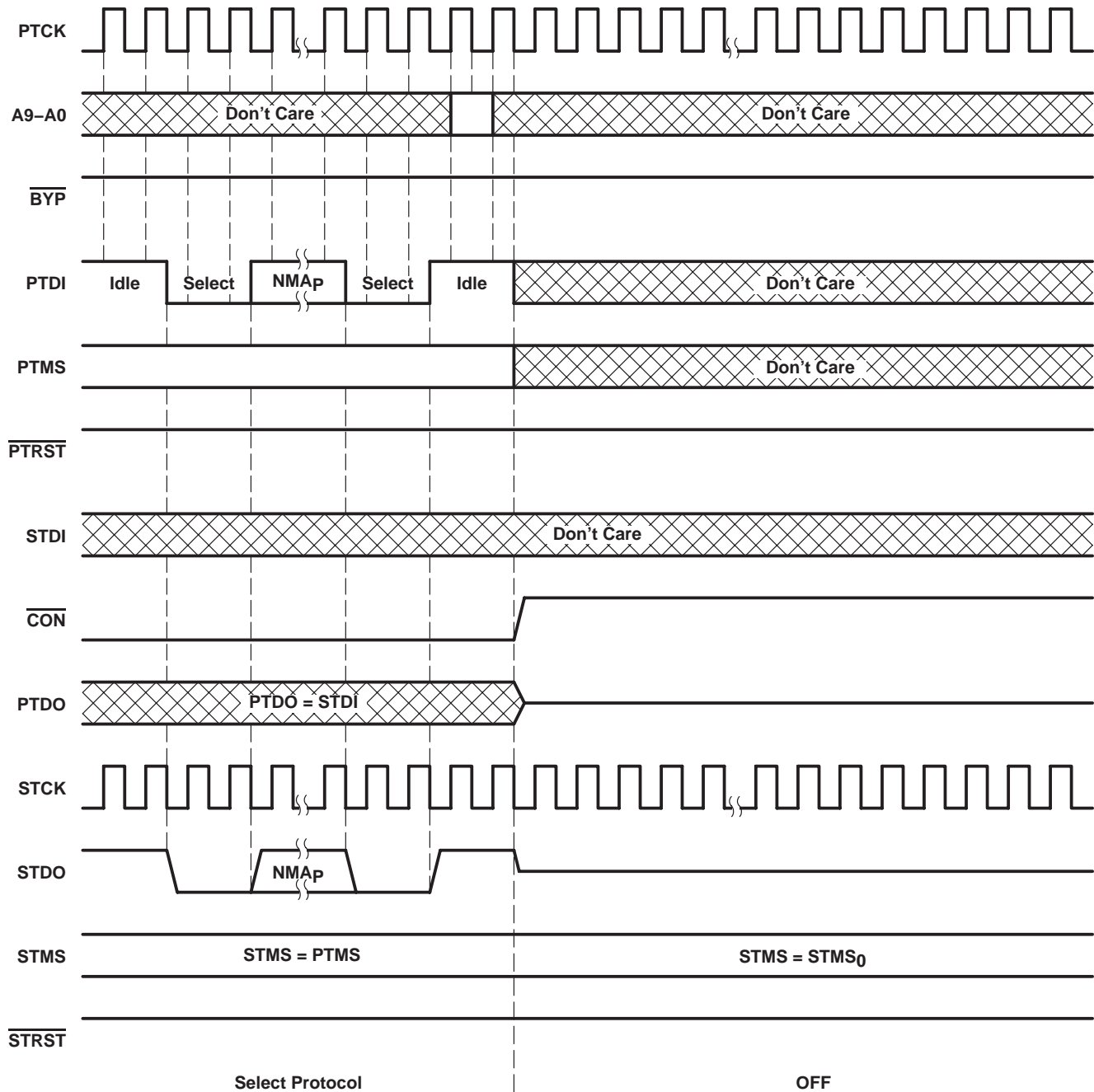


Figure 8. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = ON

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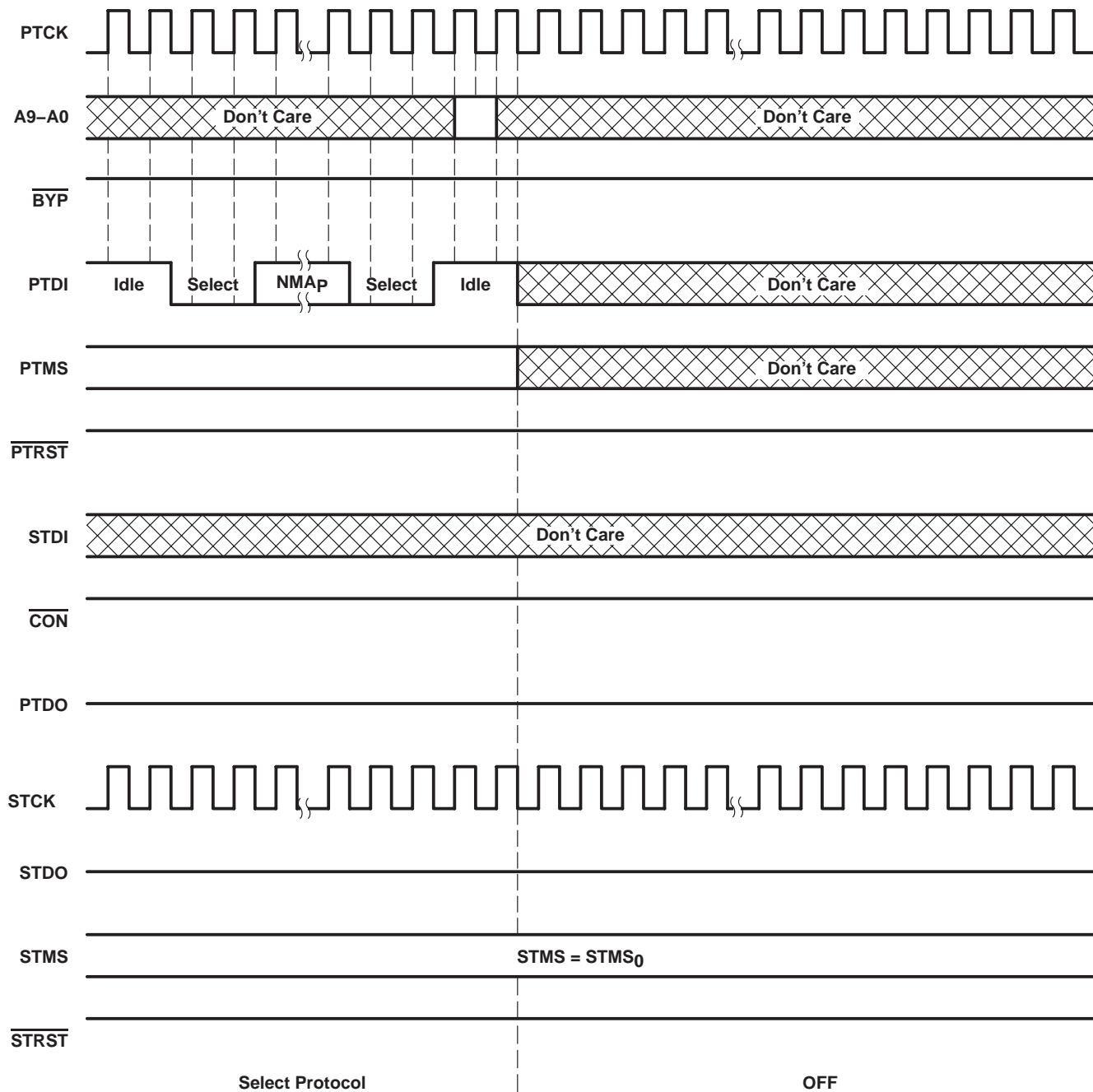


Figure 9. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = OFF

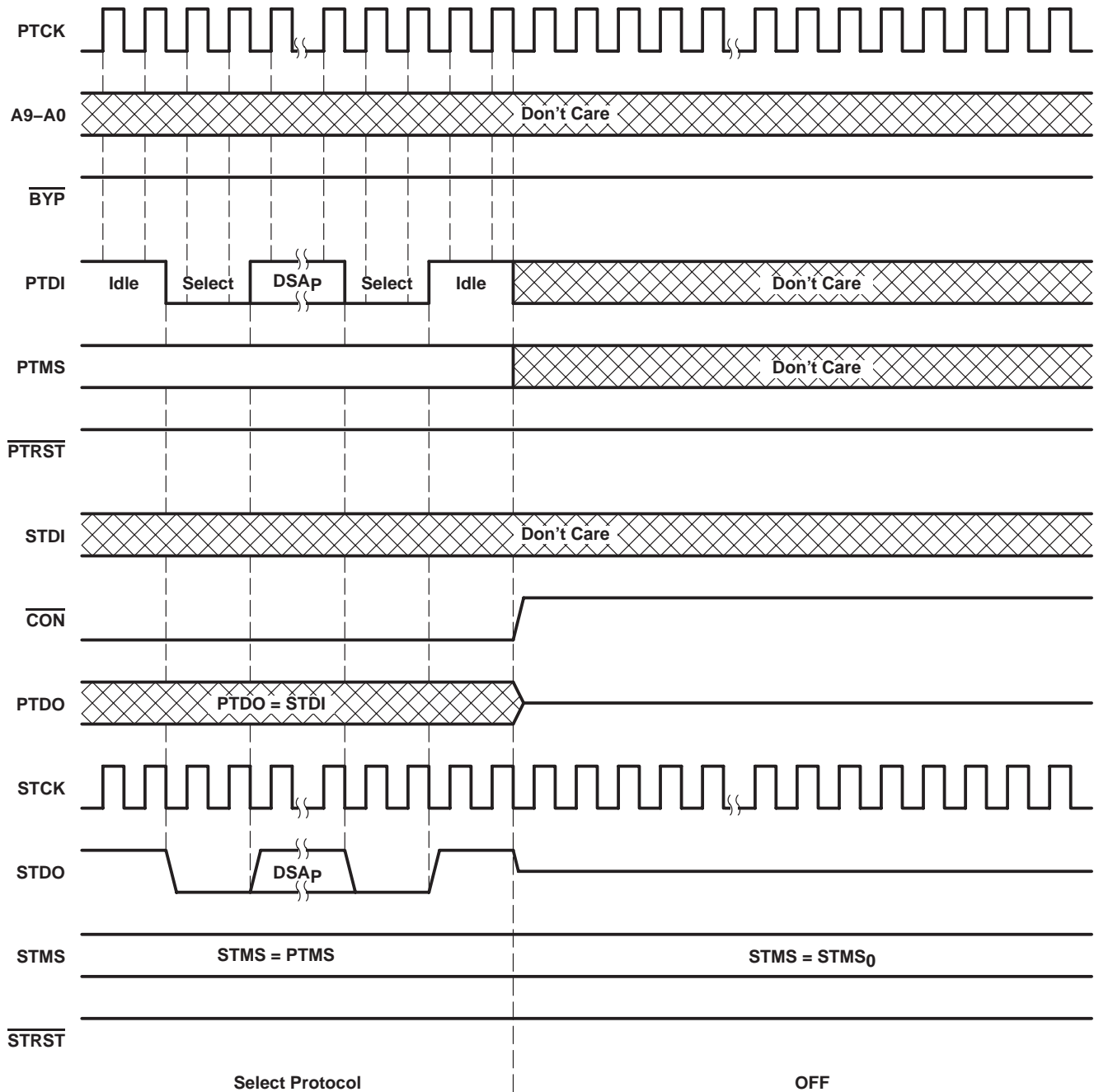
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Figure 10. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = ON

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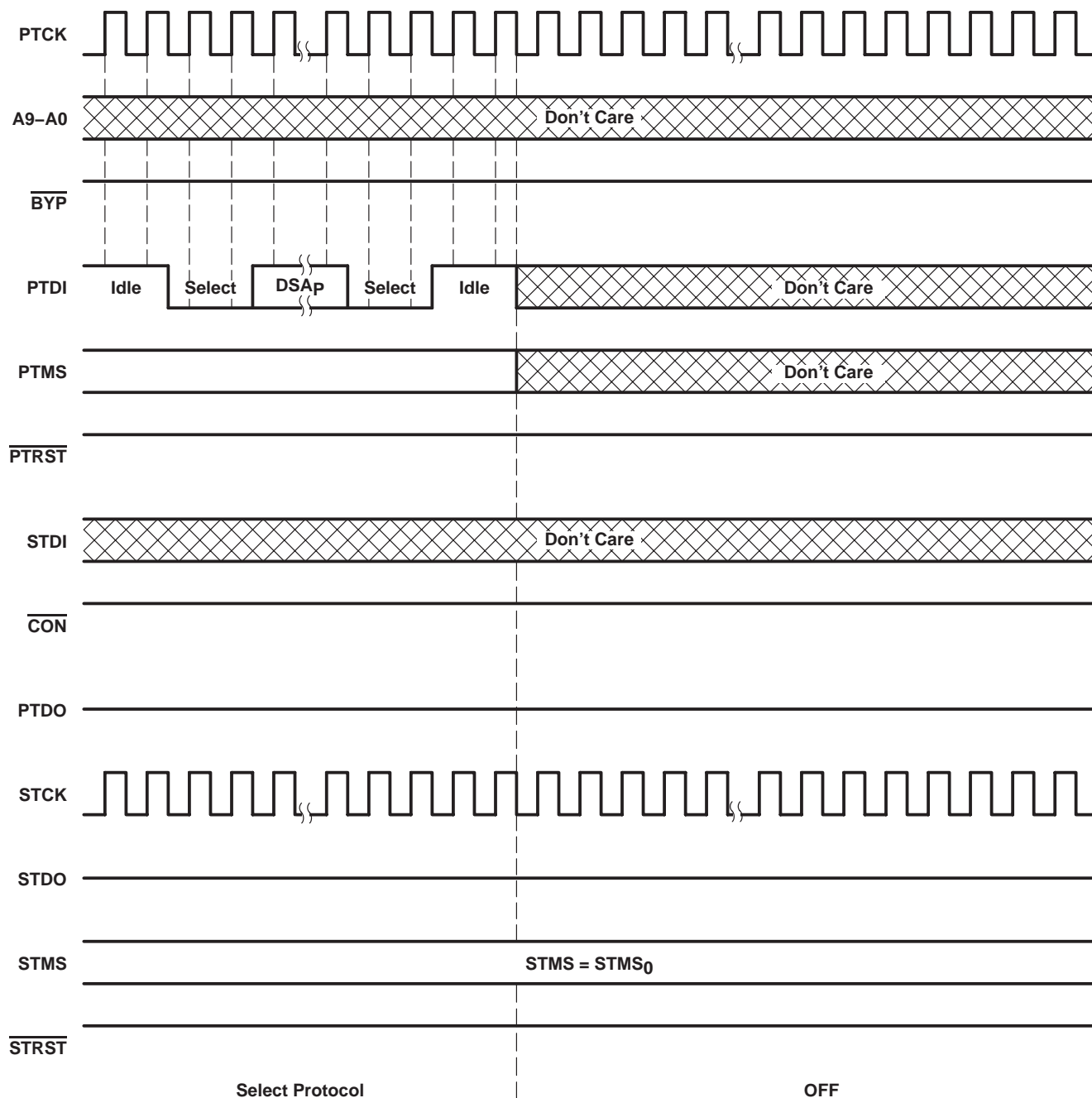


Figure 11. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = OFF

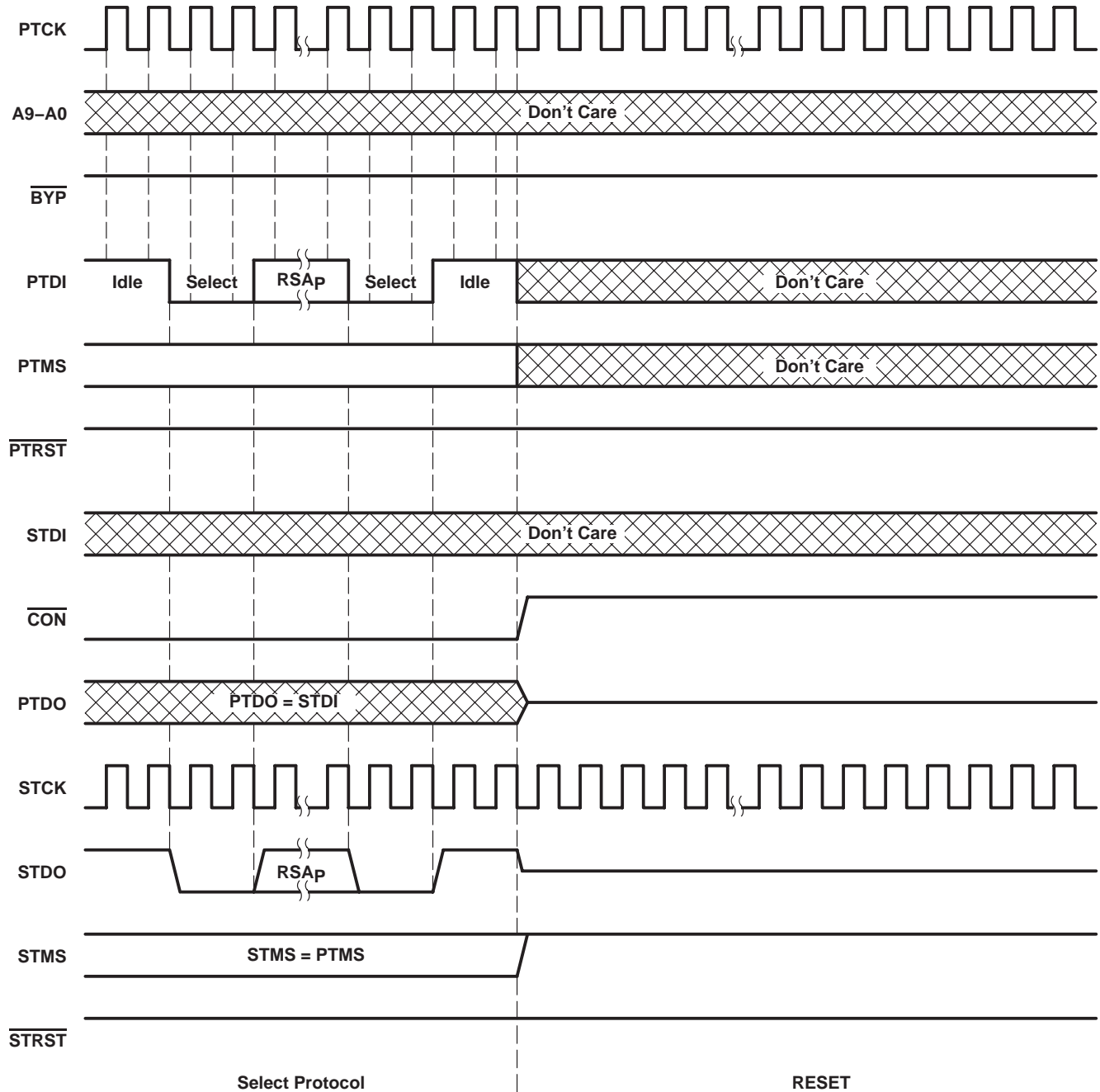
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Figure 12. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = ON

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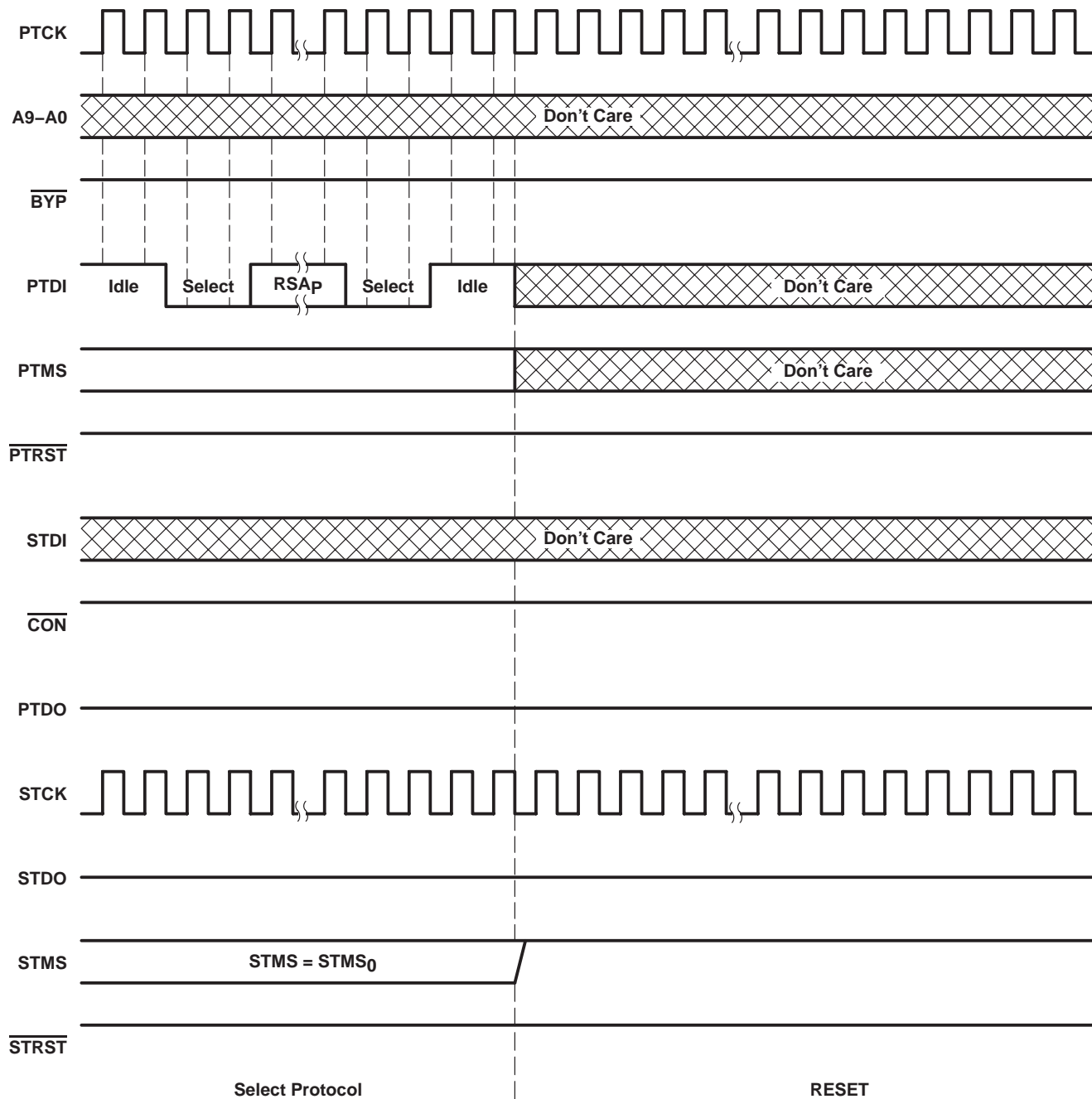


Figure 13. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = OFF

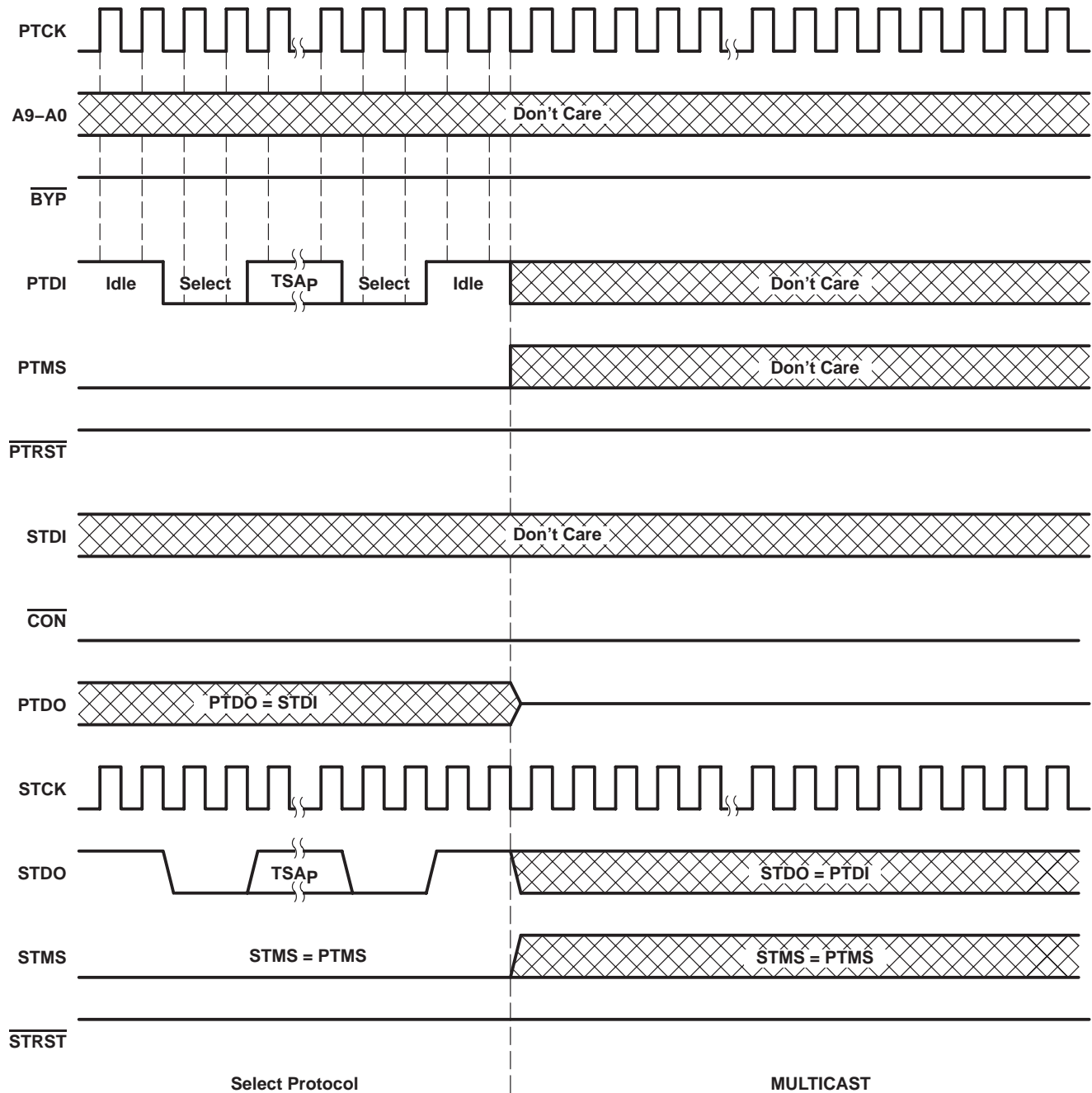


Figure 14. Shadow-Protocol Timing,
Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = ON

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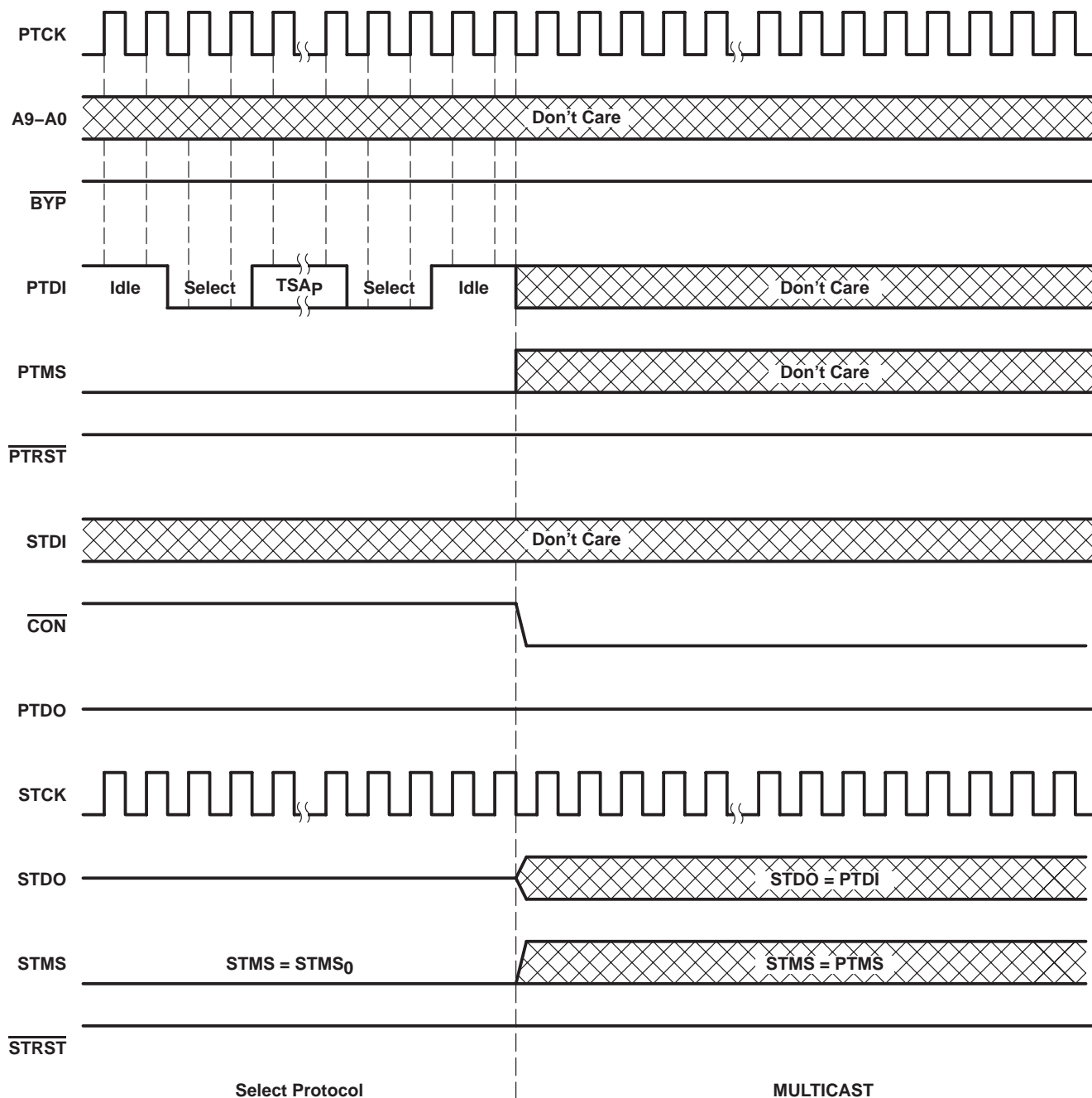
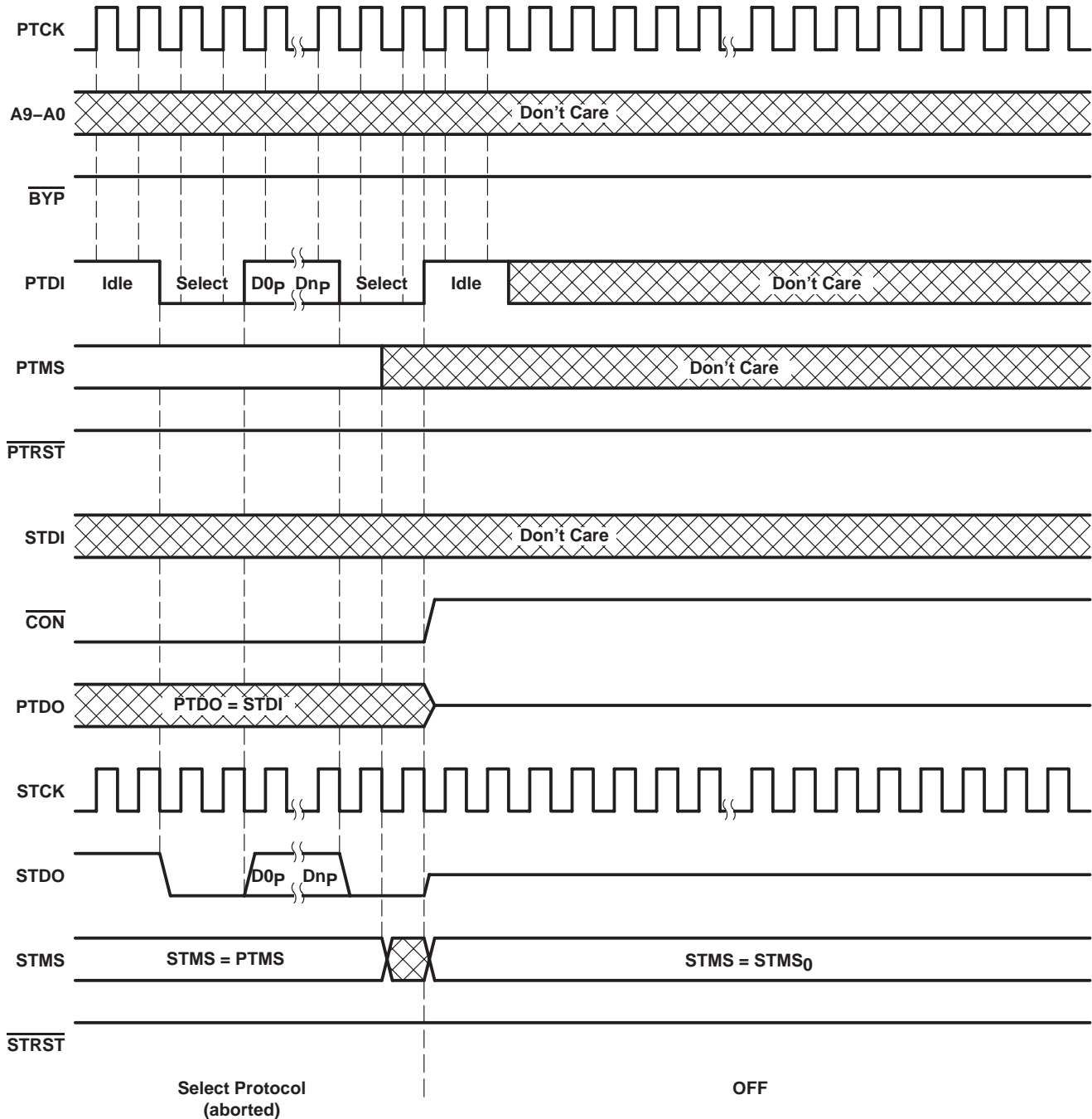


Figure 15. Shadow-Protocol Timing,
Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = OFF

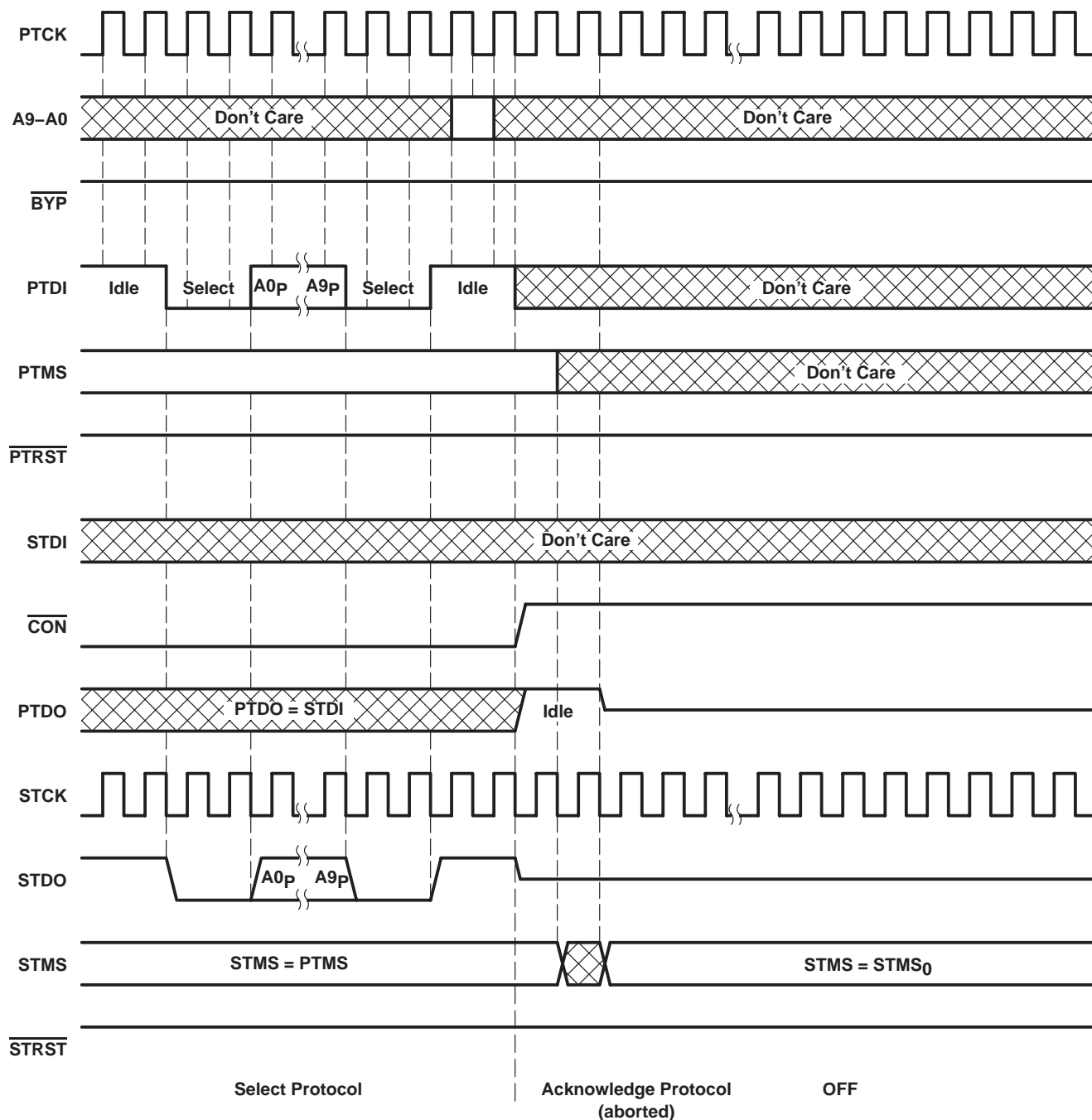


NOTE A: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

**Figure 16. Shadow-Protocol Timing,
Protocol Result = HARD ERROR (PTMS Change During Select Protocol), Prior Connect Status = ON**

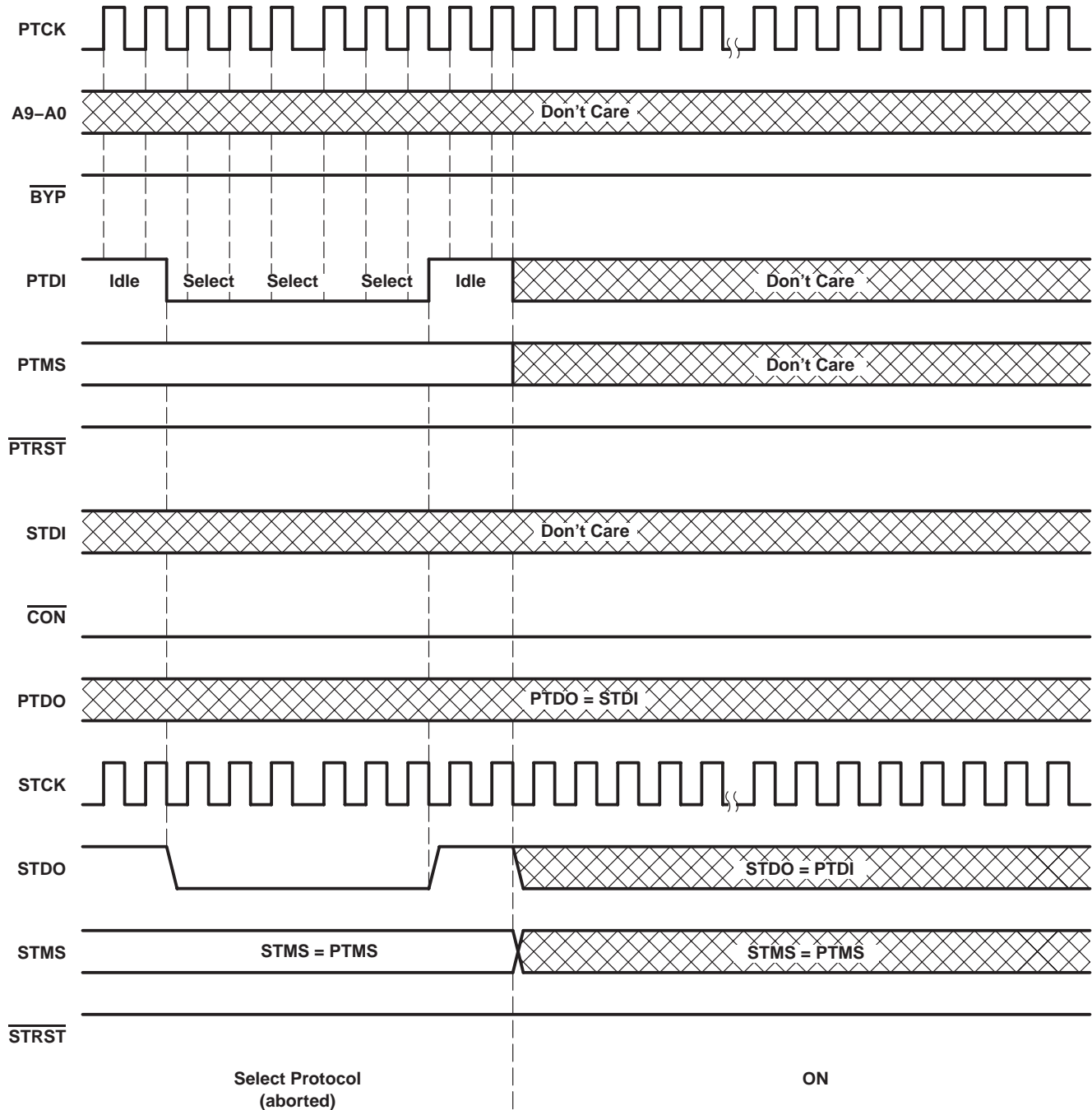
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NOTE A: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

**Figure 17. Shadow-Protocol Timing,
Protocol Result = HARD ERROR (PTMS Change During Acknowledge Protocol),
Prior Connect Status = ON**



NOTE A: The sequence of PTDI bits shown in this figure is only one of many that would produce protocol result SOFT ERROR.

**Figure 18. Shadow-Protocol Timing,
Protocol Result = SOFT ERROR, Prior Connect Status = ON**

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protocol-bypass timing

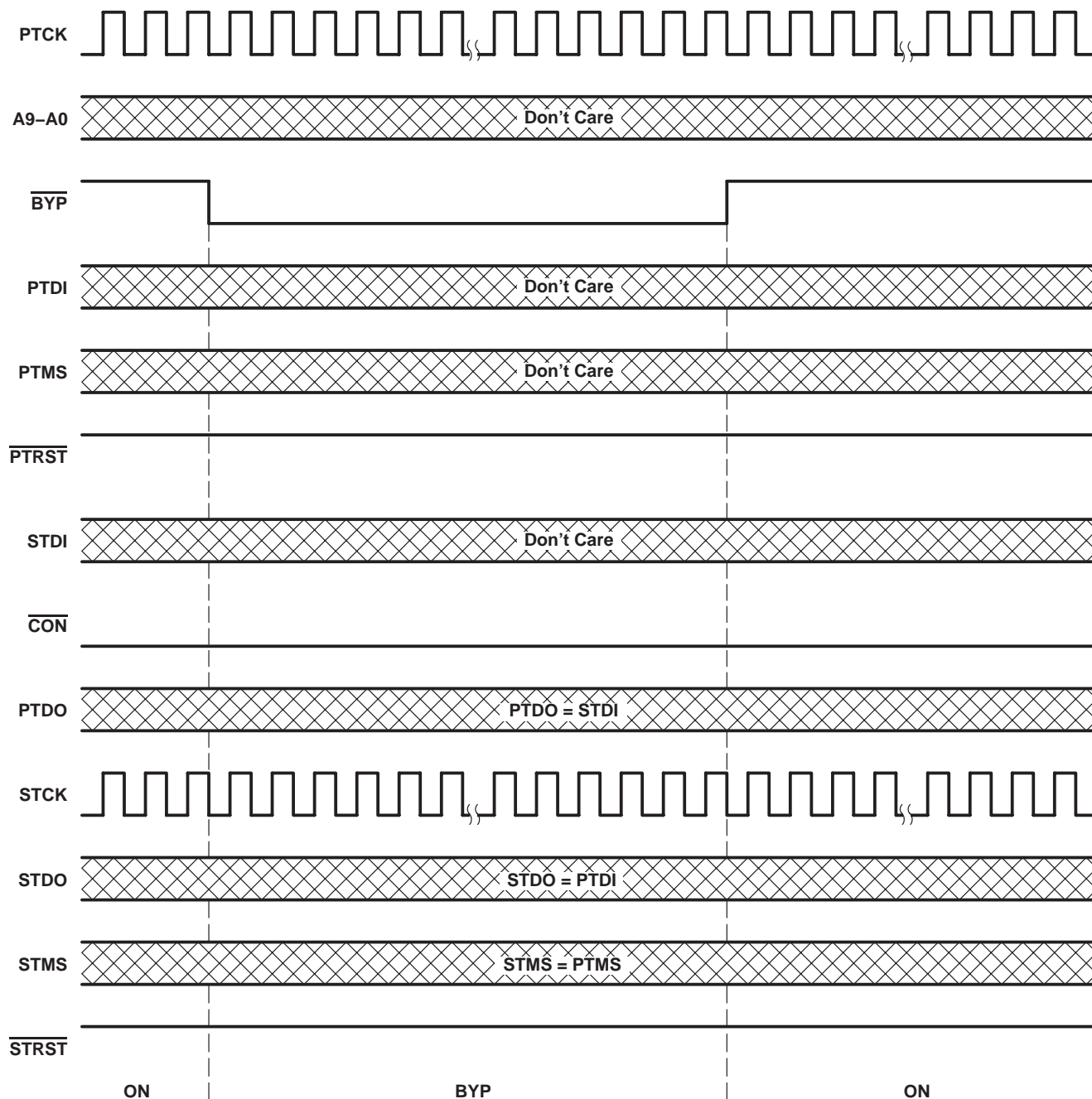


Figure 19. Protocol-Bypass Timing, Prior Connect Status = ON

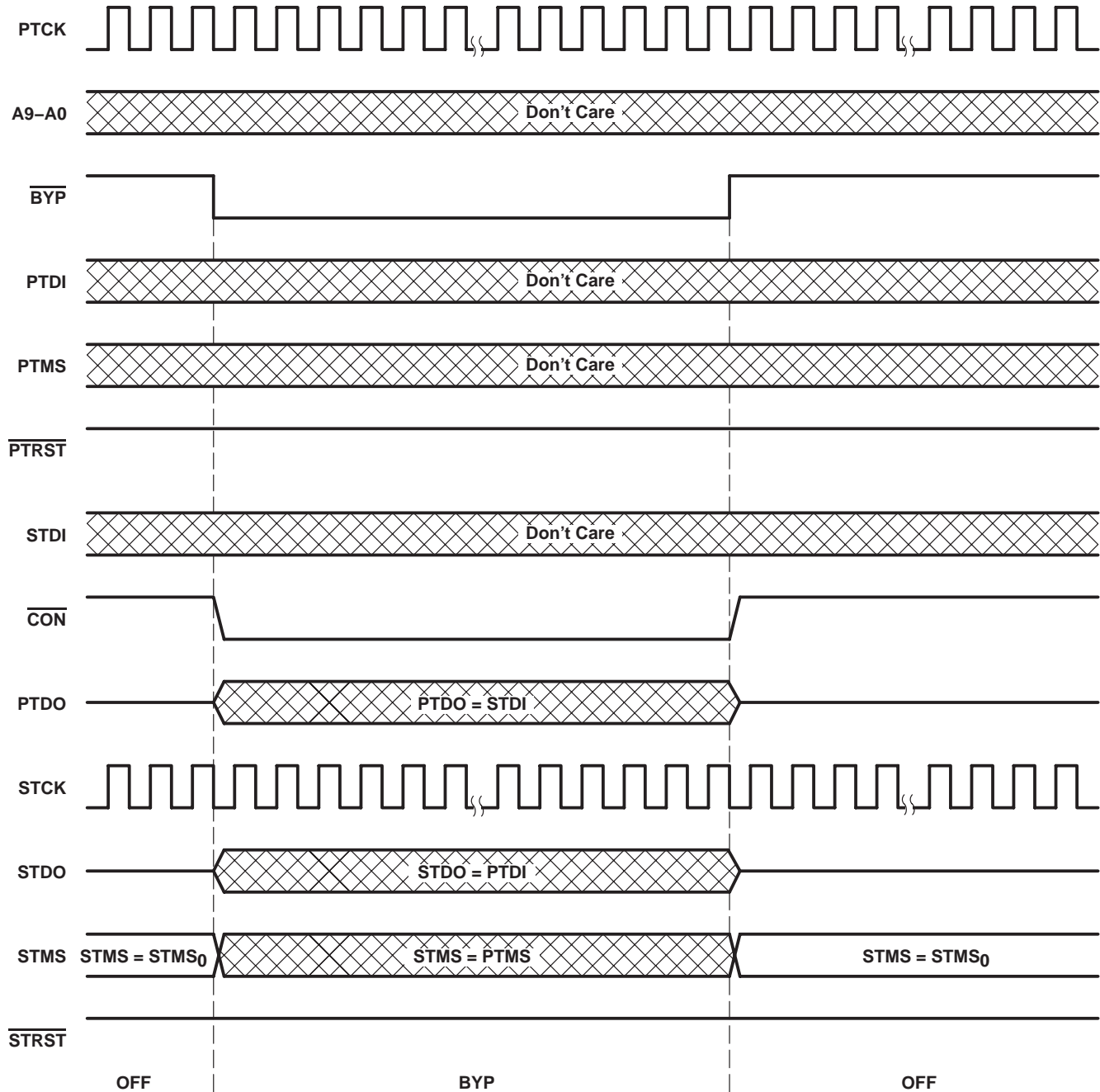


Figure 20. Protocol-Bypass Timing, Prior Connect Status = OFF

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asynchronous reset timing

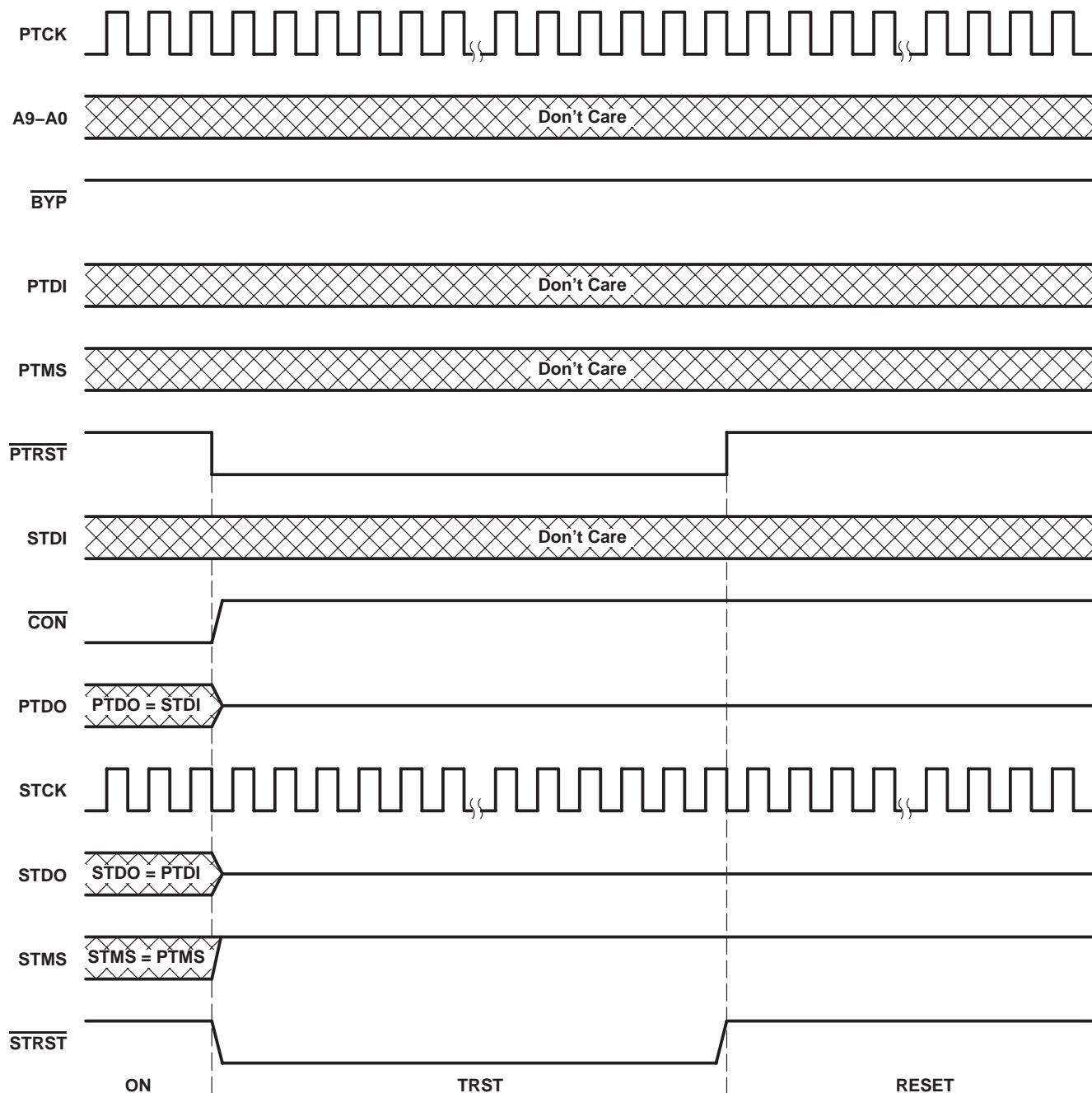


Figure 21. Asynchronous Reset Timing, Prior Connect Status = ON

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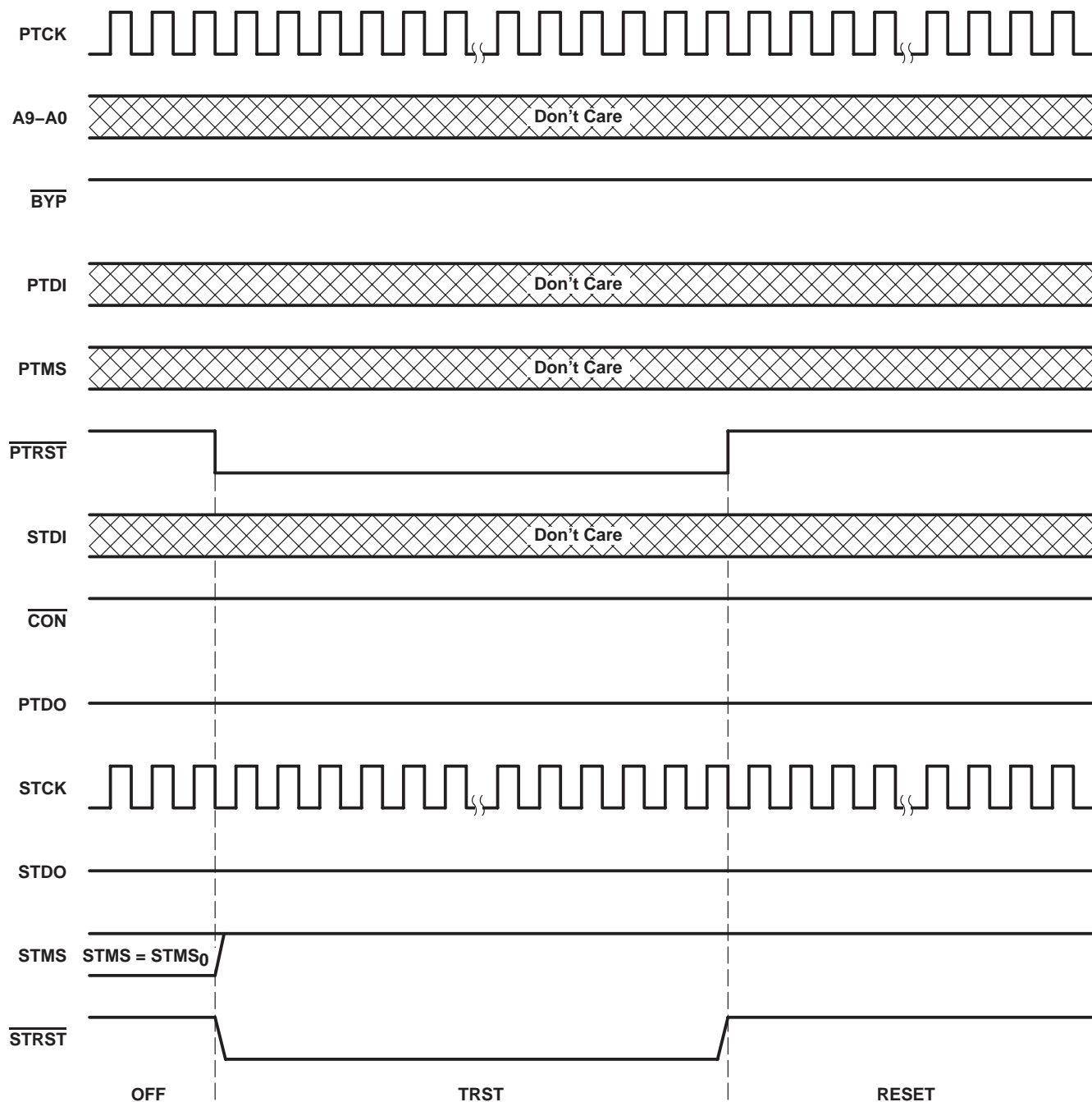


Figure 22. Asynchronous Reset Timing, Prior Connect Status = OFF

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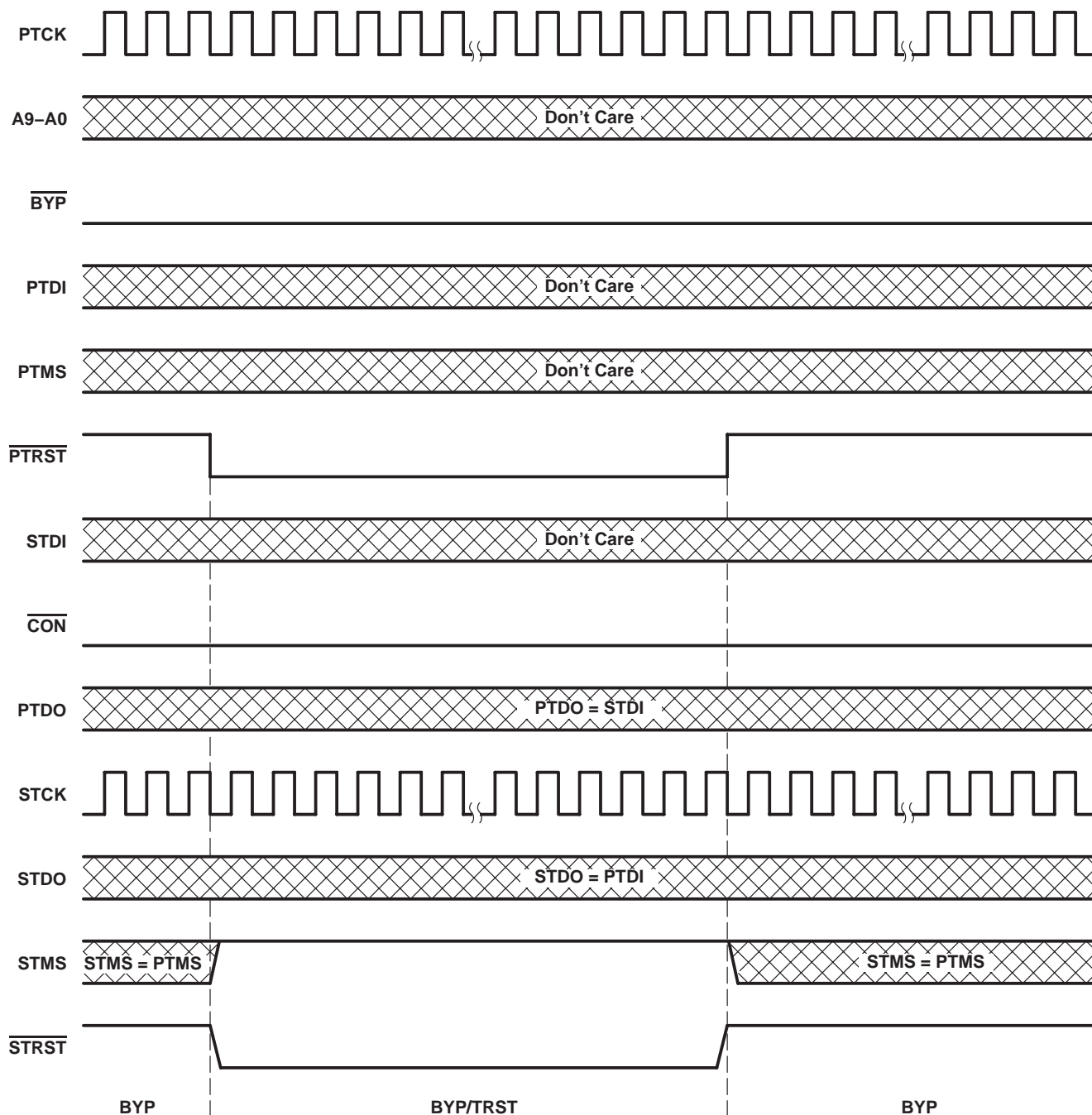


Figure 23. Asynchronous Reset Timing, $\overline{\text{BYP}} = \text{L}$

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_{OL}	128 mA
Current into any output in the high state, I_{OH} (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage		5.5	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		μs/V
T_A	Operating free-air temperature	–40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$	2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4	
		$I_{OL} = 32\text{ mA}$			0.5	
		$I_{OL} = 64\text{ mA}$			0.55	
I_I		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$			10	μA
	PTCK	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1	
I_{IH}	PTDI, PTMS, $\overline{\text{PTRST}}$	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$			1	μA
	A9-A0, $\overline{\text{BYP}}$, STDI				1	
I_{IL}	PTDI, PTMS, $\overline{\text{PTRST}}$	$V_{CC} = 3.6\text{ V}$, $V_I = \text{GND}$			-8	μA
	A9-A0, $\overline{\text{BYP}}$, STDI				-25	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$			± 100	μA
I_{OZH}	PTDO, STDO	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5	μA
I_{OZL}	PTDO, STDO	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5	μA
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$,			± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$	OFF, STCK = H, STMS = H			2	mA
		ON, PTDO = L, STCK = L, STDO = L, STMS = L			20	
		ON, PTDO = H, STCK = H, STDO = H, STMS = H			7	
		TRST, STCK = L			10	
ΔI_{CC}^\ddagger		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2	mA
C_i		$V_I = 3\text{ V or } 0$		3.5		pF
C_o		$V_O = 3\text{ V or } 0$		6.5		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

			MIN	MAX	UNIT
f _{clock} Clock frequency	PTCK	V _{CC} = 2.7 V		20	MHz
		V _{CC} = 3.3 V ± 0.3V		25	
t _w Pulse duration	BYP low [†]		8		ns
	PTCK high		20		
	PTCK low		12		
	PTRST low		9		
t _{su} Setup time	A9–A0 before PTCK↓ [‡]		10.2		ns
	PTDI before PTCK↑		10.1		
	PTMS before BYP↑↑		4		
	PTMS before PTCK↑		10		
t _h Hold time	A9–A0 after PTCK↓ [‡]		4		ns
	PTDI after PTCK↑		4		
	PTMS after BYP↑↑		4		
	PTMS after PTCK↑		4		

[†] In normal application of the ASP, such timing requirements with respect to $\overline{\text{BYP}}$ are met implicitly and, therefore, need not be considered.

[‡] These requirements apply only in the case in which the address inputs are changed during a shadow protocol. For normal application of the ASP, it is recommended that the address inputs remain static throughout any shadow protocols. In such cases, the timing of address inputs relative to PTCK need not be considered.

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			4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
--	--	--	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	-----

† The transitions at STMS are possible only when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _{PZH} [†]	$\overline{\text{BYP}}\downarrow$	PTDO	1.5	9	1.5	10.6	ns
t _{PZL}			1.5	10.1	1.5	11.9	
t _{PZH} [‡]	$\overline{\text{BYP}}\downarrow$	STDO	1.5	8.1	1.5	9.3	ns
t _{PZL}			1.5	9.2	1.5	10.7	
t _{PZH} [†]	PTCK \downarrow	PTDO	4	14.5	4	16.8	ns
t _{PZH} [‡]			4	15.8	4	18.4	ns
t _{PZL}	PTCK \downarrow	STDO	4	16.4	4	19.1	
t _{PHZ} [†]	$\overline{\text{BYP}}\uparrow$	PTDO	1.5	8.3	1.5	9.3	ns
t _{PLZ}			1.5	7.7	1.5	8.3	
t _{PHZ} [‡]	$\overline{\text{BYP}}\uparrow$	STDO	1.5	7.3	1.5	8.5	ns
t _{PLZ}			1.5	7.4	1.5	7.1	
t _{PHZ} [†]	PTCK \downarrow	PTDO	3	14	3	16.6	ns
t _{PLZ}			3	13.9	3	15.5	
t _{PHZ} [‡]	PTCK \downarrow	STDO	3.5	16.9	3.5	18.3	ns
t _{PLZ} [§]			3.5	13	3.5	15.1	
t _{PHZ} [†]	$\overline{\text{PTRST}}\downarrow$	PTDO	3.5	18.3	3.5	21.6	ns
t _{PLZ}			3.5	19.3	3.5	19.6	
t _{PHZ} [‡]	$\overline{\text{PTRST}}\downarrow$	STDO	4.5	18.2	4.5	21.4	ns
t _{PLZ}			4.5	20.6	4.5	23.4	

[†] In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.

[‡] In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.

[§] This parameter applies only in case of protocol result HARD ERROR.

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From Output Under Test

$C_L = 50 \text{ pF}$
(see Note A)

500Ω

500Ω

S1

6 V

Open

GND

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND

The diagram illustrates the timing characteristics of a CMOS inverter. It consists of three vertically stacked waveforms:

- Input:** A square wave switching between 0 V and 2.7 V. The transition region is marked with a 1.5 V level.
- Output (top):** The output of the inverter, which is a square wave switching between V_{OH} and V_{OL} . The transition region is also marked with a 1.5 V level.
- Output (bottom):** A second output waveform, identical to the first, showing the same switching behavior.

Propagation delays are indicated by horizontal double-headed arrows:

- t_{PLH} (Low-to-High delay): The time from the input rising to 1.5 V to the output rising to 1.5 V.
- t_{PHL} (High-to-Low delay): The time from the input falling to 1.5 V to the output falling to 1.5 V.

Output Control

Output Waveform 1
S1 at 6 V
(see Note B)

Output Waveform 2
S1 at Open
(see Note B)

Timing parameters: t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}

Voltage levels: 2.7 V, 1.5 V, 0 V, 3 V, $V_{OL} + 0.3 V$, V_{OL} , $V_{OH} - 0.3 V$, V_{OH} , $\approx 0 V$

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVT8996IPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04644-01YE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVT8996-EP :

- Catalog: [SN74LVT8996](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT8996IPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT8996IPWREP	TSSOP	PW	24	2000	346.0	346.0	33.0

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