FAIRCHILD
SEMICONDUCTOR®

September 2009

FDMS7656AS

N-Channel PowerTrench® SyncFET™

30 V, 49 A, 1.8 mΩ

Features

- Max $r_{DS(on)}$ = 1.8 mΩ at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 1.9 mΩ at V_{GS} = 7 V, I_D = 27 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

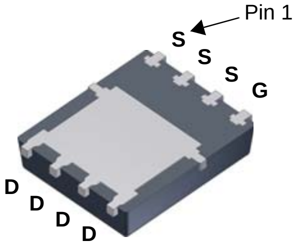
The FDMS7656AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

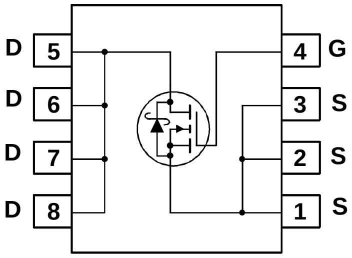
Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification

Top

Bottom





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25 °C	49	A
	-Continuous (Silicon limited) T_C = 25 °C	194	
	-Continuous T_A = 25 °C (Note 1a)	31	
	-Pulsed	180	
dv/dt	MOSFET dv/dt	1.3	V/ns
E_{AS}	Single Pulse Avalanche Energy (Note 3)	242	mJ
P_D	Power Dissipation T_C = 25 °C	96	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

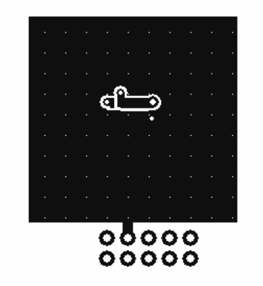
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7656AS	FDMS7656AS	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

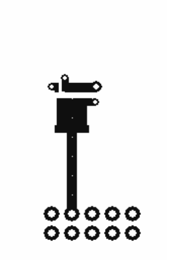
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 30 A		1.3	1.8	mΩ
		V_{GS} = 7 V, I_D = 27 A		1.5	1.9	
		V_{GS} = 4.5 V, I_D = 25 A		1.6	2.0	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125 °C		1.8	2.5	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 30 A		161		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		6545	8705	pF
C_{oss}	Output Capacitance			2465	3280	pF
C_{rss}	Reverse Transfer Capacitance			210	315	pF
R_g	Gate Resistance			0.5	1.1	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 30 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		22	35	ns
t_r	Rise Time			12	21	ns
$t_{d(off)}$	Turn-Off Delay Time			50	80	ns
t_f	Fall Time			7	13	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V V_{DD} = 15 V, I_D = 30 A		95	133	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		43	60	nC
Q_{gs}	Gate to Source Charge			18.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			9.1		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.37	0.7	V
		V_{GS} = 0 V, I_S = 30 A (Note 2)		0.74	1.2	
t_{rr}	Reverse Recovery Time	I_F = 30 A, di/dt = 300 A/μs		50	81	ns
Q_{rr}	Reverse Recovery Charge			84	136	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 242 mJ is based on starting T_J = 25 °C, L = 1 mH, I_{AS} = 22 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 34 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

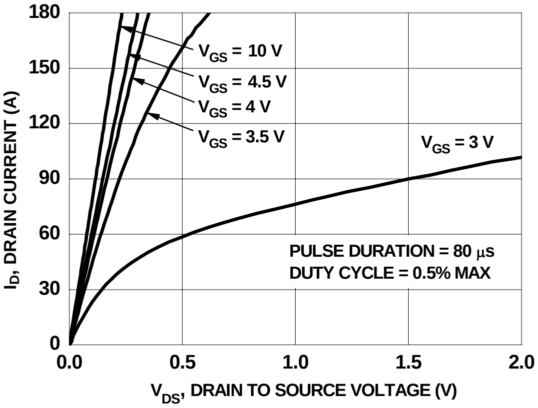


Figure 1. On Region Characteristics

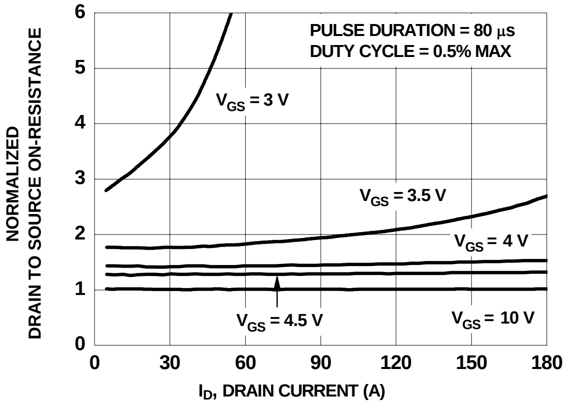


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

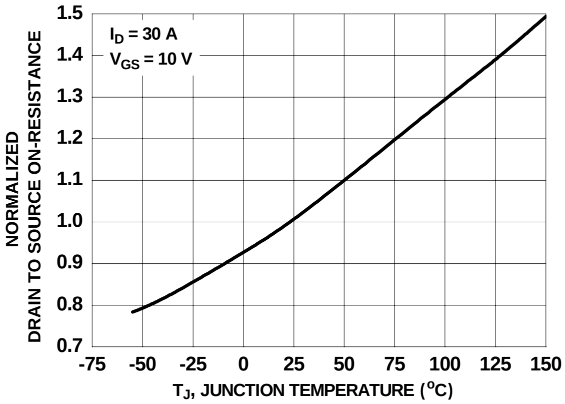


Figure 3. Normalized On Resistance vs Junction Temperature

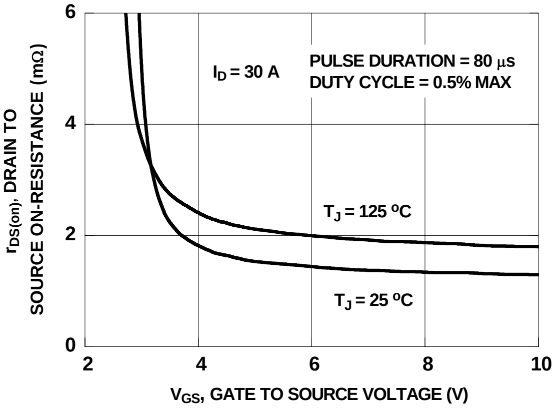


Figure 4. On-Resistance vs Gate to Source Voltage

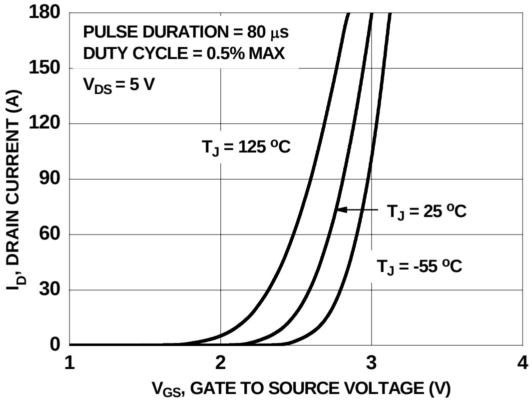


Figure 5. Transfer Characteristics

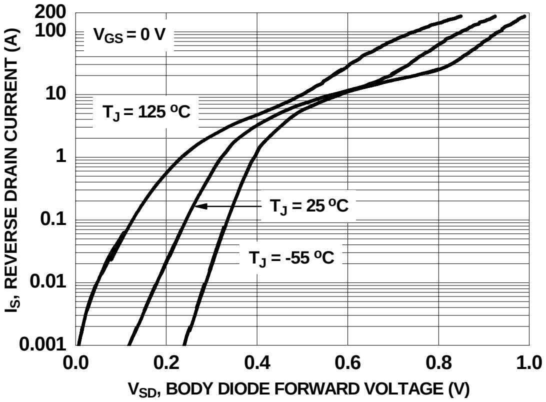


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

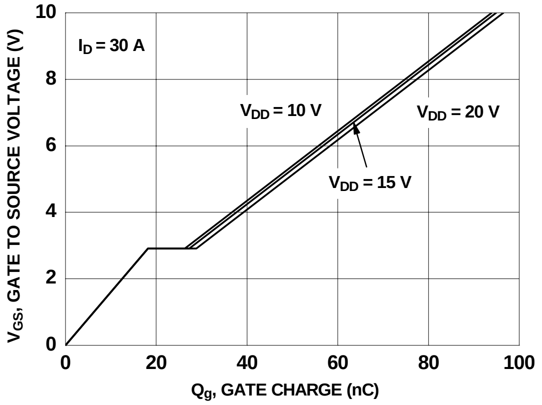


Figure 7. Gate Charge Characteristics

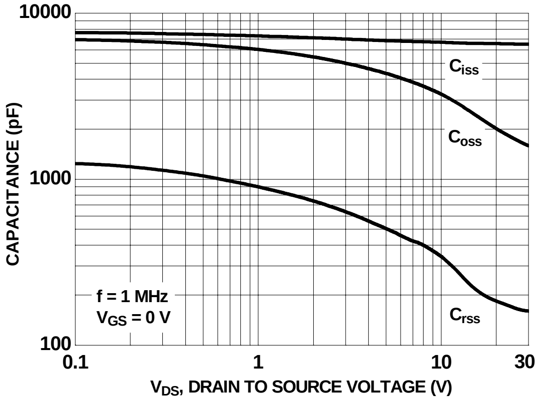


Figure 8. Capacitance vs Drain to Source Voltage

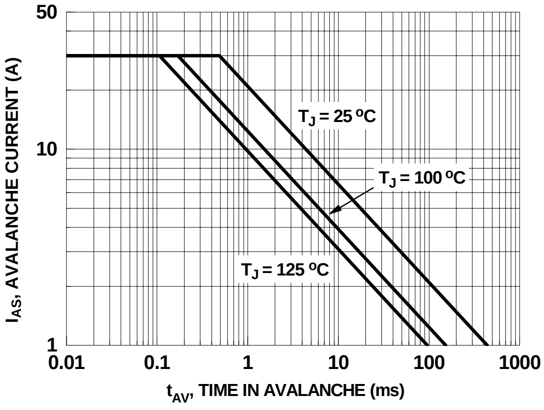


Figure 9. Unclamped Inductive Switching Capability

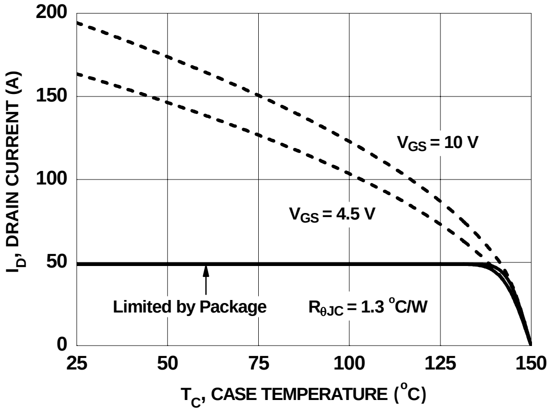


Figure 10. Maximum Continuous Drain Current vs Case Temperature

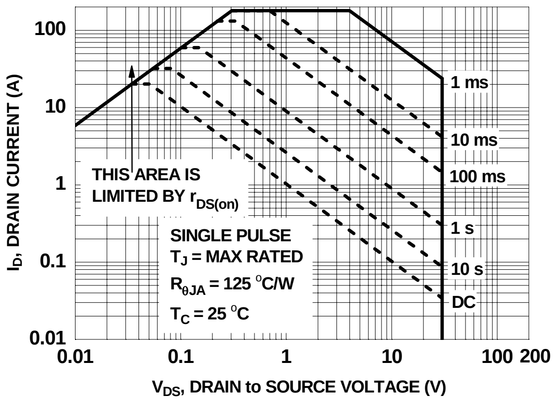


Figure 11. Forward Bias Safe Operating Area

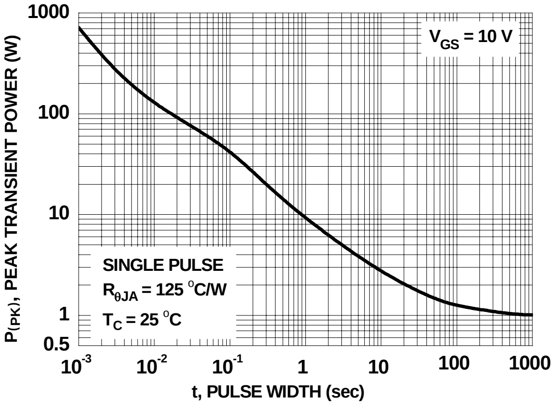


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

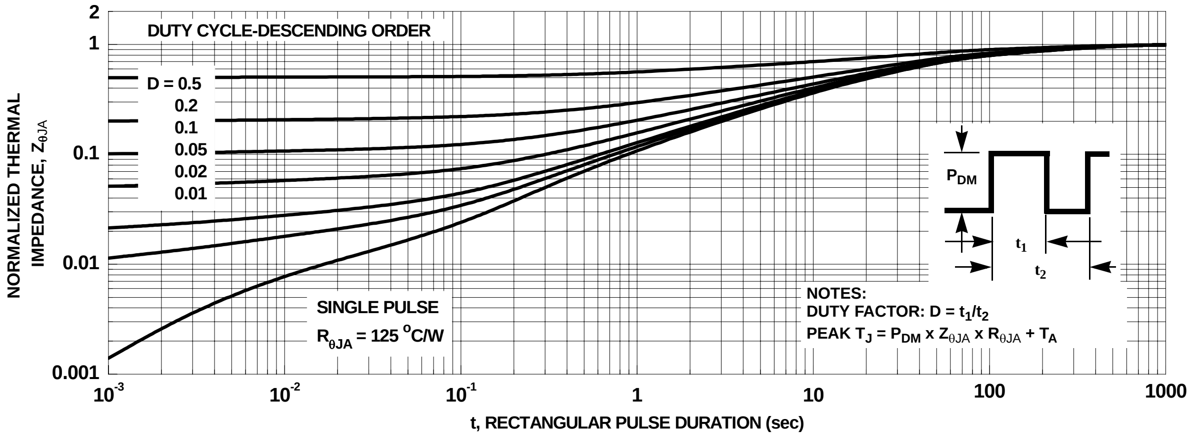


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverses recovery characteristic of the FDMS7656AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

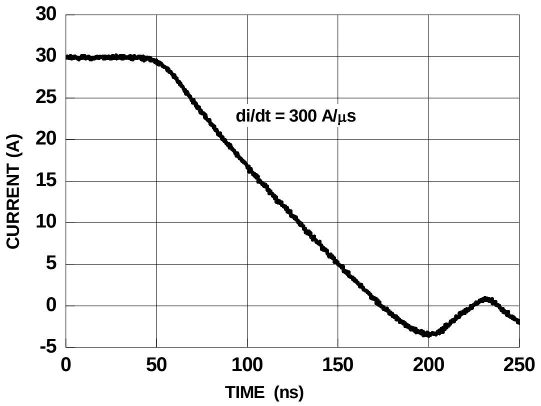


Figure 14. FDMS7656AS SyncFET body diode reverse recovery characteristic

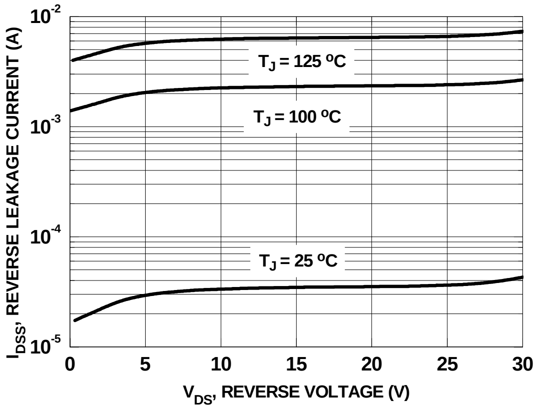
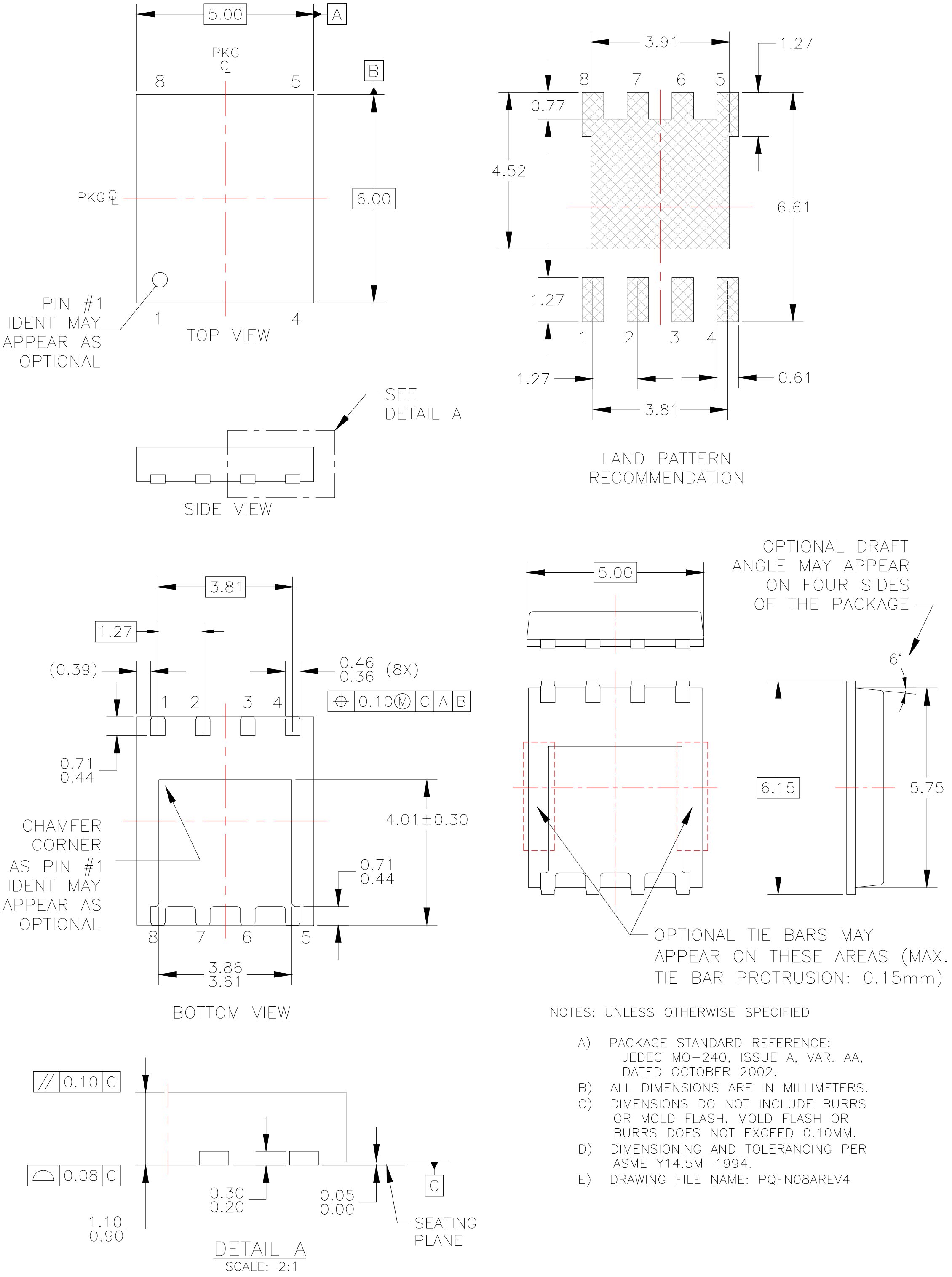


Figure 15. SyncFET body diode reverses leakage versus drain-source voltage

Dimensional Outline and Pad Layout



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JEDEC MO-240, ISSUE A, VAR. AA,
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS
OR MOLD FLASH. MOLD FLASH OR
BURRS DOES NOT EXCEED 0.10MM.
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