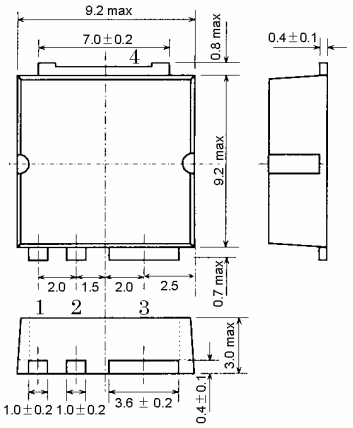
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIII)

2SK3842

Switching Regulator Applications, DC-DC Converter and Motor Drive Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ =4.6 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 93 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 60 V)
- Enhancement model: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-97
TOSHIBA	2-9F1B

Weight: 0.74 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	60	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	75	A
	Pulse(t ≦ 1 ms) (Note 1)	I_{DP}	300	
Drain power dissipation (Tc = 25°C)		P_D	125	W
Single pulse avalanche energy (Note 2)		E_{AS}	322	mJ
Avalanche current		I_{AR}	75	A
Repetitive avalanche energy (Note 3)		E_{AR}	12.5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	1.0	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

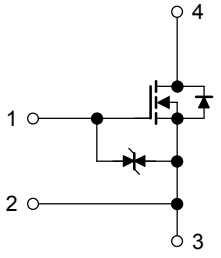
Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 78 μH, R_G = 25 Ω, I_{AR} = 75 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

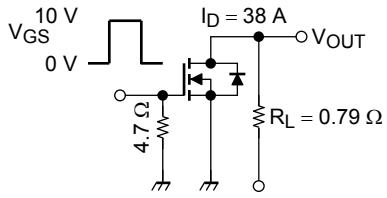
This transistor is an electrostatic-sensitive device. Please handle with caution.

Circuit Configuration

Notice:
Please use the S1 pin for gate input signal return. Make sure that the main current flows into S2 pin.



Electrical Characteristics (Note 4) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	60	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	35	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 38 A	—	4.6	5.8	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 38 A	46	93	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	12400	—	pF
Reverse transfer capacitance		C_{rss}		—	700	—	
Output capacitance		C_{oss}		—	1100	—	
Switching time	Rise time	t_r		—	18	—	ns
	Turn-ON time	t_{on}		—	45	—	
	Fall time	t_f		—	35	—	
	Turn-OFF time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	200	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 48 V, V_{GS} = 10 V, I_D = 75 A	—	196	—	nC
Gate-source charge		Q_{gs}		—	148	—	
Gate-drain (“miller”) charge		Q_{gd}		—	48	—	

Note 4: Connect the S1 and S2 pins together, and ground them except during switching time measurement.

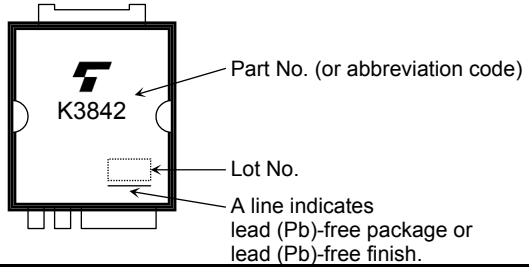
Source-Drain Ratings and Characteristics (Note 5) (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1, Note 5)	$I_{DR}1$	—	—	—	75	A
Pulse drain reverse current (Note 1,Note 5)	$I_{DRP}1$	—	—	—	300	A
Continuous drain reverse current (Note 1, Note 5)	$I_{DR}2$	—	—	—	1	A
Pulse drain reverse current (Note 1,Note 5)	$I_{DRP}2$	—	—	—	4	A
Forward voltage (diode)	V_{DS2F}	$I_{DR}1$ = 75 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 75 A, V_{GS} = 0 V, dI_{DR}/dt = 50 A/μs	—	70	—	ns
Reverse recovery charge	Q_{rr}		—	77	—	nC

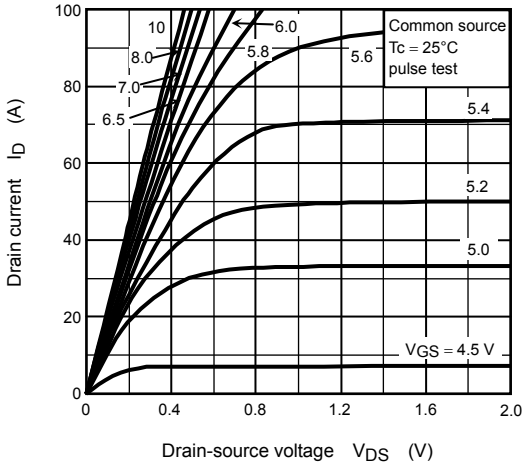
Note 5: Current flowing between the drain and the S1 pin, when open the S2 pin is left open.

Unless otherwise specified, connect the S1 and S2 pins together, and ground them.

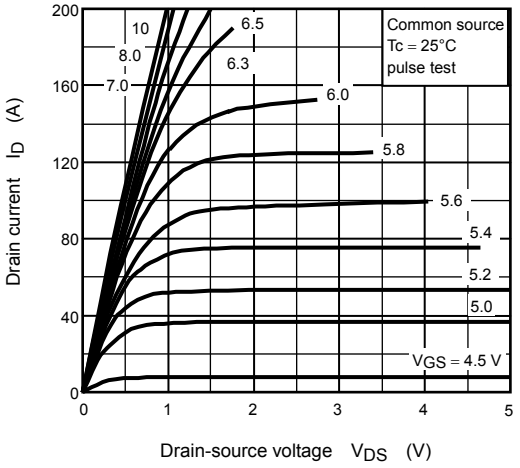
Marking



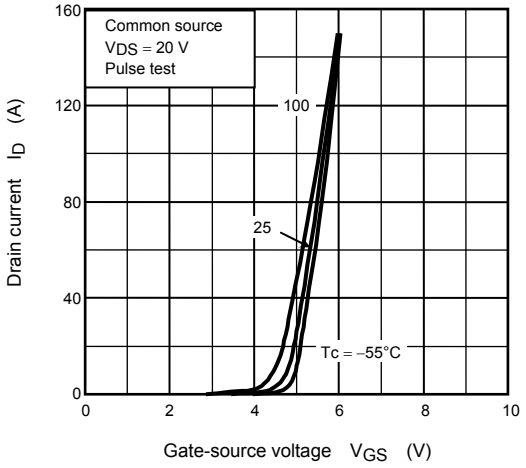
$I_D - V_{DS}$



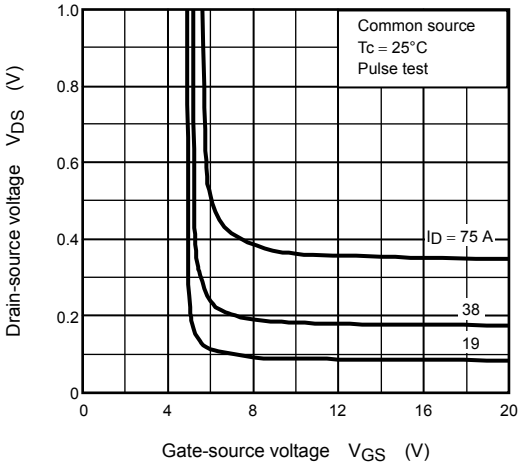
$I_D - V_{DS}$



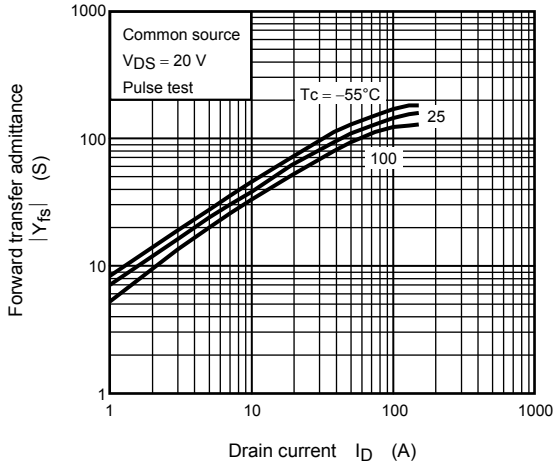
$I_D - V_{GS}$



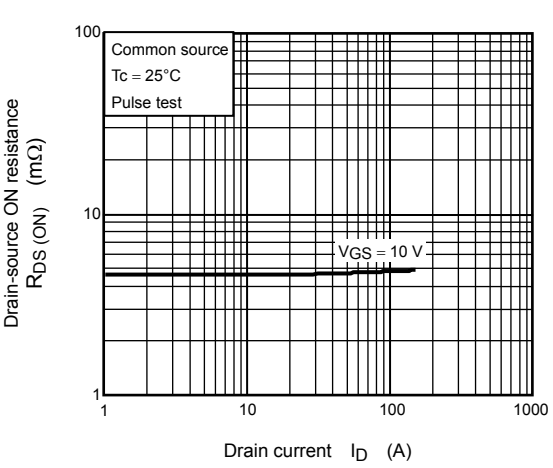
$V_{DS} - V_{GS}$



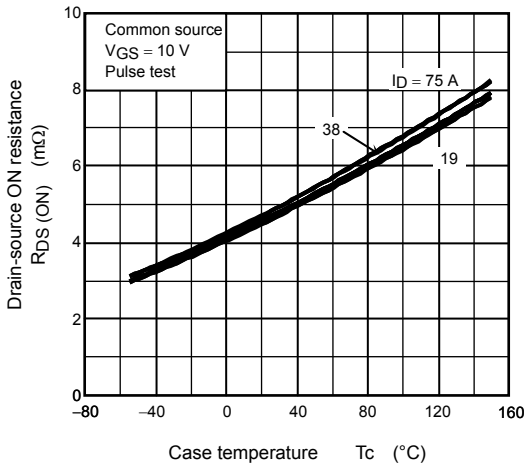
$|Y_{fs}| - I_D$



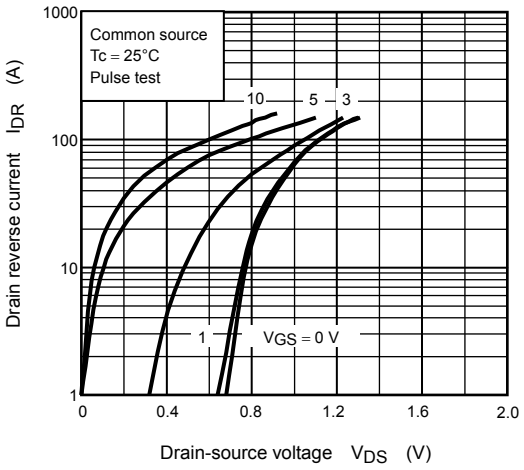
$R_{DS\ (ON)} - I_D$



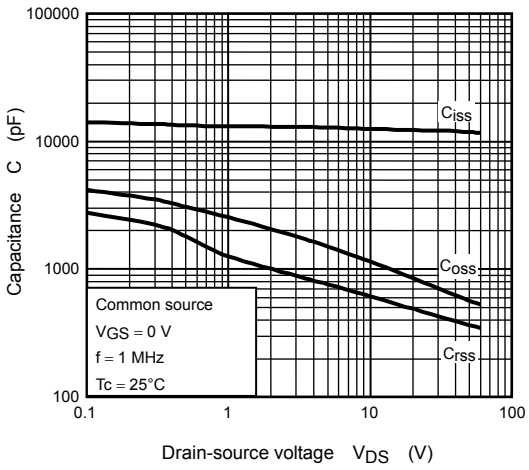
$R_{DS\ (ON)}$ – Tc



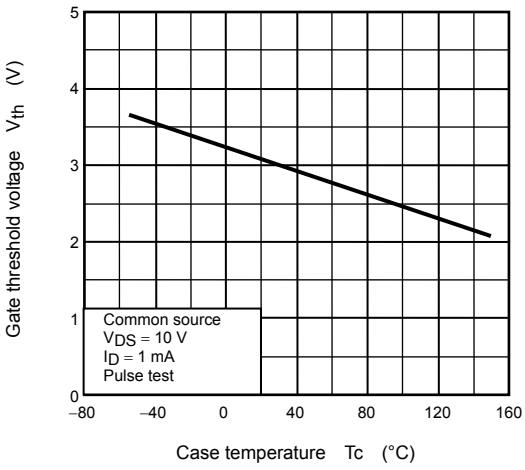
I_{DR} – V_{DS}



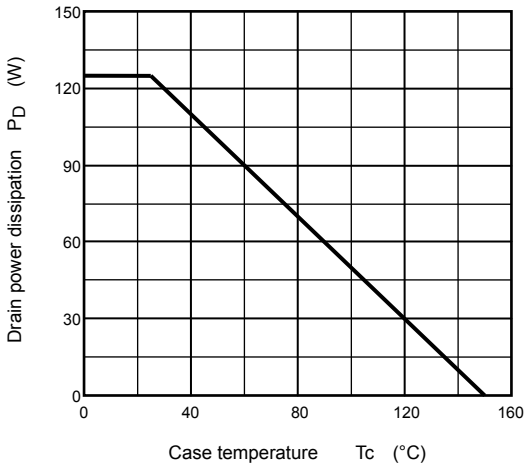
Capacitance – V_{DS}



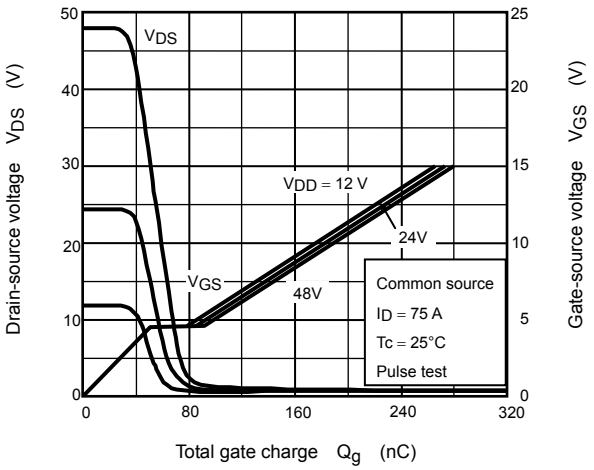
V_{th} – Tc



P_D – Tc



Dynamic input/output characteristics



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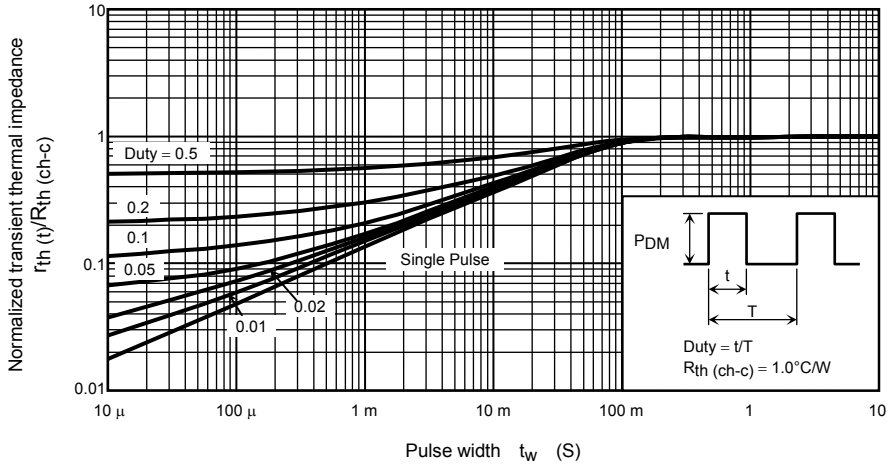
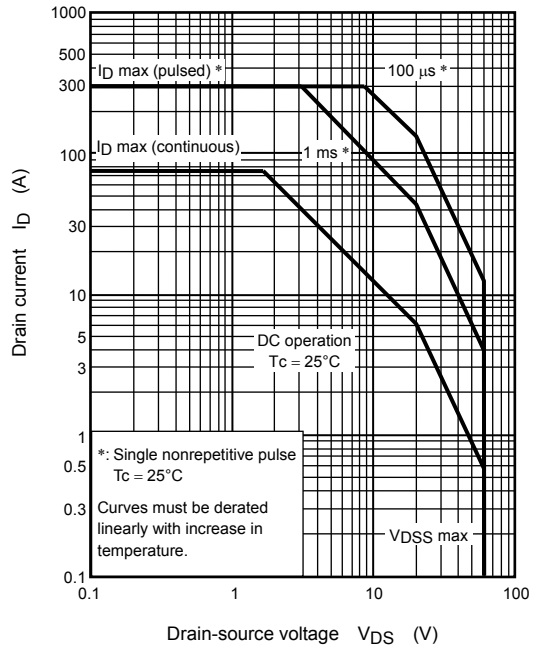
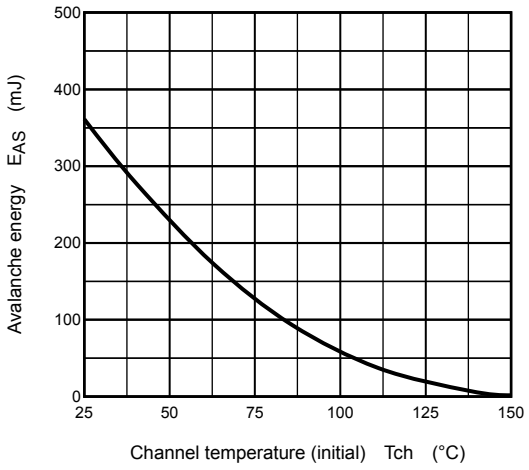
$r_{th} - t_w$

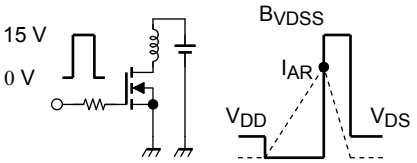


Safe operating area



$E_{AS} - T_{ch}$





Test circuit　　Wave form

$R_G = 25\ \Omega$
$V_{DD} = 25$ V, L = 78 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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