

SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS540D – OCTOBER 1995 – REVISED OCTOBER 2003

查询"5962-8755501VRA"供应商

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

description/ordering information

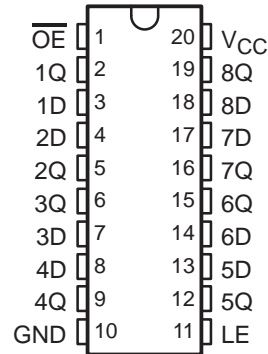
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

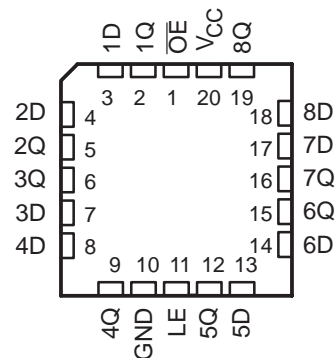
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC373 . . . J OR W PACKAGE
SN74AC373 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC373N	SN74AC373N
	SOIC – DW	Tube	SN74AC373DW	AC373
		Tape and reel	SN74AC373DWR	
	SOP – NS	Tape and reel	SN74AC373NSR	AC373
	SSOP – DB	Tape and reel	SN74AC373DBR	AC373
	TSSOP – PW	Tube	SN74AC373PW	AC373
		Tape and reel	SN74AC373PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54AC373J	SNJ54AC373J
	CFP – W	Tube	SNJ54AC373W	SNJ54AC373W
	LCCC – FK	Tube	SNJ54AC373FK	SNJ54AC373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS999E "9082-8755-01" V1.0 01/95 © 2003 德州仪器

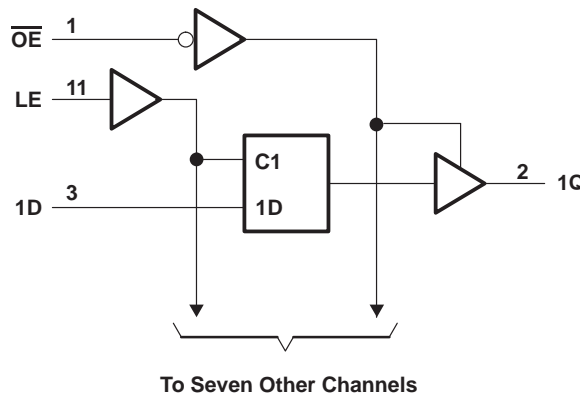
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

[查询"5962-8755501VRA"供应商](#)

SCAS540D – OCTOBER 1995 – REVISED OCTOBER 2003

recommended operating conditions (see Note 3)

		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	6	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 3 V		2.1		V
		V _{CC} = 4.5 V		3.15		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 3 V		0.9		V
		V _{CC} = 4.5 V		1.35		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V		-12		mA
		V _{CC} = 4.5 V		-24		
		V _{CC} = 5.5 V		-24		
I _{OL}	Low-level output current	V _{CC} = 3 V		12		mA
		V _{CC} = 4.5 V		24		
		V _{CC} = 5.5 V		24		
Δt/Δv	Input transition rise or fall rate	8		8		ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		0.1		V
		4.5 V	0.1			0.1		0.1		
		5.5 V	0.1			0.1		0.1		
	I _{OL} = 12 mA	3 V	0.36			0.5		0.44		
		4.5 V	0.36			0.5		0.44		
		5.5 V	0.36			0.5		0.44		
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±0.25			±5		±2.5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	4			80		40		μA
C _i	V _I = V _{CC} or GND	5 V	4.5							pF



SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS996 "9062-8755-01" VISA "0105" 2003

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5.5		6.5		6		ns
t_{su}	Setup time, data before LE↓	5.5		6.5		6		ns
t_h	Hold time, data after LE↓	1		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		5		4.5		ns
t_{su}	Setup time, data before LE↓	4		5		4.5		ns
t_h	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	13.0	1	16	1.5	14.5	
t_{PLH}	LE	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	12.5	1	15	1.5	14	
t_{PZH}	\overline{OE}	Q	1.5	9	11.5	1	14	1	13	ns
t_{PZL}			1.5	8.5	11.5	1	13.5	1	13	
t_{PHZ}	\overline{OE}	Q	1.5	10	12.5	1	16	1	14.5	ns
t_{PLZ}			1.5	8	11.5	1	13	1	12.5	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

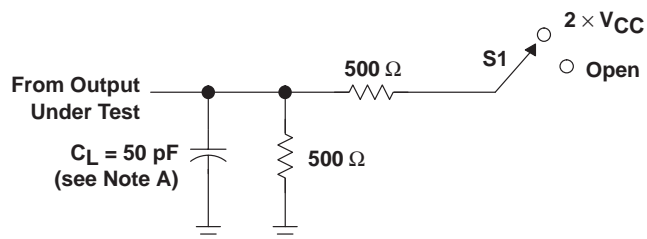
PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7	9.5	1	11.5	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11.5	1.5	10.5	
t_{PLH}	LE	Q	1.5	7.5	9.5	1	12	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11	1.5	10.5	
t_{PZH}	\overline{OE}	Q	1.5	7	8.5	1	10.5	1	9.5	ns
t_{PZL}			1.5	6.5	8.5	1	10	1	9.5	
t_{PHZ}	\overline{OE}	Q	1.5	8	11	1	13.5	1	12.5	ns
t_{PLZ}			1.5	6.5	8.5	1	10.5	1	10	

operating characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 pF$, $f = 1 MHz$	40	pF

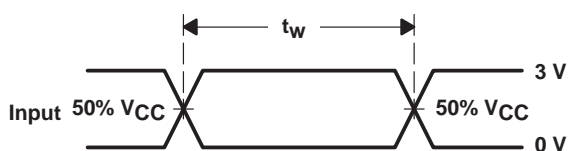


PARAMETER MEASUREMENT INFORMATION

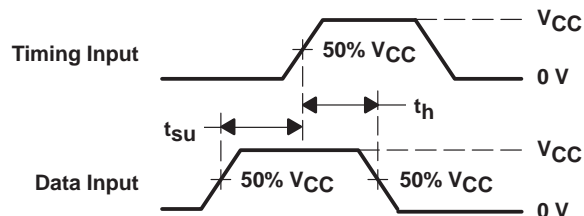


LOAD CIRCUIT

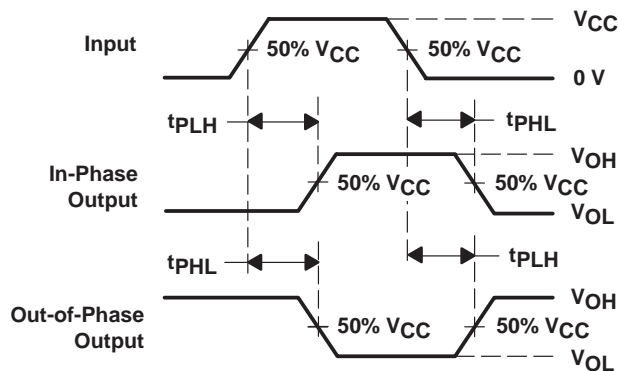
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



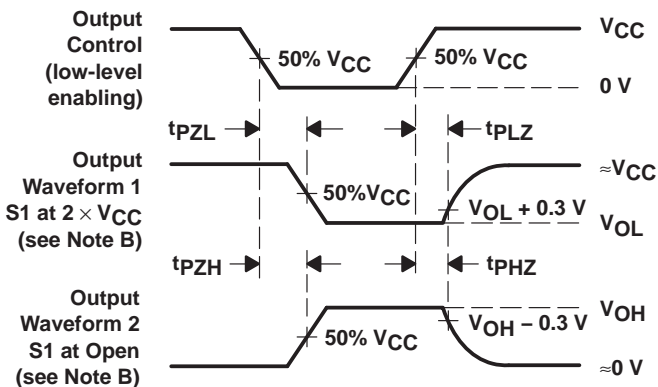
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-87555012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8755501RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8755501SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
5962-8755501VRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8755501VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN74AC373DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74AC373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AC373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54AC373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AC373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AC373W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

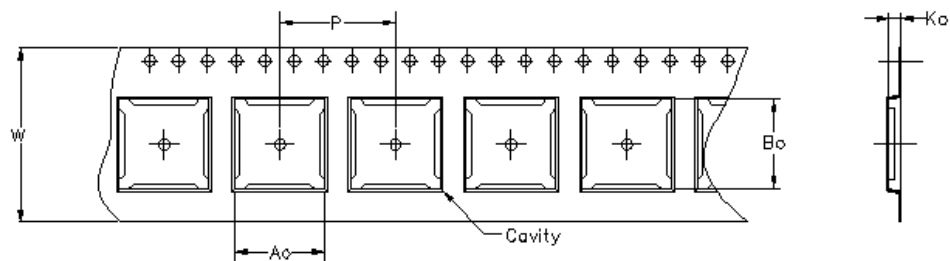
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

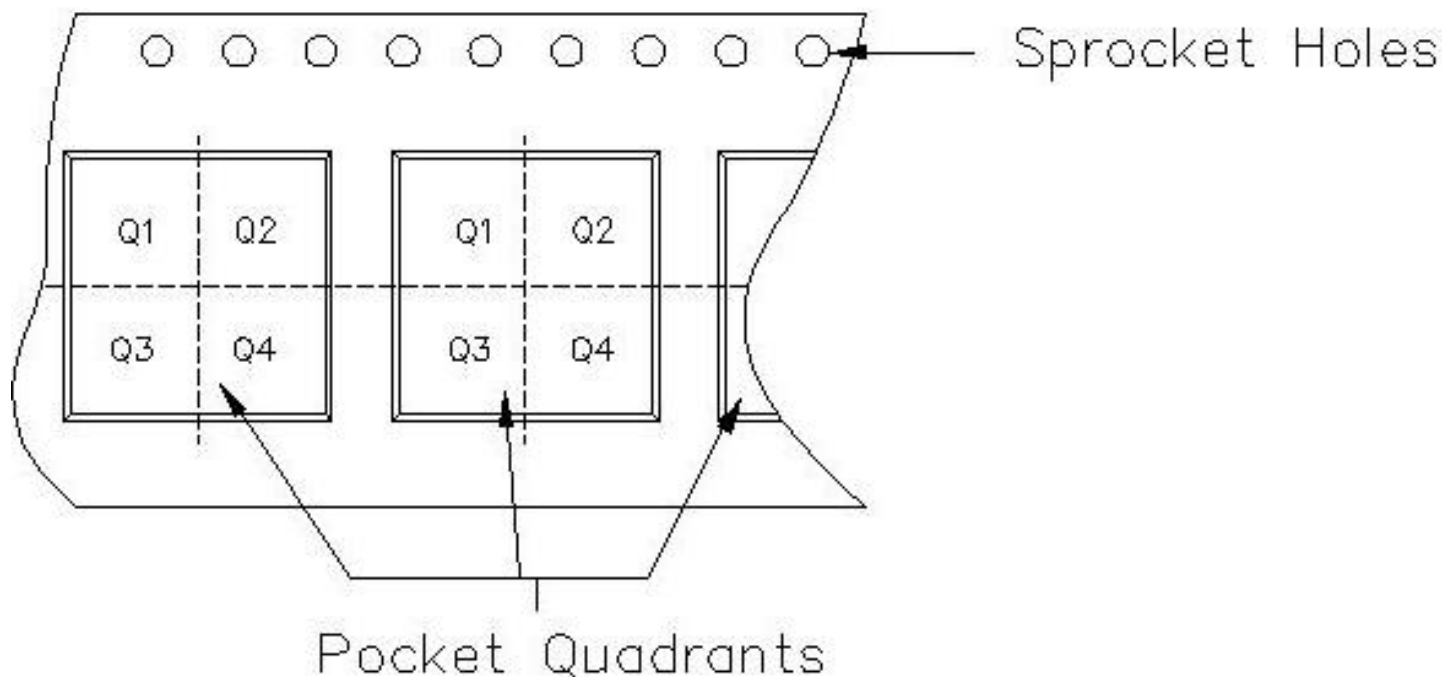
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



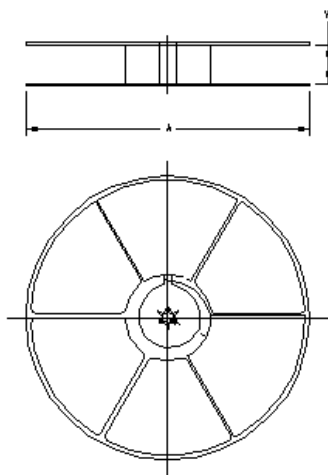
Carrier tape design is defined largely by the component length, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.

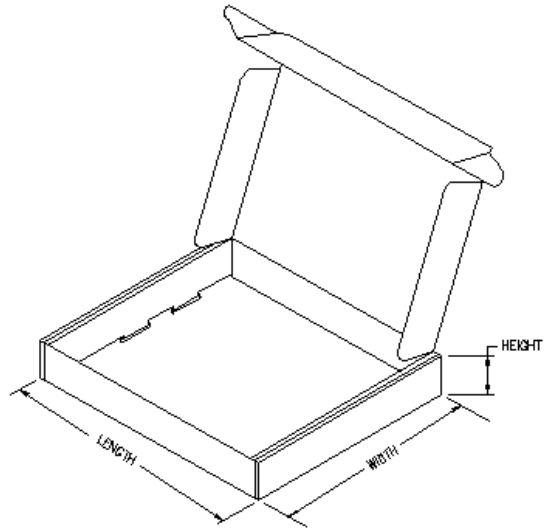


TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373DBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74AC373DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74AC373NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74AC373PWR	PW	20	MLA	330	16	6.95	7.1	1.6	8	16	Q1

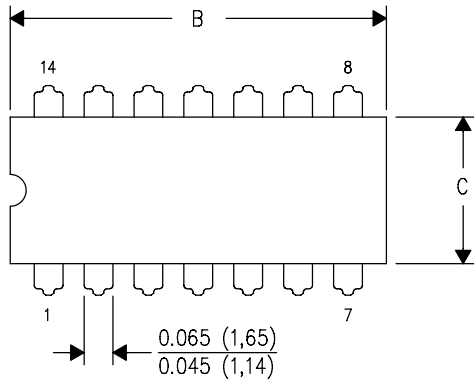

TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AC373DBR	DB	20	MLA	333.2	333.2	28.58
SN74AC373DWR	DW	20	MLA	333.2	333.2	31.75
SN74AC373NSR	NS	20	MLA	333.2	333.2	31.75
SN74AC373PWR	PW	20	MLA	333.2	333.2	28.58

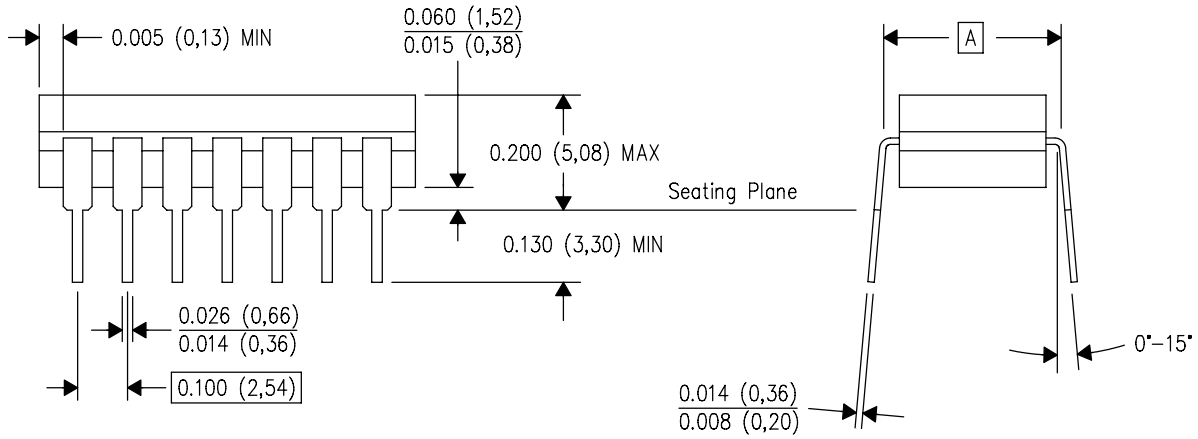


J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

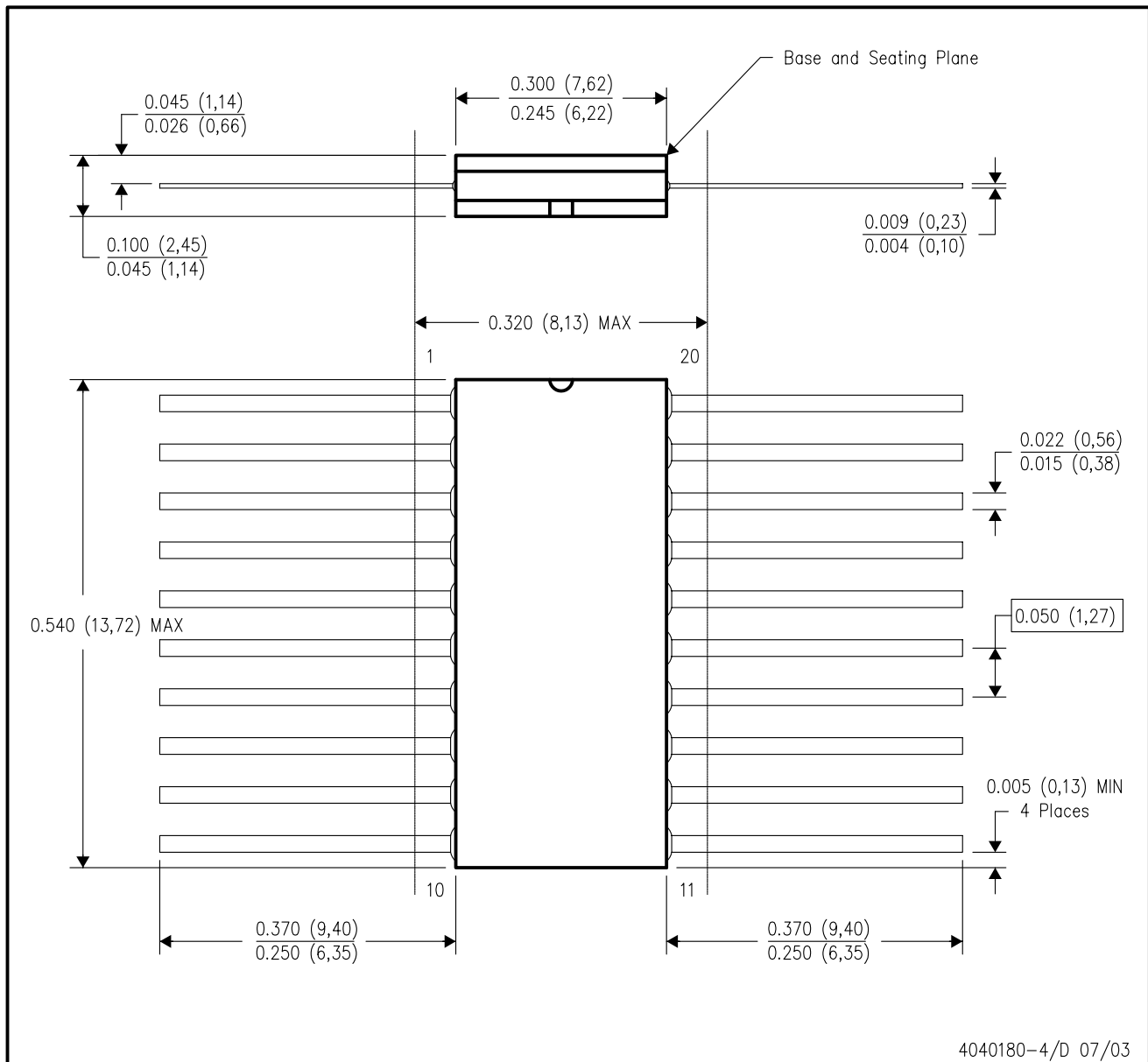


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

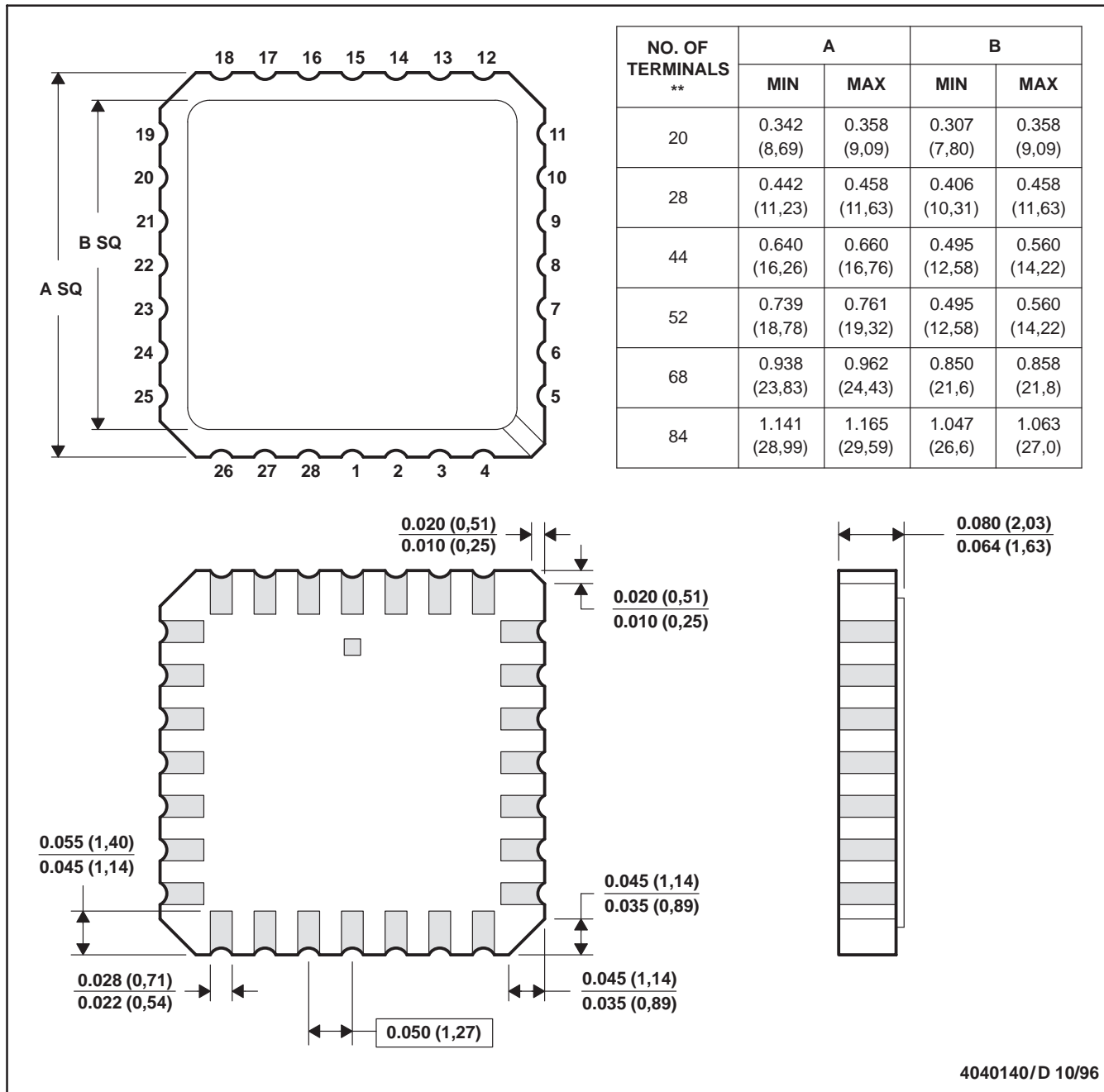


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

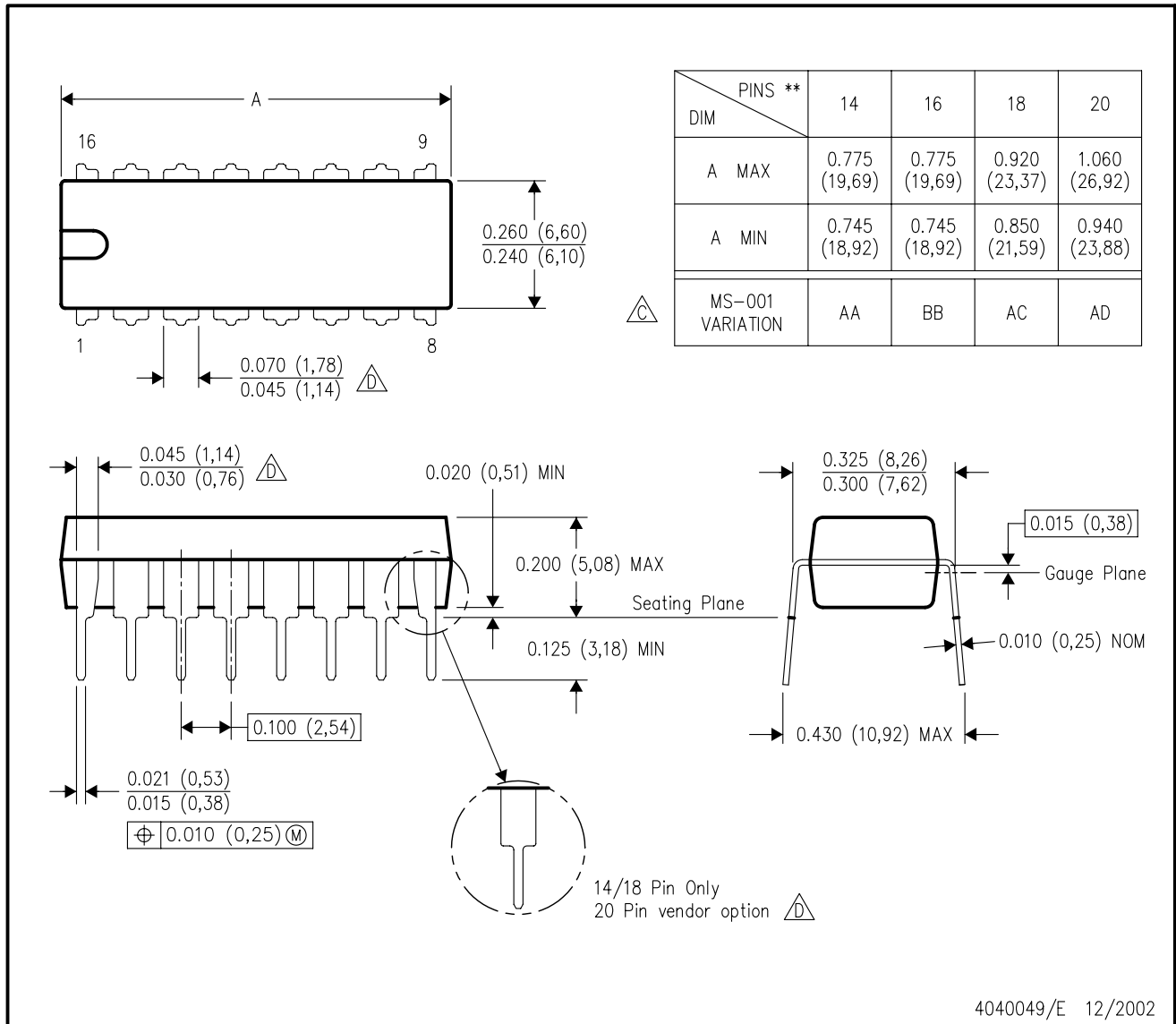
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

[查询"5962-8755501VRA"供应商](#)

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

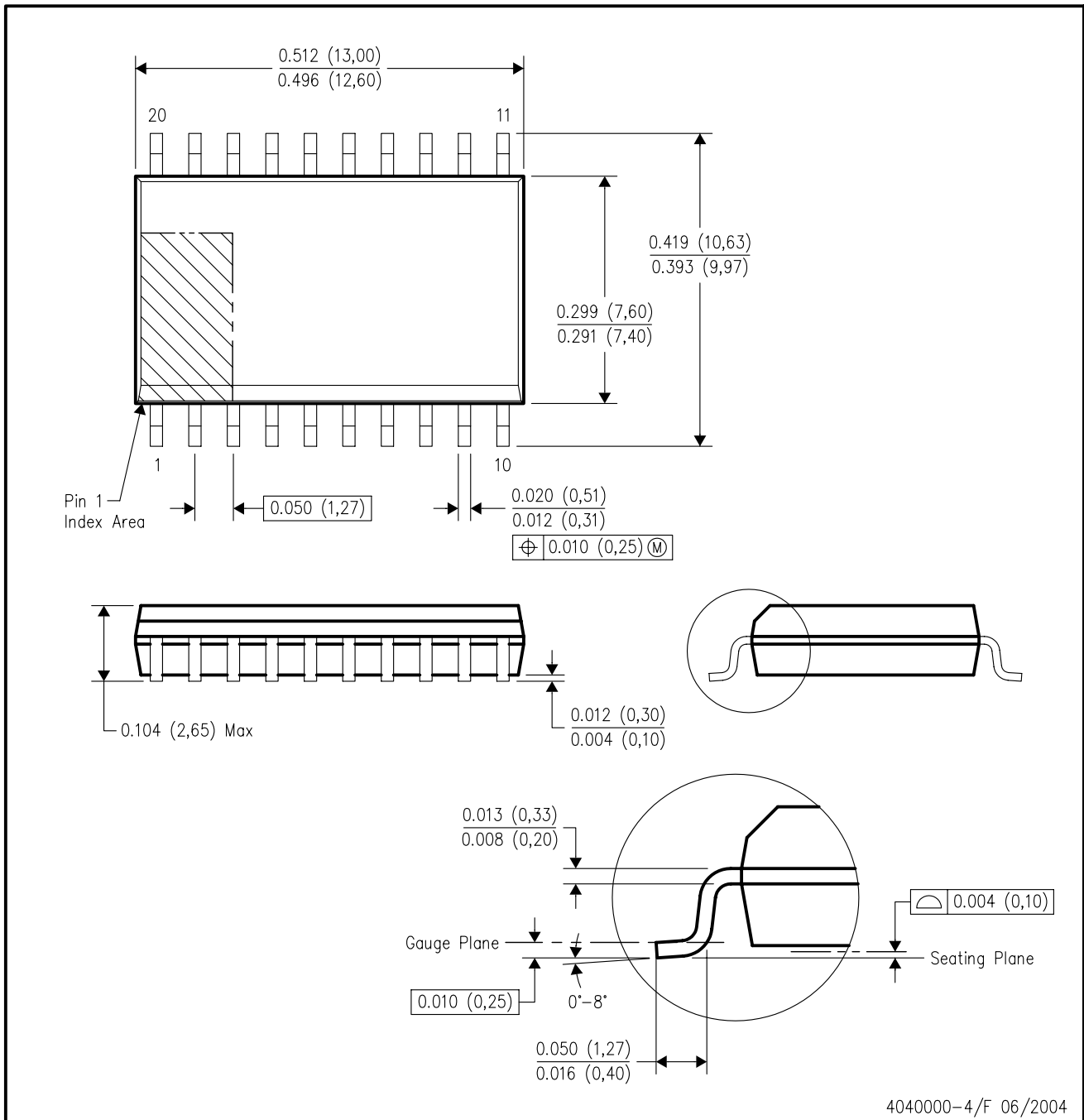


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



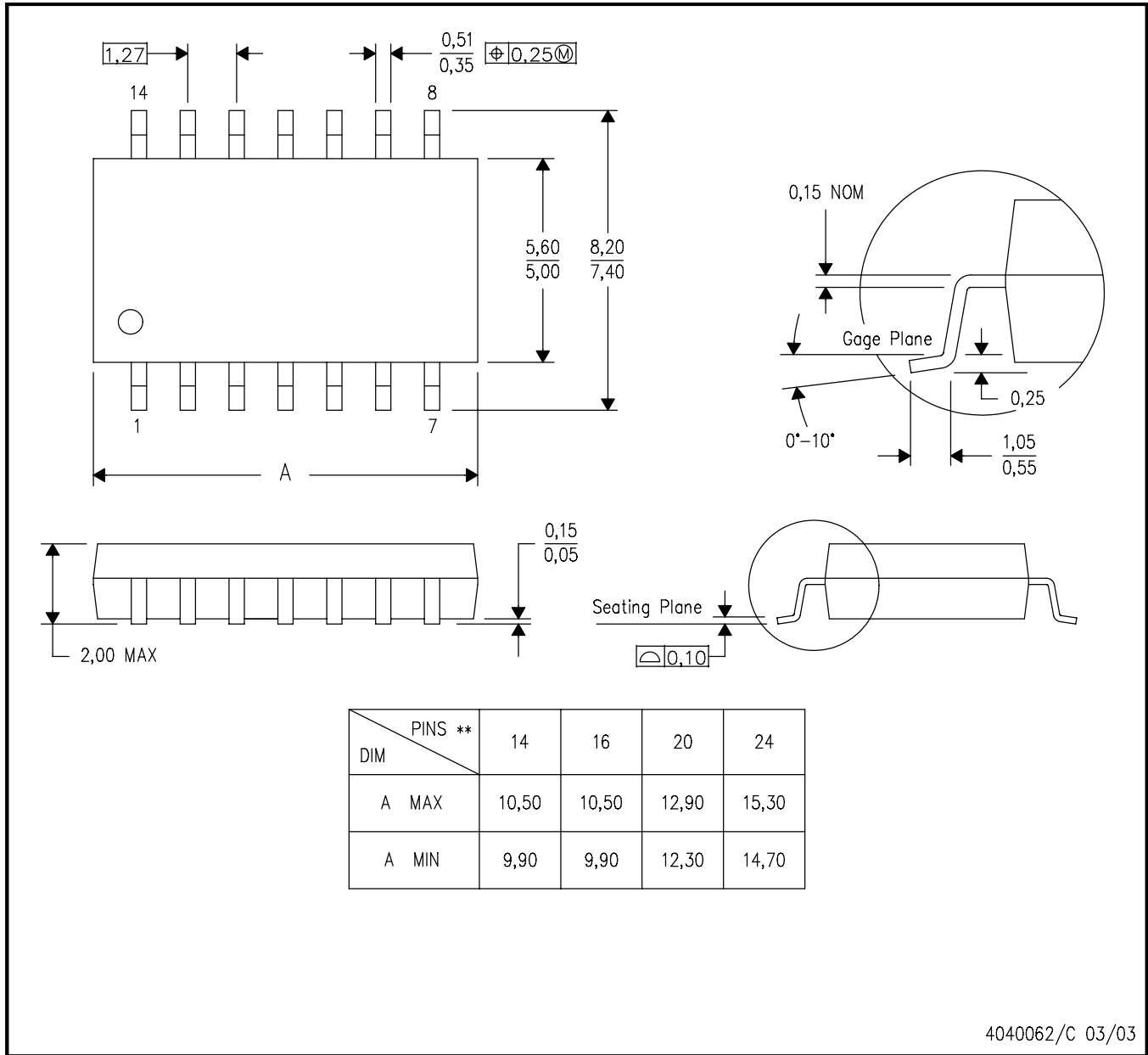
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

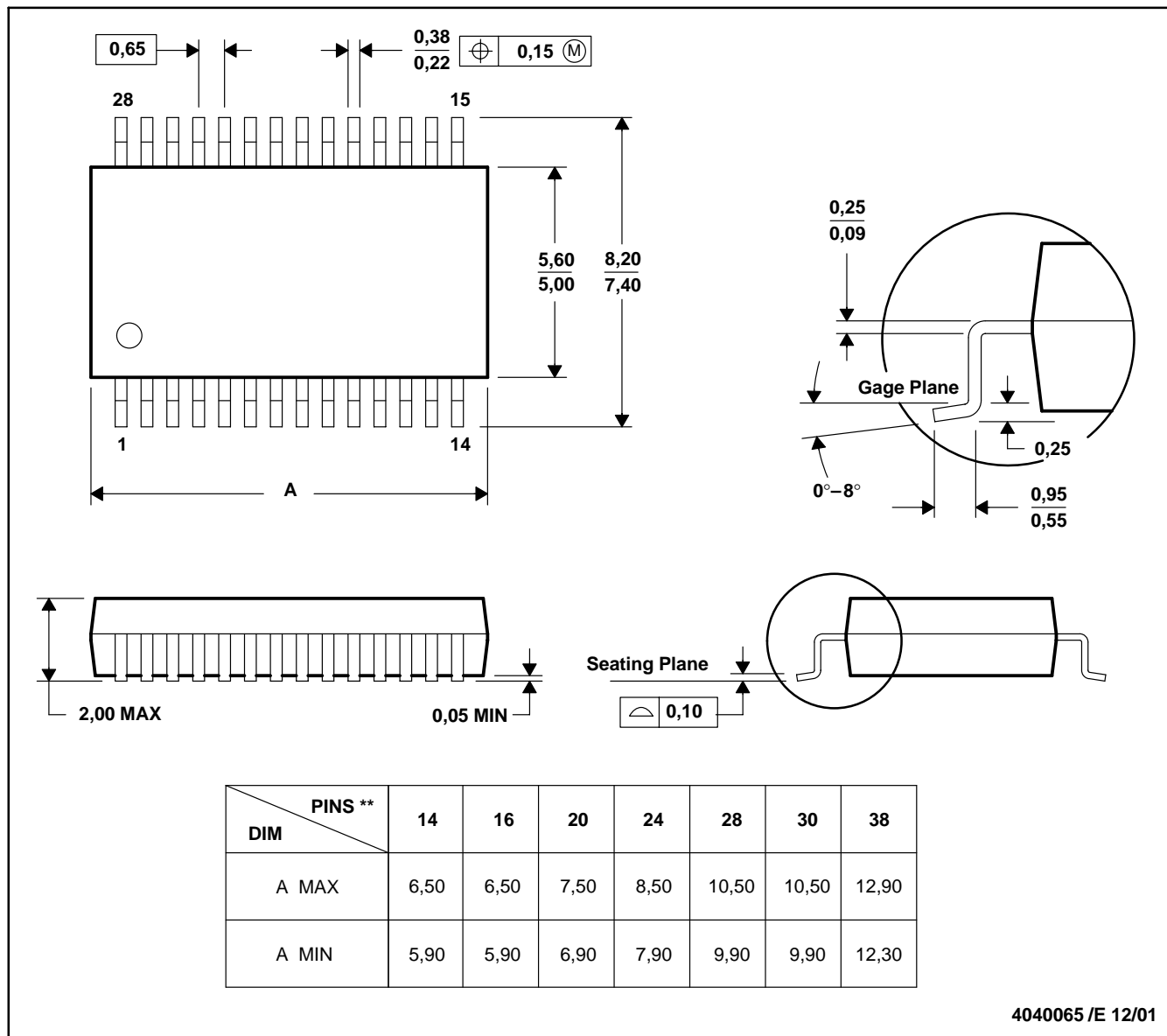


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

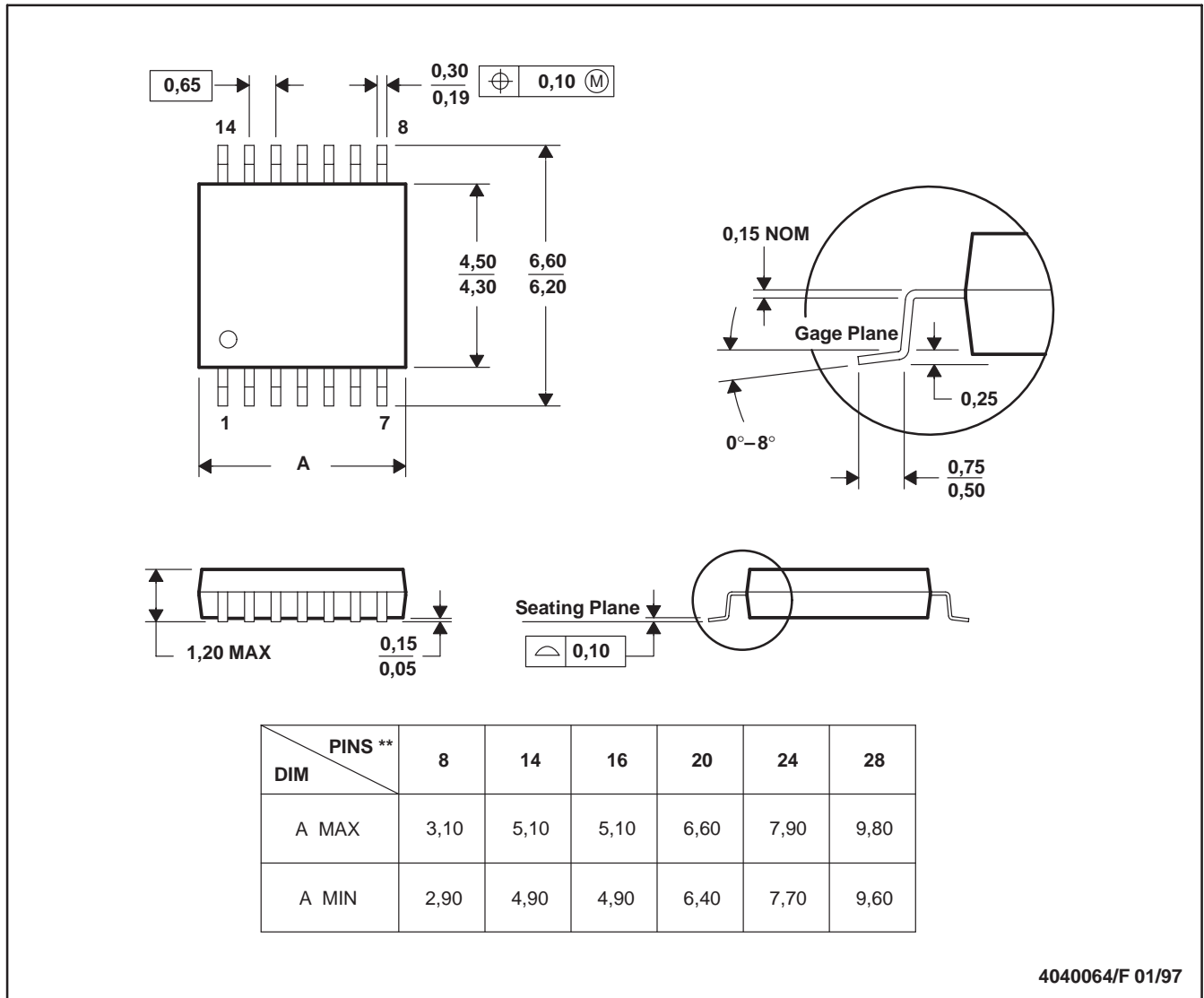


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
Low Power Wireless	www.ti.com/lpw

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless