## *Macronix NBit™ Memory Family*

## 64M-BIT [x 1] CMOS SERIAL eLite Flash™ MEMORY

# FEATURES

### GENERAL

- 67,108,864 x 1 bit structure
- 128 Equal Sectors with 64K byte each
  - Any sector can be erased
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is equal to or less than 2.2V

### PERFORMANCE

- High Performance
  - Fast access time: 25MHz serial clock (50pF + 1TTL Load)
  - Fast program time: 4ms/page (typical, 128-byte per page)
  - Fast erase time: 3s/sector (typical, 64K-byte per sector)
  - Acceleration mode:
    - Program time: 3.2ms/page (typical)
    - Erase time: 2.4s/sector (typical)
- Low Power Consumption
  - Low active read current: 24mA (typical) at 25MHz
  - Low active programming current: 35mA (typical)
  - Low active erase current: 35mA (typical)
  - Low standby current: 5uA (typical, CMOS)
- Minimum 100 erase/program cycle

### SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algrorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
  - Provides detection of program and erase operation completion.
  - Provides auto erase/ program error report

### HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- ACC Pin
  - Program/erase acceleration
- PACKAGE
  - 32-pin SOP (450mil)

## GENERAL DESCRIPTION

The MX25L6402 is a CMOS 67,108,864 bit serial MTP EEPROM, which is configured as 8,388,608 x 8 internally. The MX25L6402 features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by $\overline{CS}$ input.

The MX25L6402 provide sequential read operation on whole chip. User may start to read from any byte of the array. While the end of the array is reached, the device will wrap around to the beginning of the array and continuously outputs data until $\overline{CS}$ goes high.

After program/erase command is issued, auto program/ erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (128 bytes) basis, and erase command is executed on both chip and sector (64K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

When the device is not in operation and $\overline{CS}$ is high, it is put in standby mode and draws less than 5uA DC current.

The MX25L6402 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100 program and erase cycles.

## PIN CONFIGURATIONS

### 32-PIN SOP (450 mil)
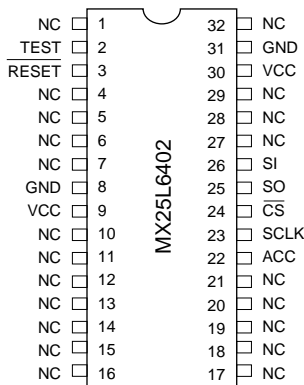


## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| $\overline{CS}$ | Chip Select |
| TEST(1) | Test Mode Select |
| $\overline{RESET}$ | Reset |
| SI | Serial Data Input |
| SO | Serial Data Output |
| SCLK | Clock Input |
| ACC | 12V for program/erase acceleration |
| VCC | + 3.3V Power Supply |
| GND | Ground |
| NC | No Internal Connection |

**Note:**

1. TEST input is used for in-house testing and must be tied to ground during normal user operation.

## BLOCK DIAGRAM

```
                    ┌─────────────┐      ┌───┬──────────────┐
                    │   Address   │      │ X │              │
                    │  Generator  │─────▶│ - │ Memory Array │
                    └─────────────┘      │ D │              │
                           ▲             │ e │              │
                           │             │ c │              │
                           │             │ o │              │
                           │             │ d │              │
                           │             │ e │              │
                           │             │ r │              │
                           │             └───┴──────────────┘
         ┌──────┐    ┌─────────────┐        │        ▲
         │  SI  │───▶│    Data     │────────┤        │
         └──────┘    │  Register   │        │   ┌──────────┐
                     └─────────────┘        └──▶│Y-Decoder │
                           │                    └──────────┘
                           │    ┌─────────┐         ▲
                           └───▶│  SRAM   │         │
                                │ Buffer  │         │
                                └─────────┘         │
                                     │              │
   ┌──────────┐   ┌──────┐    ┌──────────┐   ┌──────────┐   ┌──────────┐   ┌──────────┐
   │ CS,ACC,  │──▶│ Mode │───▶│  State   │──▶│    HV    │   │  Sense   │──▶│  Output  │
   │ RESET    │   │Logic │    │ Machine  │   │Generator │   │Amplifier │   │  Buffer  │
   └──────────┘   └──────┘    └──────────┘   └──────────┘   └──────────┘   └──────────┘
                      ▲                                                          │
                      │                                                          ▼
   ┌──────────┐   ┌──────────────────┐                                     ┌──────────┐
   │  SCLK    │──▶│ Clock Generator  │                                     │    SO    │
   └──────────┘   └──────────────────┘                                     └──────────┘
```
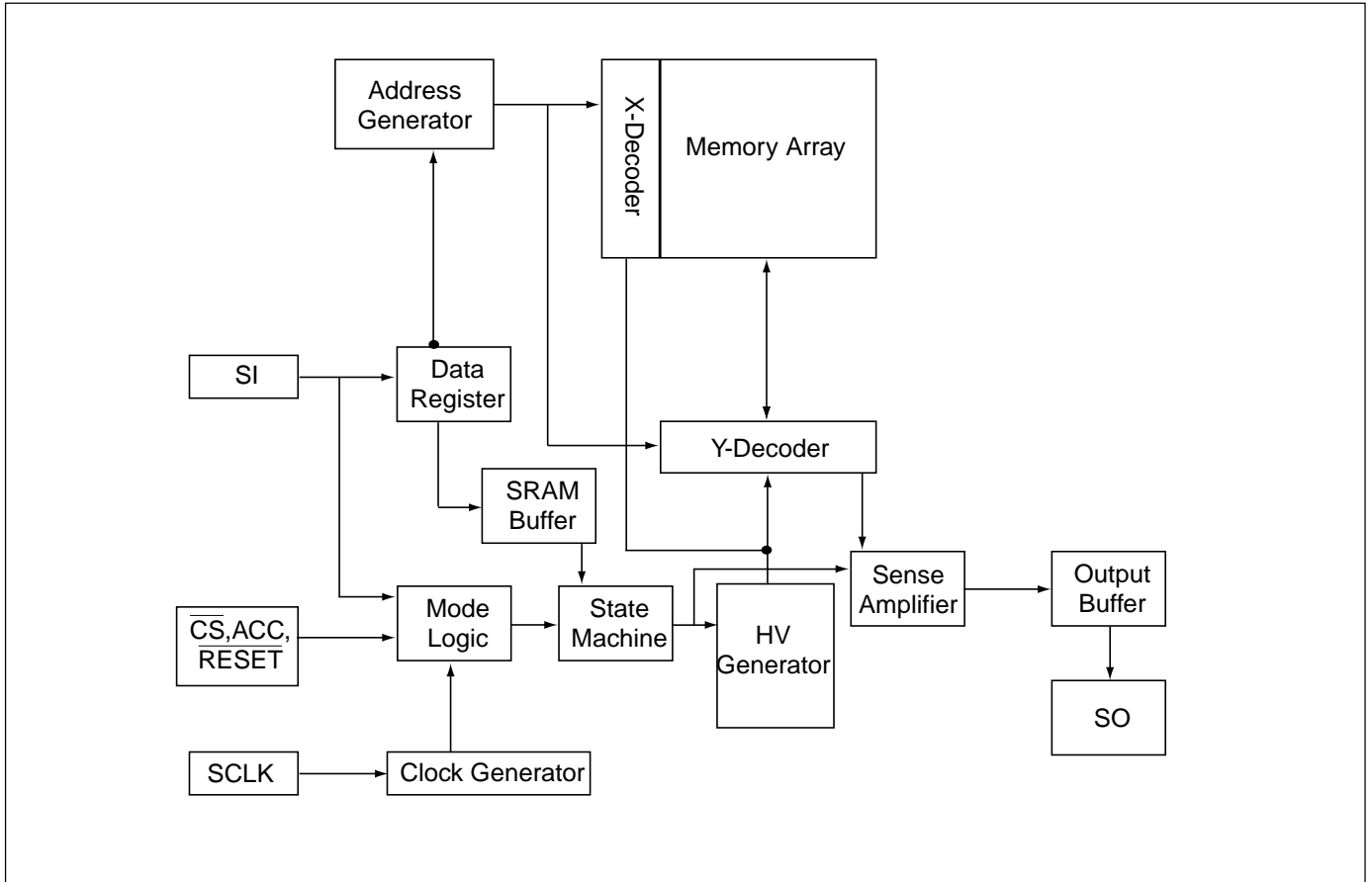
## COMMAND DEFINITION

| Com-mand (byte) | Read Array | Status Read | Clear Status | Read ID | Sector Erase | Chip Erase | Page Program |
|---|---|---|---|---|---|---|---|
| 1st | 52H | 83H | 89H | 85H | F1H | F4H | F2H |
| 2nd | AD1 | X | | X | AD1 | X | AD1 |
| 3rd | AD2 | | | | AD2 | X | AD2 |
| 4th | AD3 | | | | | | AD3 |
| 5th | BA | | | | | | BA |
| 6th | X | | | | | | |
| 7th | X | | | | | | |
| 8th | X | | | | | | |
| 9th | X | | | | | | |
| Action | n bytes read out until $\overline{CS}$ goes high | Output status byte until $\overline{CS}$ goes high | Clear status byte | Output vendor code until $\overline{CS}$ goes high | Start to erase at $\overline{CS}$ rising edge | Start to erase at $\overline{CS}$ rising edge | Load n bytes data to buffer until $\overline{CS}$ goes high & start to program |

Note:
1.X is dummy cycle and is necessary
2.AD1 to AD3 are address input data
3.BA is byte address

| | Bit7(MSB) | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| 1-byte command code | | | | | | | | |
| 3-byte address(0 to 0FFFH) | | | | | | | | |
| AD1: | X | X | A22 | A21 | A20 | A19 | A18 | A17 |
| AD2: | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 |
| AD3: | X | X | X | X | X | X | A8 | A7 |
| 1-byte byte address(0 to 7FH) | | | | | | | | |
| BA: | X | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

Note:
A22 to A16=Sector address

## DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS rising edge.

## COMMAND DESCRIPTION

### (1) Read Array

This command is sent with the 4-byte address (command included), and the byte address, followed by four dummy bytes sent to give the device time to stabilize. The device will then send out data starting at the byte address until CS goes high. The clock to clock out the data is supplied by the master SPI. The read operation is executed on whole array. If the end of the array is reached then the device will wrap around to the beginning of the array.

### (2) Read Status Register

When this command is sent, the device will continuously send out the status register contents starting at bit7. The clock to clock out the data is supplied by the master SPI.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| program/erase completion | NA | NA | erase error | program error | NA | NA | ready/busy |
| Note1 | | | 1=error | 1=error | | | 1=ready 0=busy |

Bit 6,5,2,1 = Reserve for future use.
Bit 4 = "1" -----> There is an error occurred in last erase operation.
    = "0" -----> There is no error occurred in last erase operation.
Bit 3 = "1" -----> There is an error occurred in last program operation.
    = "0" -----> There is no error occurred in last program operation.
Bit 0 = "1" -----> Device is in ready mode.
    = "0" -----> Device is in busy mode.

Note 1: The initial value of Bit7 is "1". Bit7 will have "1" to "0" transit only after program/erase operation is completed. Bit7 will shift from "0" to "1" only after issued program/erase/Clear status register command. Please note the Bit7=0 if program/erase fail.

Note 2: The value of Bit 0 is "1", no matter the result of program/erase is pass or fail.

### (3) Clear Status Register

This command only resets erase error bit (bit 4) and program error bit (bit 3). These two bits are set by on-chip state machine during program/erase operation, and can only be reset by issuing a clear status register command or by powering down VCC.

If status register indicates that error occurred in the last program/erase operation, any further program/erase operation will be prohibited until status register is cleared.

### (4) Read ID

This command is sent with an extra dummy byte( 2-byte command). The device will clock out manufacturer code (C2H) and device code (9CH) when this command is issued. The clock to clock out the data is supplied by the master SPI.

## (5) Sector/Chip Erase

This command is sent with the sector address(A22~A16) when operating Sector Erase.  The device will start the erase sequence after $\overline{CS}$ goes high without any further input.  A sector should be erased in a typical of 3 sec. The average current is less than 35mA.  The chip erase operation does not require the sector address input but two extra dummy bytes are necessary. During this operation, customer can also access Read Status & Read ID operations.

## (6) Page Program

This command is sent with the page number(A22~A7), and 128-byte page address(A6~A0), followed by programming data. The 128-byte page address (A6-A0) must start from 0. One to 128 bytes of data can be loaded into the buffer of the device until $\overline{CS}$ goes high. User needs to issue a complete last byte data, otherwise the last byte data will be ignored. If the end of the page is reached, then the device will wrap around to the beginning of the page. The device will program the specified page with buffered data(Until $\overline{CS}$ goes high) without any further input.  The typical page program time is 4mS. The average current is less than 35mA.

During this operation, customer can also access Read Status & Read ID operations.

## (7) Standby Mode

When $\overline{CS}$ is high and there is no operation in progress, the device is put in standby mode.  Typical standby current is less than 5uA.

## (8) ACC FAST PROGRAM/ERASE FUNCTIONS

When ACC pin is not connected to a 12V power supply, all program and erase current is drawn through the VCC pin. When ACC pin is connected to a 12V power supply, the device draws program and erase current directly from the ACC pin. This eliminates the need for an external switching transistor control the voltage VHH.

The 12V ACC mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. ACC pin may be connected to 12V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

## POWER-ON  STATE

After power-up, the device is placed in the standby state with following status:

The status register is reset with following status :
Bit 7 = "1" -----> Refer to page 5 for detail.
Bit 6,5,2,1 = Reserve for future use.
Bit 4 = "0" -----> Erase error flag is reset.
Bit 3 = "0" -----> Program error flag is reset.
Bit 0="1" -----> Device is in ready state.

## RESET OPERATION

The $\overline{\text{RESET}}$ pin provides a hardware method of resetting the device to reading array data. When the $\overline{\text{RESET}}$ pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tri-states all output pins, and ignores all commands for the duration of the $\overline{\text{RESET}}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity. Current is reduced for the duration of the $\overline{\text{RESET}}$ pulse. When $\overline{\text{RESET}}$ is held at VSS ± 0.3V, the device draws reset current (ICC4). If $\overline{\text{RESET}}$ is held at VIL but not within VSS ± 0.3V, the reset current will be greater. The $\overline{\text{RESET}}$ pin may be tied to system reset circuitry. A system reset would that also reset the SPI memory. Refer to the AC Characteristics tables for $\overline{\text{RESET}}$ parameters.
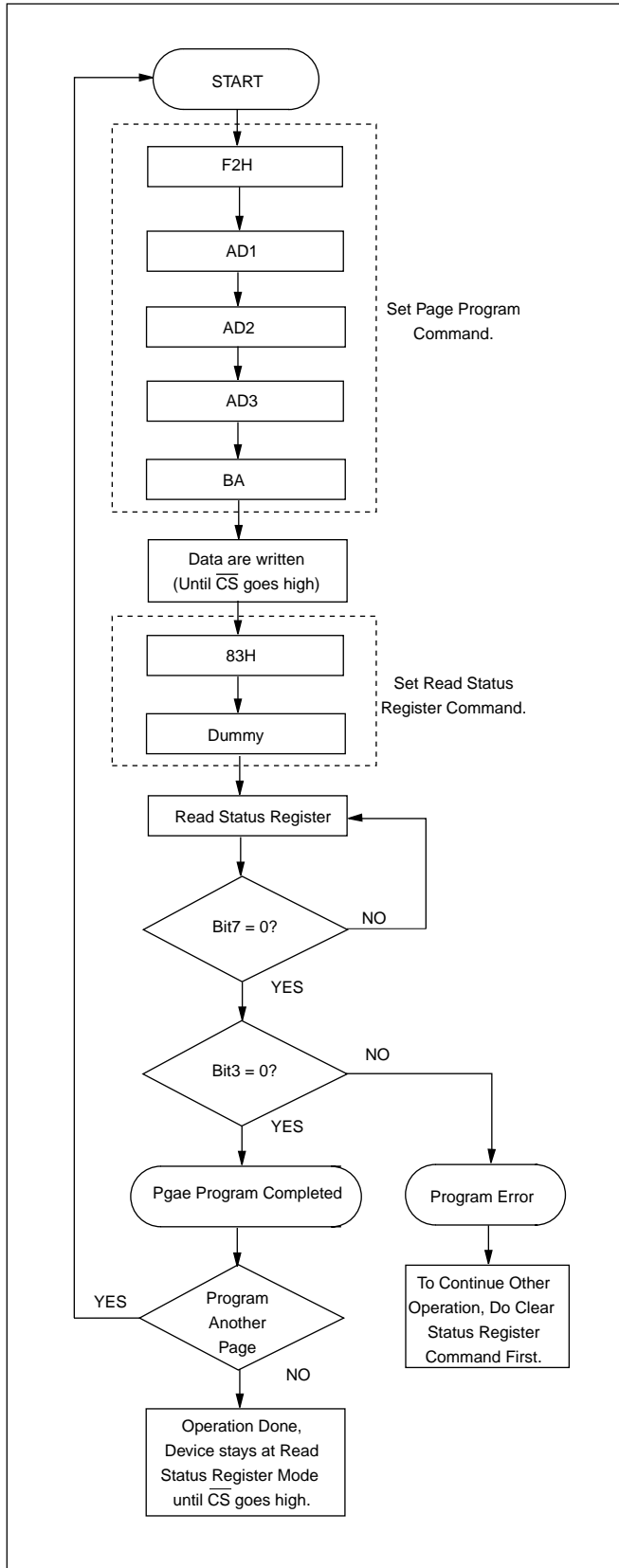
## DATA SEQUENCE

Output data is serially sent out through SO pin, synchronized with the rising edge of SCLK, whereas input data is serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data is bit 7 (MSB) first, then bit 6, bit 5, ...., and bit 0.(LSB)

## ADDRESS SEQUENCE

The address assignment is described as follows :

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BA: Byte address Bit sequence: | X | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| AD1:First Address Bit sequence: | X | X | A22 | A21 | A20 | A19 | A18 | A17 |
| AD2:Second Address Bit sequence: | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 |
| AD3:Thrid Address Bit sequence: | X | X | X | X | X | X | A8 | A7 |

## Auto Page Program Flow Chart

```
                    START

                     F2H          ┐
                                   │
                     AD1           │
                                   │
                     AD2           ├ Set Page Program
                                   │  Command.
                     AD3           │
                                   │
                      BA           ┘

             Data are written
             (Until CS goes high)

                     83H           ┐
                                   ├ Set Read Status
                    Dummy          ┘  Register Command.

             Read Status Register ◄─┐
                                    │
                   Bit7 = 0? ──NO───┘

                      YES

                   Bit3 = 0? ──NO───┐
                                    │
                      YES           │
                                    │
         Pgae Program Completed   Program Error

                      │              │
              ┌───────┤         To Continue Other
         YES  │   Program        Operation, Do Clear
              └── Another         Status Register
                   Page           Command First.

                     NO

             Operation Done,
             Device stays at Read
             Status Register Mode
             until CS goes high.
```

## Auto Chip Erase Flow Chart

```
                    START

                     F4H           ┐
                                   │
                    Dummy          ├ Set Chip Erase
                                   │  Command.
                    Dummy          ┘

                     83H           ┐
                                   ├ Set Read Status
                    Dummy          ┘  Register Command.

             Read Status Register ◄─┐
                                    │
                   Bit 7= 0? ──NO───┘

                      YES

                   Bit 4 = 0? ──NO───┐
                                      │
                      YES             │
                                      │
         Chip Erase Completed     Erase Error

                      │                │
                     NO           To Continue Other
             Operation Done,       Operation, Do Clear
             Device stays at Read   Status Register
             Status Register Mode   Command First
             until CS goes high.
```
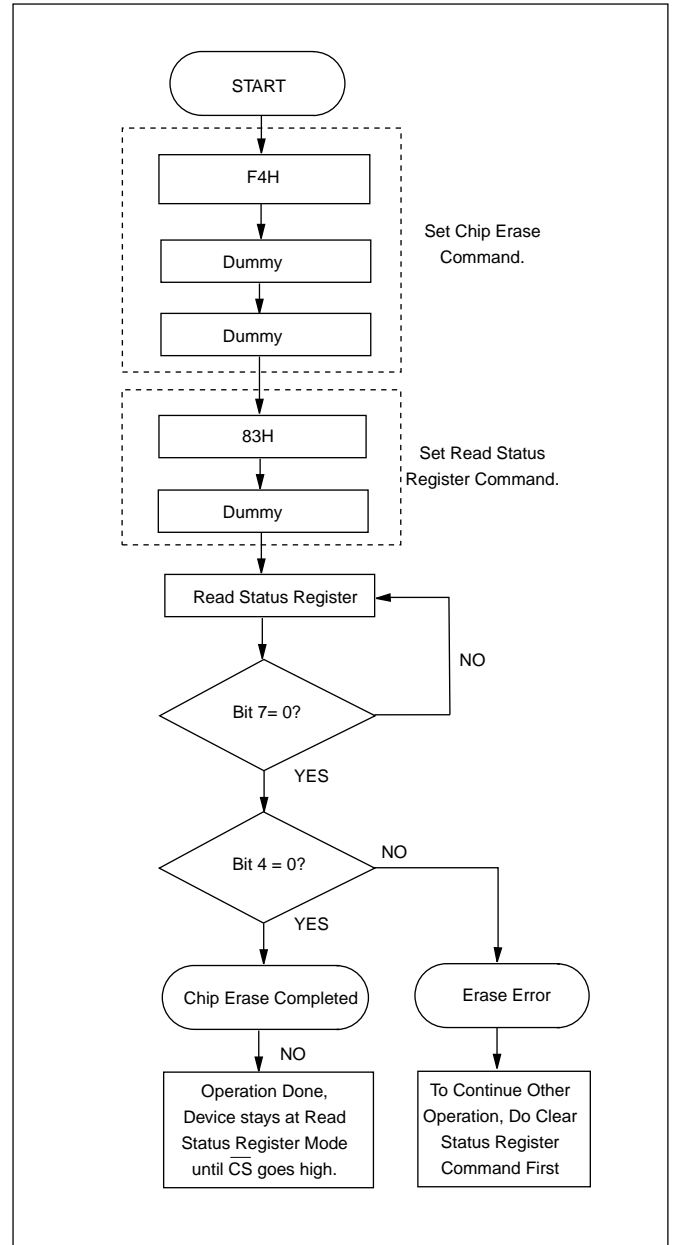
**Auto Sector Erase Flow Chart**

```
                    ┌──────────────┐
             ┌─────▶│    START     │
             │      └──────────────┘
             │              │
             │   ┌ ─ ─ ─ ─ ─│─ ─ ─ ─ ┐
             │      ┌────────▼───────┐
             │   │  │      F1H       │ │
             │      └────────────────┘
             │   │          │          │   Set Sector Eraes
             │      ┌────────▼───────┐       Command.
             │   │  │      AD1       │ │
             │      └────────────────┘
             │   │          │          │
             │      ┌────────▼───────┐
             │   │  │      AD2       │ │
             │      └────────────────┘
             │   └ ─ ─ ─ ─ ─│─ ─ ─ ─ ┘
             │   ┌ ─ ─ ─ ─ ─│─ ─ ─ ─ ┐
             │      ┌────────▼───────┐
             │   │  │      83H       │ │
             │      └────────────────┘    Set Read Status
             │   │          │          │  Register Command.
             │      ┌────────▼───────┐
             │   │  │     Dummy      │ │
             │      └────────────────┘
             │   └ ─ ─ ─ ─ ─│─ ─ ─ ─ ┘
             │      ┌────────▼─────────┐
             │      │ Read Status      │◀──┐
             │      │ Register         │   │
             │      └──────────────────┘   │
             │              │              │
             │          ╱───▼───╲     NO   │
             │         ╱ Bit7 = 0?╲────────┘
             │         ╲         ╱
             │          ╲───┬───╱
             │            YES│
             │               │
             │          ╱───▼───╲     NO
             │         ╱ Bit4 = 0?╲────────────┐
             │         ╲         ╱             │
             │          ╲───┬───╱              │
             │            YES│                 │
             │    ┌──────────▼──────┐   ┌──────▼──────┐
             │    │ Sector Erase    │   │ Erase Error │
             │    │ Completed       │   └─────────────┘
             │    └─────────────────┘          │
             │               │          ┌──────▼──────────┐
             │          ╱────▼────╲     │ To Continue Other│
        YES  │         ╱  Erase    ╲    │ Operation, Do Clear│
        ┌────┴────────╱ Another Sector?╲│ Status Register   │
        │             ╲               ╱ │ Command First.    │
        │              ╲─────┬───────╱  └──────────────────┘
        │                 NO │
        │         ┌──────────▼──────┐
        │         │ Operation Done, │
        │         │ Device stays at Read│
        │         │ Status Register Mode│
        │         │ until CS goes high.│
        │         └─────────────────┘
```
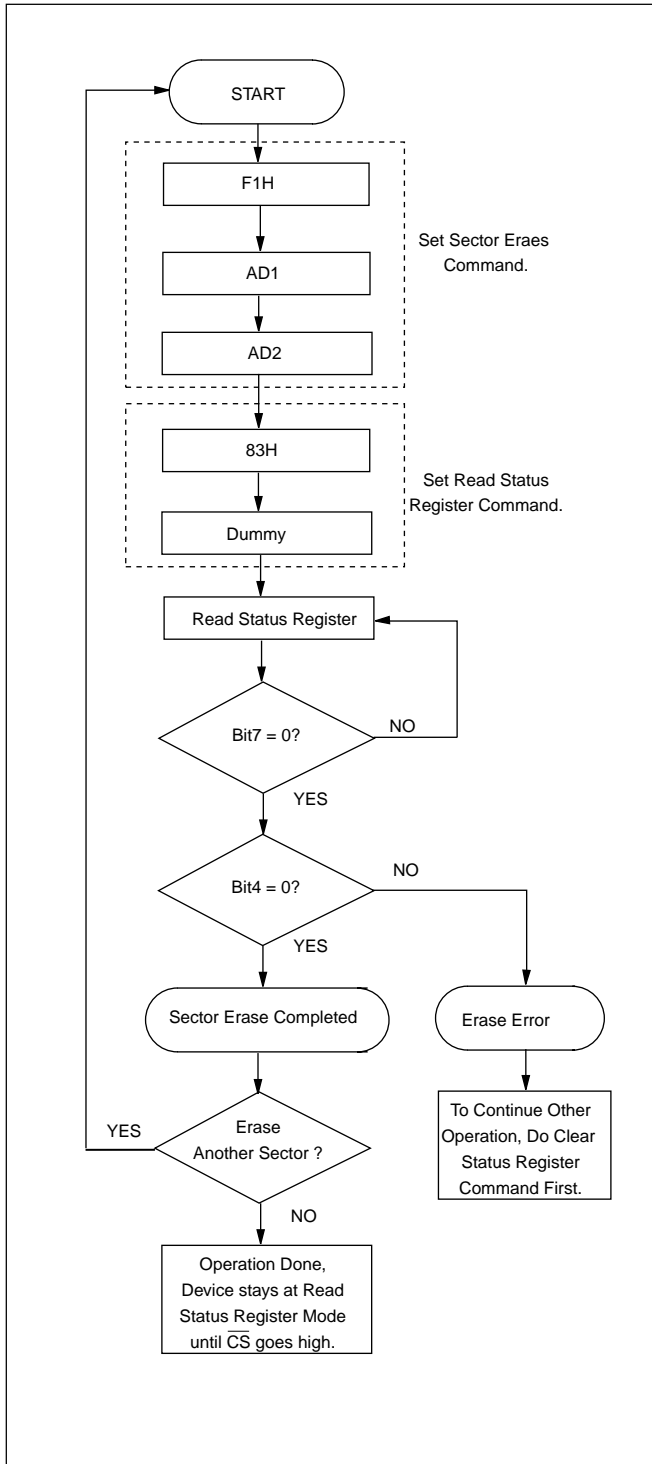
## ELECTRICAL  SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|---|---|
| Ambient Operating Temperature | 0° C to 70° C |
| Storage Temperature | -55° C to 125° C |
| Applied Input Voltage | -0.5V to 4.6V |
| Applied Output Voltage | -0.5V to 4.6V |
| VCC to Ground Potential | -0.5V to 4.6V |

**NOTICE:**

1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device.  This is stress rating only and functional operational sections of this specification is not implied.  Exposure to absolute maximum rating conditions for extended period may affect reliability.

2.Specifications contained within the following tables are subject to change.

3.During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.

4.All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

**Maximum Negative Overshoot Waveform**
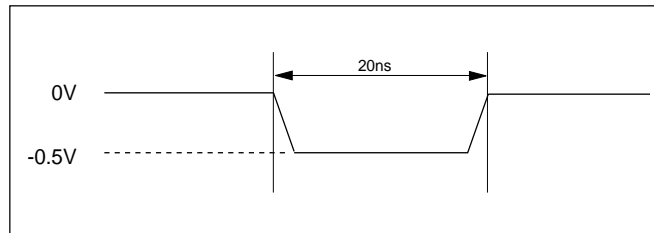
**Maximum Positive Overshoot Waveform**
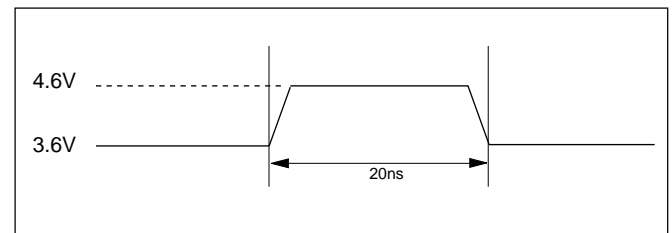
## CAPACITANCE TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 10 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 10 | pF | VOUT = 0V |

## INPUT TEST WAVEFORMS AND MEASURESMENT LEVEL

3.0V

1.5V

0V

AC
Measurement
Level

Note:Input pulse rise and fall time are < 10ns

## OUTPUT LOADING

DEVICE UNDER
TEST

CL

DIODES=IN3064
OR EQUIVALENT

+3.3V

CL=50pF Including jig capacitance
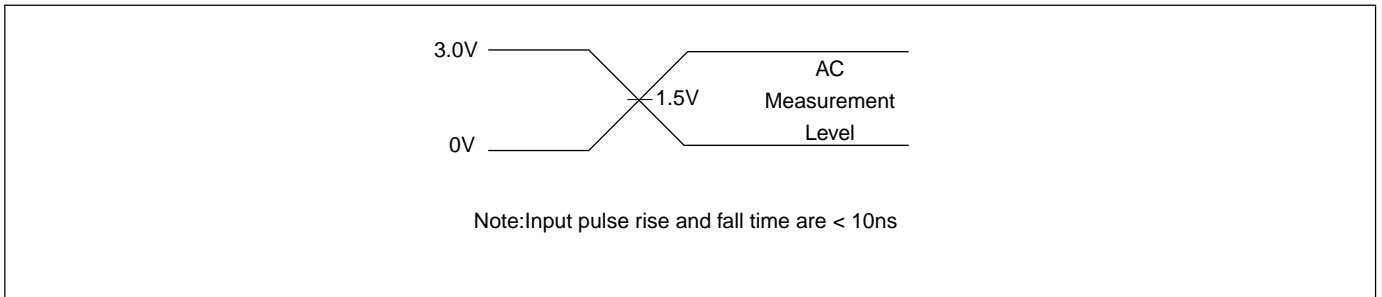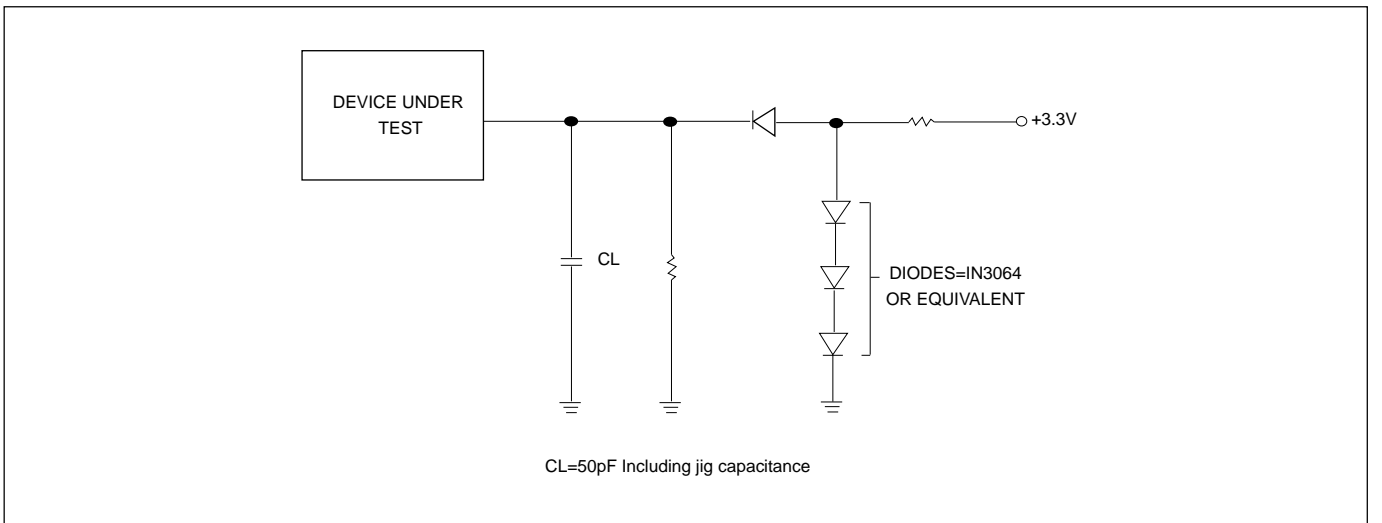
## DC CHARACTERISTICS (Temperature = 0°C to 70°C, VCC = 3.0V ~ 3.6V)

| SYMBOL | PARAMETER | NOTES | MIN. | TYP | MAX. | UNITS | TEST CONDITIONS |
|--------|-----------|-------|------|-----|------|-------|-----------------|
| ILI | Input Load Current | 1 | | | ± 2 | uA | VCC = VCC Max VIN = VCC or GND |
| ILO | Output Leakage Current | 1 | | | ± 10 | uA | VCC = VCC Max VIN = VCC or GND |
| ISB1 | VCC Standby Current(CMOS) | 1 | | 5 | 50 | uA | VCC = VCC Max $\overline{CS}$ = VCC ± 0.2V |
| ISB2 | VCC Standby Current(TTL) | | | 1 | 3 | mA | VCC = VCC Max $\overline{CS}$ = VIH |
| ICC1 | VCC Read | 1 | | 24 | 29 | mA | |
| ICC2 | VCC Program Current | 1 | | 35 | 60 | mA | Program in Progress |
| ICC3 | VCC Erase Current | 1 | | 35 | 70 | mA | Erase in Progress |
| ICC4 | VCC Reset Current | 1 | | 5 | 50 | uA | $\overline{RESET}$=GND ± 0.3V |
| VHH | Voltage for ACC Program Acceleration | 1 | 11.5 | | 12.5 | V | VCC=3.0V~3.6V |
| VIL | Input Low Voltage | | -0.5 | | 0.3VCC | V | |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.5 | V | |
| VOL | Output Low Voltage | | | | 0.4 | V | IOL = 500uA, VCC=2/3 x VCC |
| VOH | Output High Voltage | | 0.8VCC | | | V | IOH = -100uA, VCC=VCC min. |

**NOTES:**

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

## AC CHARACTERISTICS (Temperature = 0° C to 70° C, VCC = 3.0V ~ 3.6V)

| SYMBOL | PARAMETER | Min. | Typ. | Max. | Units | Condition |
|--------|-----------|------|------|------|-------|-----------|
| fSCLK | Clock Frequency | | | 25 | MHz | |
| tCYC | Clock Cycle Time | 40 | | | ns | |
| tSKH | Clock High Time | 20 | | | ns | |
| tSKL | Clock Low Time | 20 | | | ns | |
| tR | Clock Rise Time | | | 5 | ns | f=25MHz |
| tF | Clock Fall Time | | | 5 | ns | f=25MHz |
| tCSA | $\overline{CS}$ Lead Clock Time | 40 | | | ns | |
| tCSB | $\overline{CS}$ Lag Clock Time | 40 | | | ns | |
| tCSH | $\overline{CS}$ High Time | 80 | | | ns | |
| tCSR | $\overline{CS}$ Rise Time | | | 50 | ns | |
| tCSF | $\overline{CS}$ Fall Time | | | 50 | ns | |
| tCSHR | $\overline{RESET}$ High Time to Write Command Valid | 500 | | | ns | |
| tRP | $\overline{RESET}$ Pulse Width | 500 | | | ns | |
| tRST | $\overline{RESET}$ Rise Time | | | 100 | us | |
| tRFT | $\overline{RESET}$ Fall Time | | | 100 | us | |
| tDS | SI Setup Time | 5 | | | ns | |
| tDH | SI Hold Time | 20 | | | ns | |
| tAA | Access Time | | | 30 | ns | |
| tDOH | SO Hold Time | 5 | | | ns | |
| tDOZ | SO Floating Time | 0 | | 20 | ns | |

**NOTES:**
1. Typical value is calculated by simulation.

## SERIAL DATA INPUT/OUTPUT TIMING
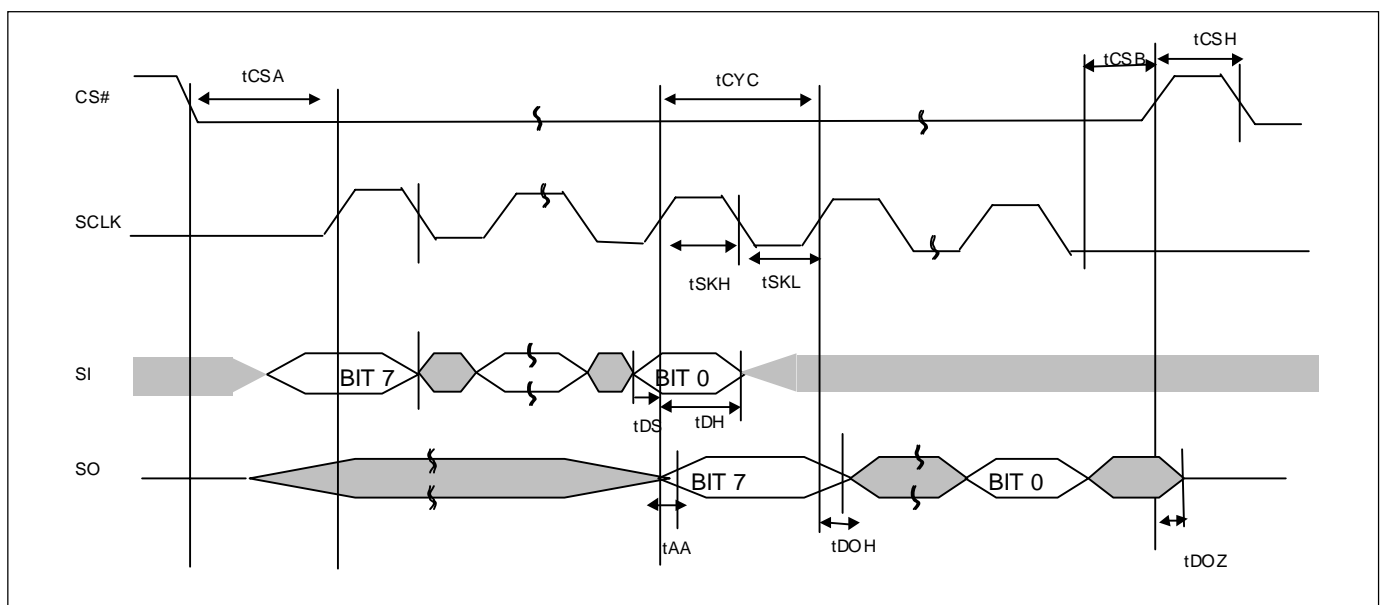
## STANDBY TIMING WAVEFORM
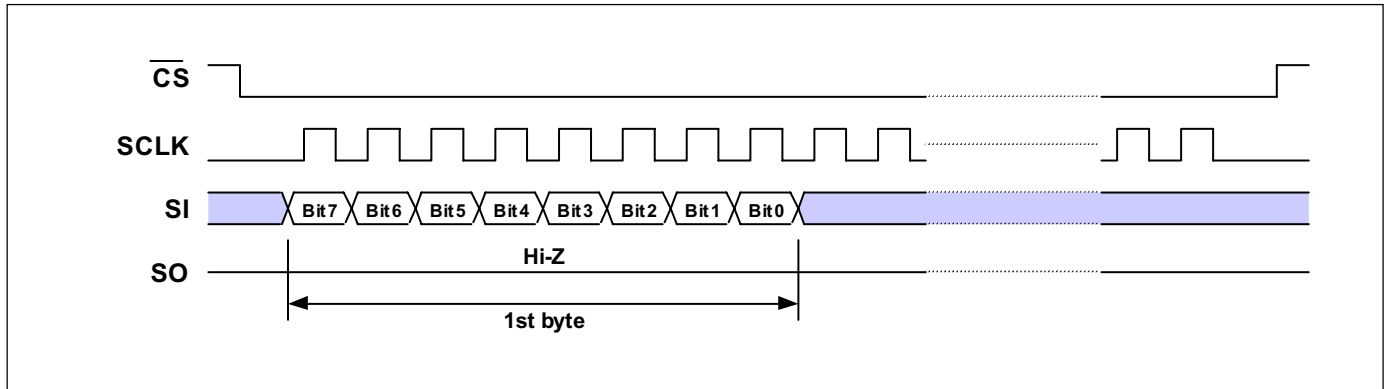


When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next $\overline{CS}$ falling edge. In standby mode, SO pin of this LSI should be High-Z. While $\overline{CS}$=VIH, current=standby current, while $\overline{CS}$=VIL and commands are issuing, or commands are invalid, current=24mA(typ.) to 29mA(max.).

## $\overline{RESET}$ TIMING WAVEFORM
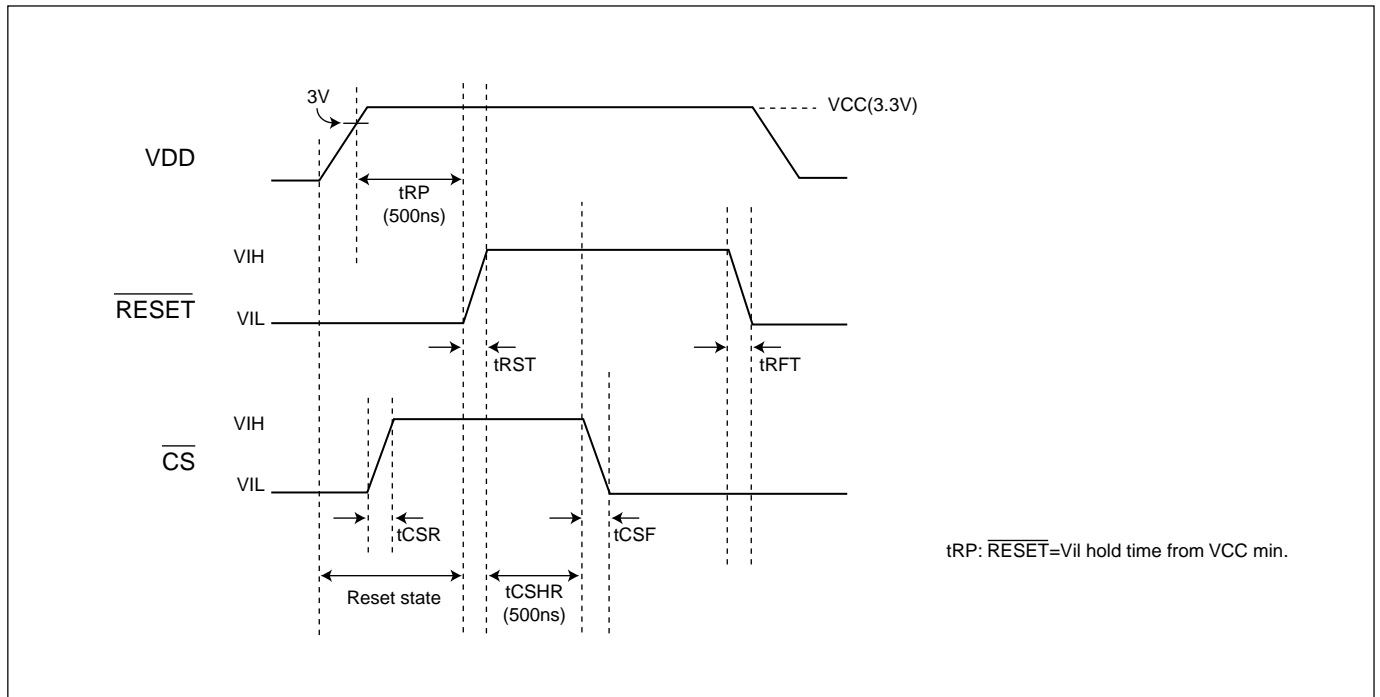
## READ ARRAY TIMING WAVEFORM
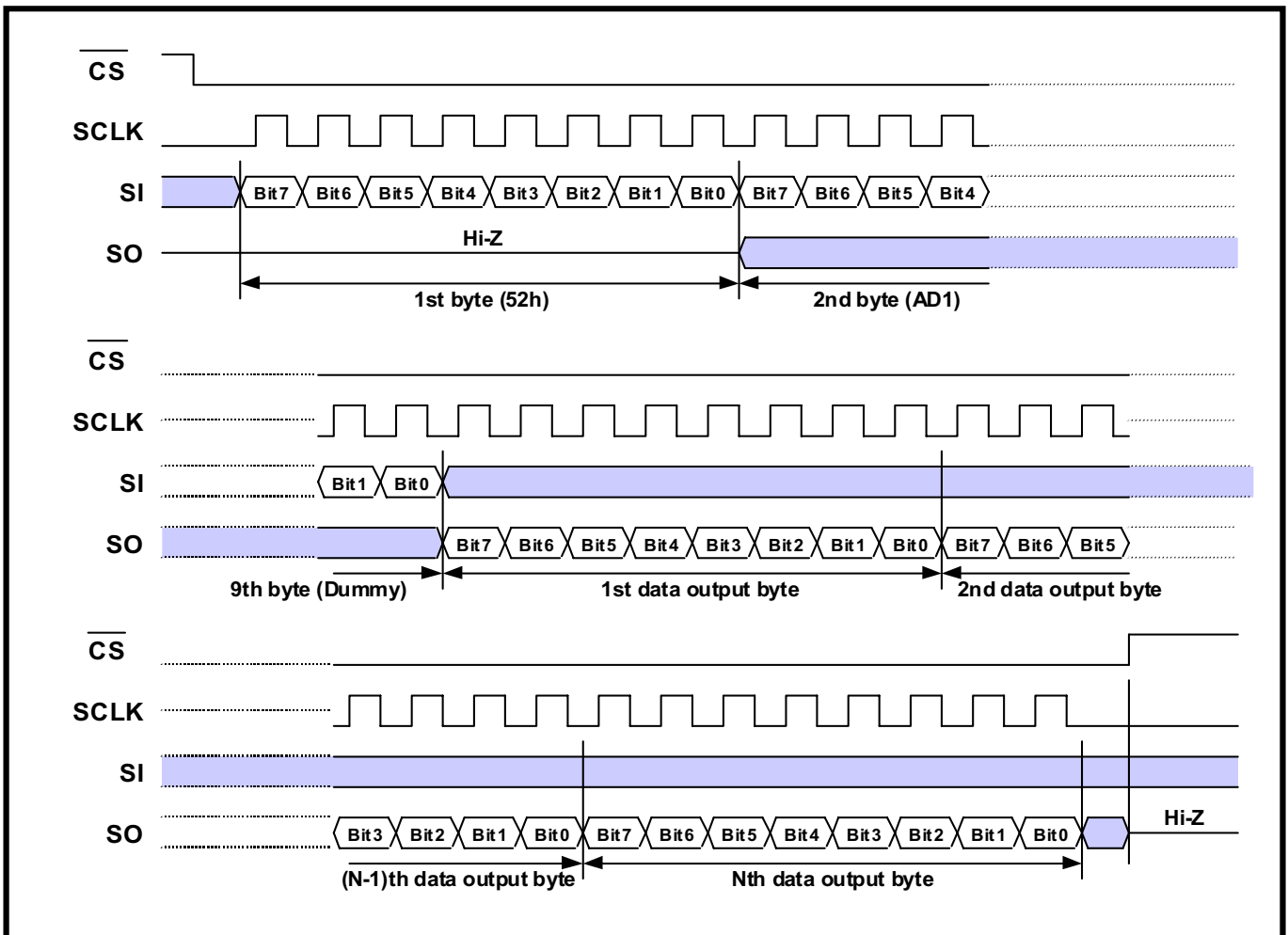


**NOTES:**

1. 1st Byte='52h'
2. 2nd Byte=Address 1(AD1), A17=BIT 0, A18=BIT1, A19=BIT2, A20=BIT3, A21=BIT4, A22=BIT5.
3. 3rd Byte=Address 2(AD2), A9=BIT0, A10=BIT1,......A16=BIT7
4. 4th Byte=Address 3(AD3), A7=BIT0, A8=BIT1
5. 5th Byte=Byte Address(BA), A0=BIT0, A1=BIT1,......A6=BIT6
6. 6th-9th Bytes for SI ==> Dummy Bytes (Don't care)
7. From Byte 10, SO Would Output Array Data

# READ STATUS REGISTER TIMING WAVEFORM
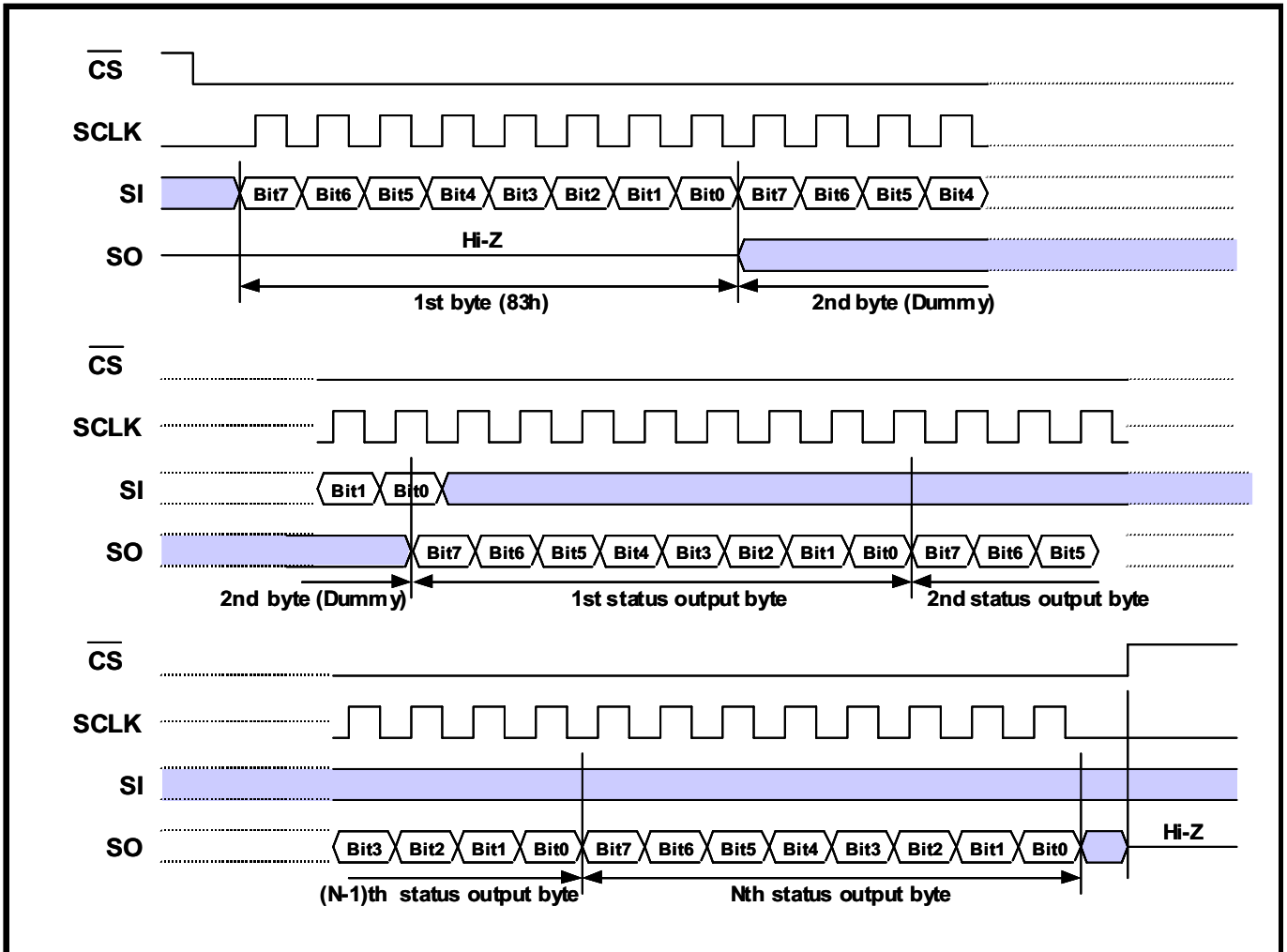


**NOTES:**

1. BIT 7=0 ==> Program/Erase completed
2. BIT 4=1 ==>Erase Error
3. BIT 3=1 ==>Program Error
4. BIT 1,2,5,6 ==> Reserve for future use
5. Bit  0=1 ==> Device is in ready state

## CLEAR STATUS REGISTER TIMING WAVEFORM
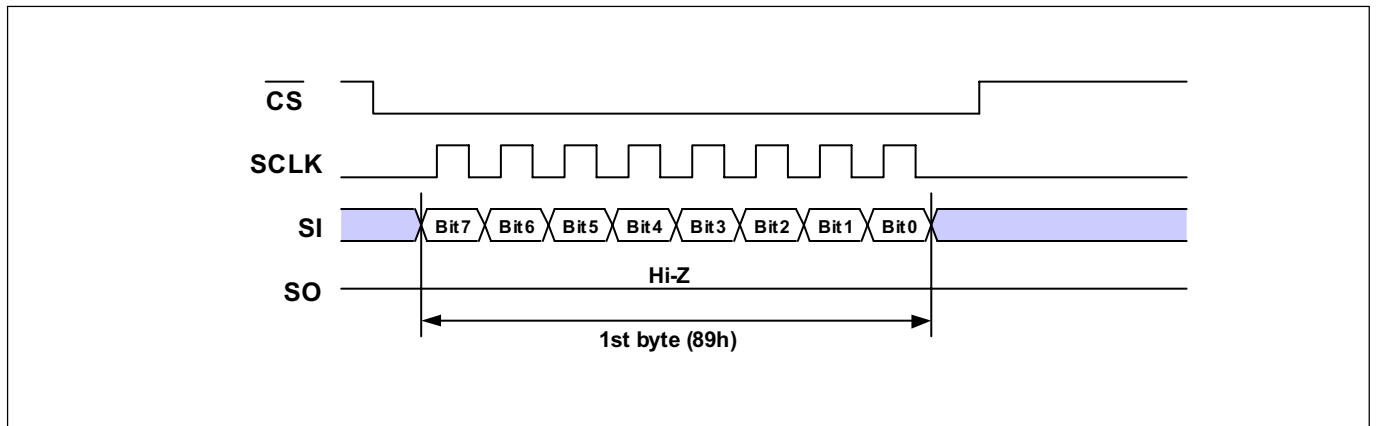


**NOTES:**

1. 1st Byte='89h' ==> CLEAR STATUS REGISTER
2. SO at Hi-Z state

## READ ID TIMING WAVEFORM
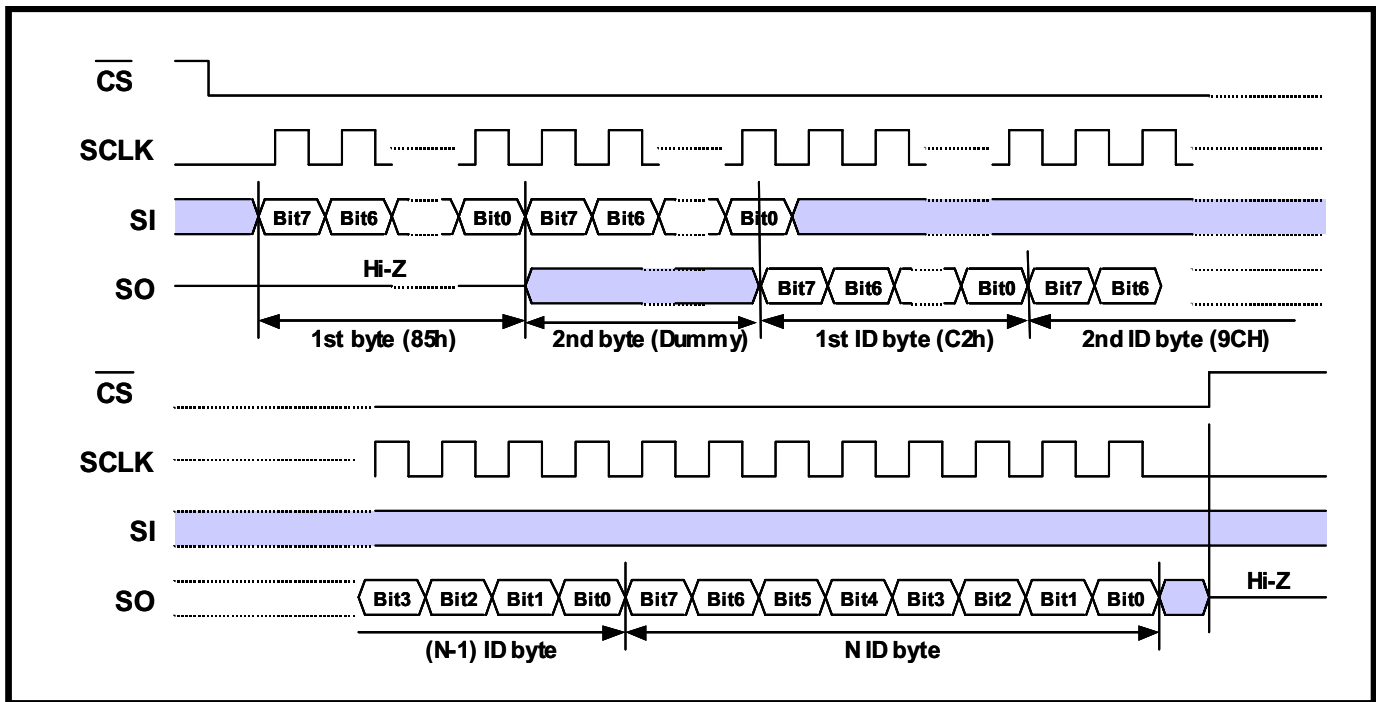


**NOTES:**
1. 1st Byte:85h.
2. 2nd Byte:Dummy Byte.
3. 3rd Byte:Output Manufacture Code(C2h).
4. 4th Byte:Output Device Code(9CH).
5. The 2 bytes ID output will be wrap around.

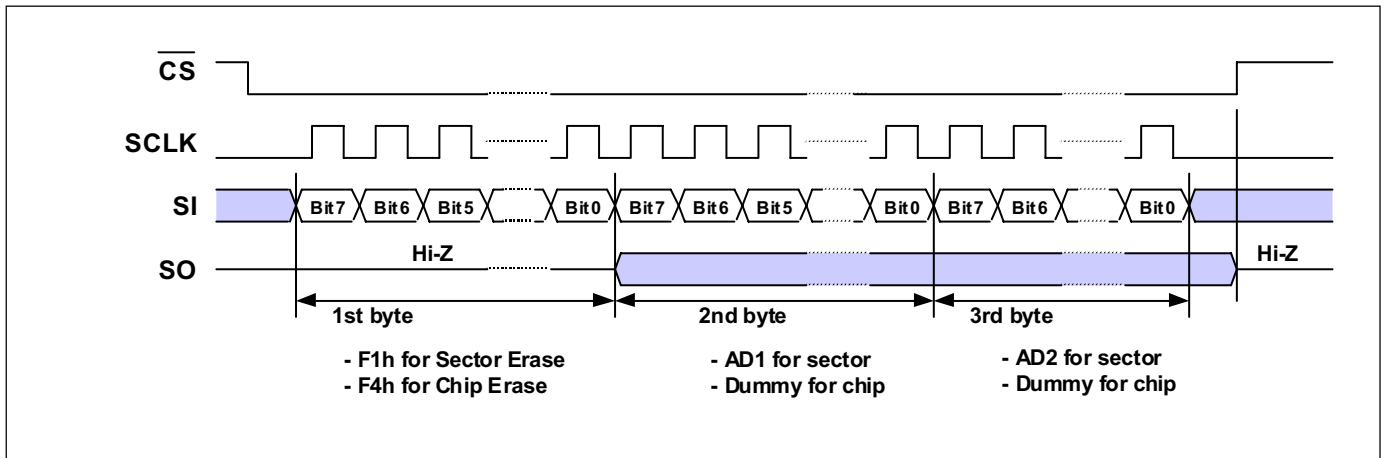## AUTO PAGE PROGRAM TIMING WAVEFORM
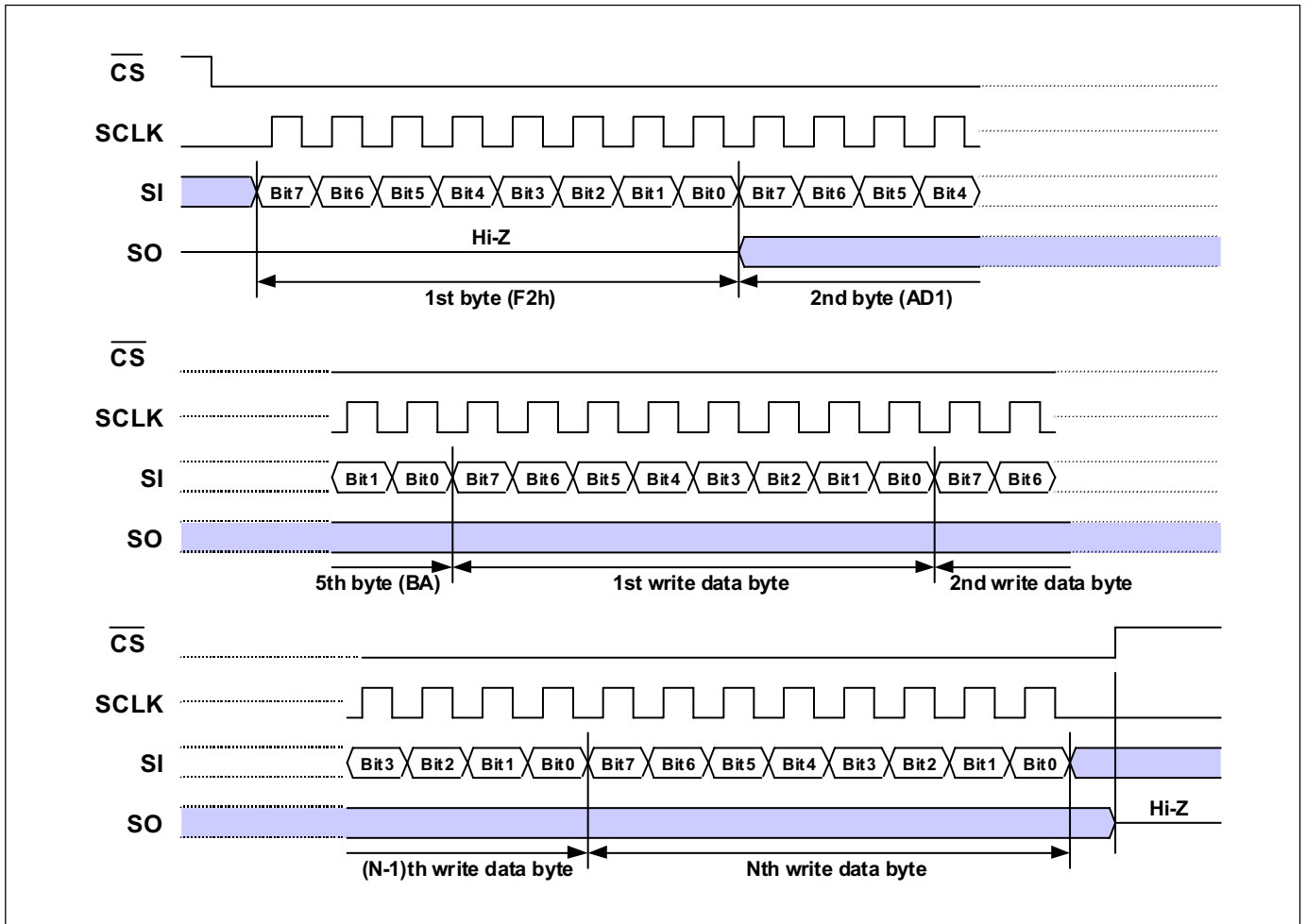


**NOTES:**
1. 1st Byte:F2h.
2. 2nd Byte:Address AD1.
3. 3rd Byte:Address AD2
4. 4th Byte:Address AD3
5. 5th Byte:Address BA.
6. 6th byte:1st write data byte.
7. When the last byte of the page will be written, the Byte Address will be wrap around to the first byte of the Page.
8. The 128-byte page address (A6~A0) must start from 0.

## ACCELERATED PROGRAM TIMING DIAGRAM
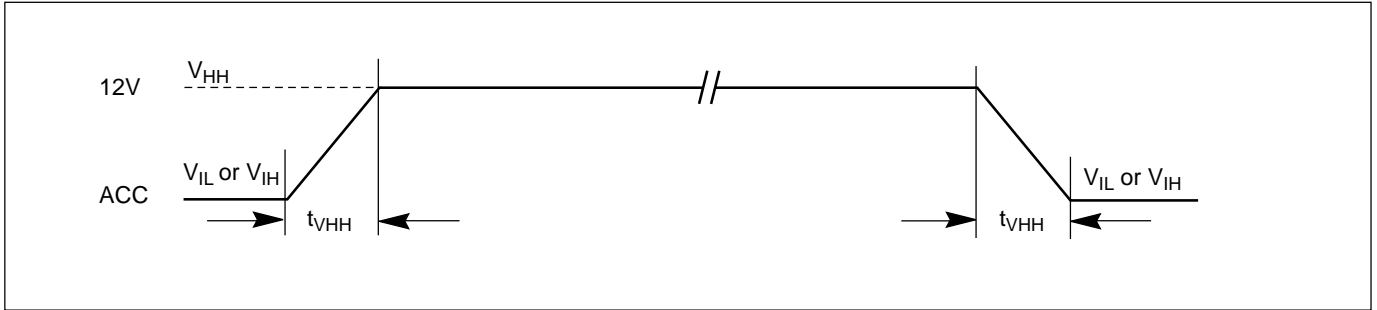


Note: tVHH (VHH Rise and Fall Time) min. 250ns

## AUTO SECTOR/CHIP ERASE  TIMING WAVEFORM



1st byte
- F1h for Sector Erase
- F4h for Chip Erase

2nd byte
- AD1 for sector
- Dummy for chip

3rd byte
- AD2 for sector
- Dummy for chip

**NOTES:**

1. 1st byte:F1h for Sector Erase.
2. 2nd byte:Address AD1 for Sector Erase, Dummy byte for chip erase.
3. 3rd byte:Address AD2 for Sector Erase, Dummy byte for chip erase.

## ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | TYP. (1) | Max. (2) | UNIT | Comments |
|---|---|---|---|---|
| Chip Erase Time | 160 | 512 | s | Note (4) |
| Chip Erase Time (with ACC=12V) | 128 | 410 | s | Note (4) |
| Sector erase Time | 3 | 24 | s | Note (4) |
| Sector erase Time (with ACC=12V) | 2.4 | 19 | s | Note (4) |
| Page Programming Time | 4 | 16 | mS | Excludes system level overhead(3) |
| Page Programming Time (with ACC=12V) | 3.2 | 12.8 | mS | |
| Chip Programming Time | 240 | 480 | s | Excludes system level overhead(3) |
| Chip Programming Time (with ACC=12V) | 180 | 360 | s | |

Note:

1. Typical program and erase time assumes the following conditions: 25° C, 3.0V, and all bits are programmed by checker-board pattern.
2. Under worst conditions of 70° C and 3.0V. Maximum values are up to including 100 program/erase cycles.
3. System-level overhead is the time required to execute the command sequences for the page program command.
4. Excludes 00H programming prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure)

## ORDERING INFORMATION

| PART NO. | ACCESS TIME | OPERATING CURRENT | STANDBY CURRENT | PACKAGE | Remark |
|---|---|---|---|---|---|
| MX25L6402MC-40 | 25MHz | 24mA | 50uA | 32 pin SOP (450 mil) | |
| MX25L6402MC-40G | 25MHz | 24mA | 50uA | 32 pin SOP (450 mil) | Pb-free |

## PACKAGE IMFORMATION

**Title:** **Package Outline for SOP 32L (450MIL)**
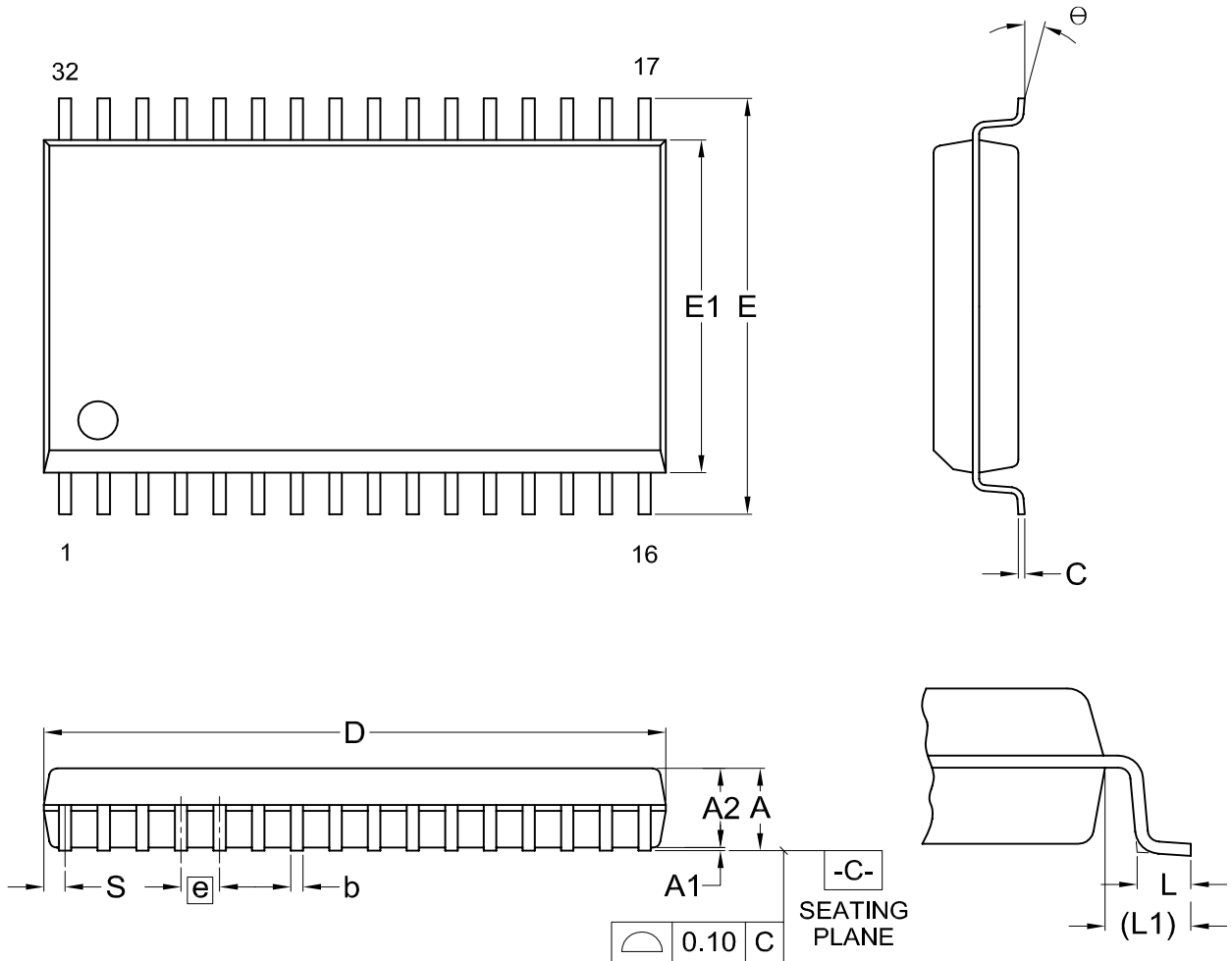


Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **mm** | Min. | --- | 0.10 | 2.59 | 0.36 | 0.15 | 20.32 | 13.92 | 11.18 | | 0.56 | 1.20 | 0.58 | 0 |
| | Nom. | --- | 0.15 | 2.69 | 0.41 | 0.20 | 20.45 | 14.12 | 11.30 | 1.27 | 0.76 | 1.40 | 0.70 | 5 |
| | Max. | 3.00 | 0.20 | 2.80 | 0.51 | 0.25 | 20.57 | 14.32 | 11.43 | | 0.96 | 1.60 | 0.83 | 8 |
| **Inch** | Min. | --- | 0.004 | 0.102 | 0.014 | 0.006 | 0.800 | 0.548 | 0.440 | | 0.022 | 0.047 | 0.023 | 0 |
| | Nom. | --- | 0.006 | 0.106 | 0.016 | 0.008 | 0.805 | 0.556 | 0.445 | 0.050 | 0.030 | 0.055 | 0.028 | 5 |
| | Max. | 0.118 | 0.008 | 0.110 | 0.020 | 0.010 | 0.810 | 0.564 | 0.450 | | 0.038 | 0.063 | 0.033 | 8 |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|---|---|---|---|---|---|
| | | **JEDEC** | **EIAJ** | | |
| 6110-1404 | 5 | MO-099 | | | 11-26-'03 |

## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1. Removed title "Preliminary" on page 1 | P1 | SEP/29/2004 |

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