

Quad 2-input NOR Gate with Strobe

ELECTRICALLY TESTED PER: MPG 10500

The 10500 is a quad 2 input NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

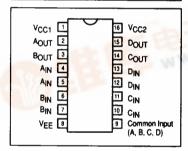
- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% 80%)

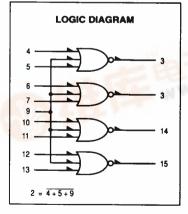
	PI	N ASSIGNM	ENTS	
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V _{CC1}	1	5	2	GND
AOUT	2	6	3	51 Ω to VTT
BOUT	3	7	4	51 Ω to V _{TT}
AIN	4	8	5	OPEN
AIN	5	9	7	OPEN
BIN	6	10	8	OPEN
B _{IN}	7	11	9	OPEN
VEE	8	12	10	VEE
Common Input	9	13	12	OPEN
C _{IN}	10	14	13	OPEN
C _{IN}	11	15	14	OPEN
D _{IN}	12	16	15	OPEN
D _{IN}	13	1	17	OPEN
COUT	14	2	18	51 Ω to V _{TT}
DOUT	15	3	19	51 Ω to V _{TT}
VCC2	16	4	20	GND

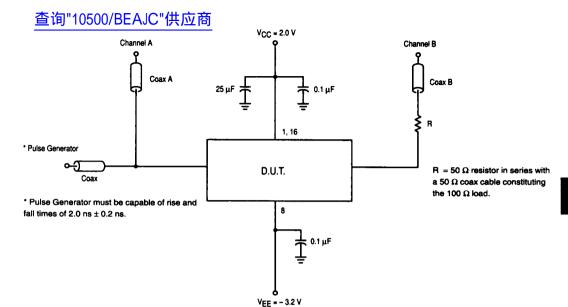
BURN - IN CONDITIONS: VTT = -2.0 V MAX/ -2.2 V MIN VEE = -5.7 V MAX/ -5.2 V MIN

Military 10500





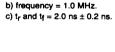




- Length of CoaxA and CoaxB should be of equal length for equal time delay.
- 2. Unused outputs should be loaded 100 Ω to ground.
- 3. 2:1 divider may be used.

NOTES

VIN waveform has the following characteristics:



a) Pulse width ≥ 20 ns.

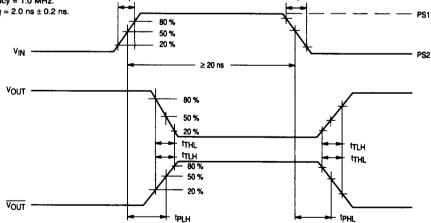


Figure 1. Switching Test Circuit and Waveforms

10500 QUIESCENT LIMIT TABLE *

VEE

VCC +2.0 +2.0 +2.0

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Test Voltage Values (Volts)

5.2

PS2

P. ±

-1.475

-1.105

-1.85 -1.82

T_A = 25 °C T_A = 125 °C

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VIH2

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VIH1 -0.78 -0.63

Test Temperature OŽBĘÃ

5.2

+0.345

+1.24

-1.510

-1.92

-0.88

TA = -55 °C

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

	_			,				,		·		
供	应	Pinouts referenced are for DIL package, check Pin Assignarents		P. U. T.	2, 3, 14, 15	2, 3, 14, 15	2, 3, 14, 15	2, 3, 14, 15	8	4 - 7, 10 - 13	6	4 - 7, 10 - 13
	TEST VOLTAGE APPLIED TO PINS BELOW:	k Pin As	$V_{CC} = 0$ V, Output Load = 100 Ω to - 2.0 V	သူ	1, 16	1, 16	1, 16	1, 16	1, 16	1, 16	1, 16	1, 16
	TO PINS	ige, chec	. 100 £2 to	VEE	80	8	80	8	8	8	8	80
	PPLIED	IL pack	It Load =	GND								
	TAGE A	are for D	V, Outpr	VIL2			4 - 7, 9 - 13					
	FST VO	erenced	0= 00 0= 00	VIH2				4 - 7, 9 - 13				
		inouts ref		VIL1	4, 5, 10, 11							4 - 7, 9 - 13
		α.		γ.		4-7, 9-13				4 - 7, 9 - 13	6	
	Units				>	>	>	>	ωĄ	μA	μA	Αμ
		J₀ 99	e dno	Max	- 0.88	- 1.655	- 0.88	- 1.635	- 3.0	415	800	
		- 55	Subgroup 3	Min	- 1.08	- 1.92	- 1.10	- 1.92	- 29			0.5
	its	ာ ့	oup 2	Мах	- 0.63	- 1.565	- 0.63	- 1.565	- 3.0	415	800	
	Limits	+ 125 °C	Subgroup 2	Min	- 0.825	- 1.82	- 0.845	- 1.82	- 29			0.3
		၁့	oup 1	Мах	-0.78	- 1.62	- 0.78	- 1.60	- 3.0	245	470	
		+ 25 °C	Subgroup 1	Νin	- 0.93	- 1.85	- 0.95	- 1.85	- 26			0.5
	Parameter	L	Functional Parameters:		High Output Voltage	Low Output Voltage	High Output Voltage	Low Output Voltage	Power Supply Drain Current	Input Current High	Input Current High	Input Current Low
	Symbol				но,	NOL	VОНА	VOLA	33	НII	H1 ₁	⊒

10500 QUIESCENT LIMIT TABLE *

ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 2 0 notes

VEE

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VIH2 VIL2 -1.105 -1.475

P.31

PS = +

VIL1

-0.78

T_A = 25 °C T_A = 125 °C

Έ

Test Temperature

Test Voltage Values (Volts)

查询"10500

5.2

+2.0 +2.0

-1.82 | -1.000 | -1.400 | +1.24 | +0.345

to - 2.0 volts.	olts.							7A = -6	2, S	T_A = -55 °C -0.88 -1.92 -1.255 -1.510 +1.03 +0.285 +2.0 ₹294 -5.2	1.92	1.255	1.510	+1.03	+0.285	+2.0	" * #	-5.2	
																	区		
Symbol	Parameter			Limits	its			Units			TEST VC	CTAGE	APPLIE	ED TO P	TEST VOLTAGE APPLIED TO PINS BELOW:		7 [_
		+ 25	+ 25 °C	+ 125 °C	2 ، د	− 55 °C	ပ္		•	Pinouts referenced are for DIL package, check Pin Assignments	ference	d are for	r DIL pa	ckage,	check Pin	n Assigi	nments		
	Functional Parameters:	Subgr	Subgroup 9	Subgro	Subgroup 10	Subgroup 11	up 11				NCC=	2.0 V, O	utbut L	oad = 1(V _{CC} = 2.0 V, Output Load = 100 Ω to GND	Q.			
		Min	Max	Min	Min Max	Min Max	Max		N/N	VOUT VCC VEEL	_	ပ္ပ	VEEL			P. U. T.			_
TLH	Rise Time	1.1	3.3	1.0	4.0	0.1	4.0	SII	4,6	2,3		1, 16	8		2,	2, 3, 14, 15	2		
Ŧ	Fall Time	1.	3.3	3.3 1.0	4.0	4.0 1.0 4.0	4.0	us	4,6	2,3		1, 16	8		2,	2, 3, 14, 15	5		
tPLH	Propagation Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	su	10, 13	14, 15		1, 16	8			2, 3, 14			
tP.H.	Propagation Delay	1.0	5.9	2.9 1.0 3.7 1.0 3.7	3.7	1.0	3.7	Su	10, 13	ns 10,13 14,15 1,16	5	. 16	80			2, 3, 14			