



April 1992
Revised November 1999

74ABT16244

16-Bit Buffer/Line Driver with 3-STATE Outputs

General Description

The ABT16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

Features

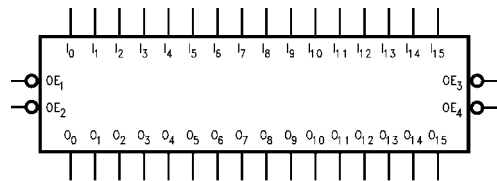
- Separate control logic for each nibble
- 16-bit version of the ABT244
- Outputs sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Ordering Code:

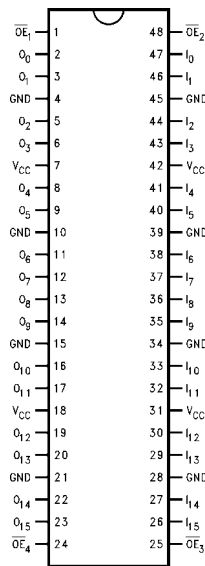
Order Number	Package Number	Package Description
74ABT16244CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16244CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices are also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



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Truth Tables

Inputs		Outputs
$\overline{OE_1}$	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE_2}$	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE_3}$	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

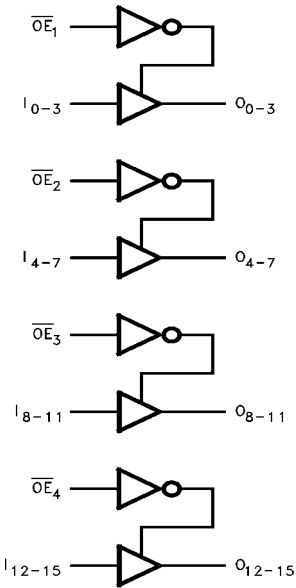
Inputs		Outputs
$\overline{OE_4}$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The ABT16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagram



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DC Electrical Characteristics									
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.4	0.7	V	5.0	T _A = 25°C (Note 4)		
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.3	-1.0		V	5.0	T _A = 25°C (Note 4)		
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.7	3.0		V	5.0	T _A = 25°C (Note 5)		
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.4		V	5.0	T _A = 25°C (Note 6)		
V _{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T _A = 25°C (Note 6)		
Note 4: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.									
Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.									
Note 6: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V _{ILD}), 0V to threshold (V _{IHD}). Guaranteed, but not tested.									
AC Electrical Characteristics									
Symbol	Parameter	T _A =+25°C V _{CC} =+5V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 50 pF		Units		
		Min	Typ	Max	Min	Max			
t _{PLH}	Propagation	1.0	2.3	3.9	1.0	3.9	ns		
t _{PHL}	Delay Data to Outputs	1.0	2.7	3.9	1.0	3.9			
t _{PZH}	Output Enable	1.5	3.5	6.3	1.5	6.3	ns		
t _{PZL}	Time	1.5	3.5	6.3	1.5	6.3			
t _{PHZ}	Output Disable	1.0	4.2	6.7	1.0	6.7	ns		
t _{PLZ}	Time	1.0	3.2	6.7	1.0	6.7			
Extended AC Electrical Characteristics									
Symbol	Parameter	-40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 50 pF 16 Outputs Switching (Note 7)			T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 250 pF 1 Output Switching (Note 8)		T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 250 pF 16 Outputs Switching (Note 9)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{TOGGLE}	Max Toggle Frequency	100							MHz
t _{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns
t _{PHL}	Data to Outputs	1.5		5.3	1.5	6.0	2.5	8.0	
t _{PZH}	Output Enable Time	1.5		6.5	2.5	7.8	2.5	9.5	ns
t _{PZL}		1.5		6.5	2.5	7.8	2.5	8.5	
t _{PHZ}	Output Disable Time	1.0		6.7	(Note 10)		(Note 10)		ns
t _{PLZ}		1.0		6.7					
Note 7: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).									
Note 8: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.									
Note 9: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.									
Note 10: The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.									

Skew				
Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50 \text{ pF}$ 16 Outputs Switching (Note 11)	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250 \text{ pF}$ 16 Outputs Switching (Note 12)	Units
		Max	Max	
t_{OSHL} (Note 13)	Pin to Pin Skew HL Transitions	1.0	1.5	ns
t_{OSLH} (Note 13)	Pin to Pin Skew LH Transitions	1.0	1.5	ns
t_{PS} (Note 14)	Duty Cycle LH-HL Skew	1.5	1.5	ns
t_{OST} (Note 13)	Pin to Pin Skew LH/HL Transitions	1.7	2.0	ns
t_{PV} (Note 15)	Device to Device Skew LH/HL Transitions	2.0	2.5	ns
Note 11: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) Note 12: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. Note 13: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested. Note 14: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested. Note 15: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.				
Capacitance				
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^{\circ}\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 5.0\text{V}$
C_{OUT} (Note 16)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$
Note 16: C_{OUT} is measured at frequency $f = 1 \text{ MHz}$; per MIL STD-883, Method 3012.				

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AC Loading

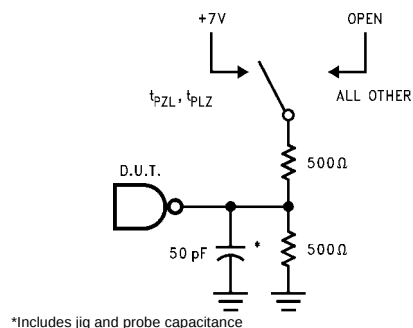


FIGURE 1. Standard AC Test Load

Amplitude	Rep Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

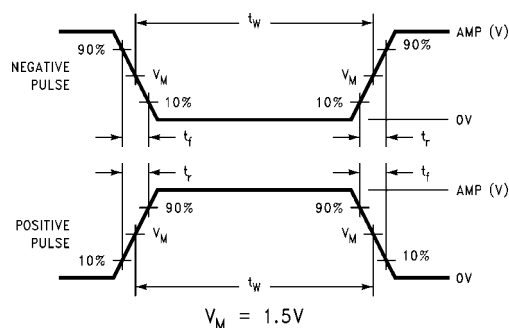


FIGURE 2. Test Input Pulse Requirements

AC Waveforms

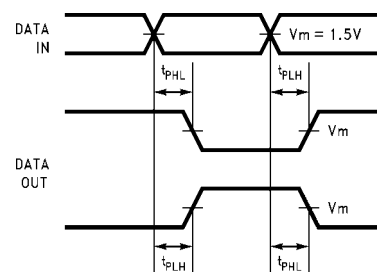


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

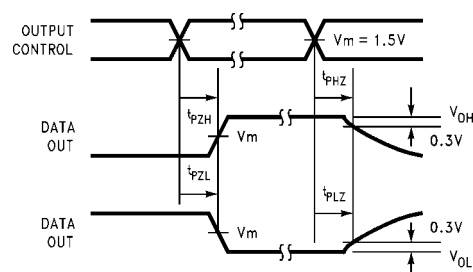


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

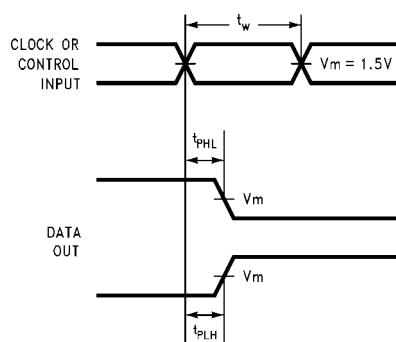


FIGURE 5. Propagation Delay, Pulse Width Waveforms

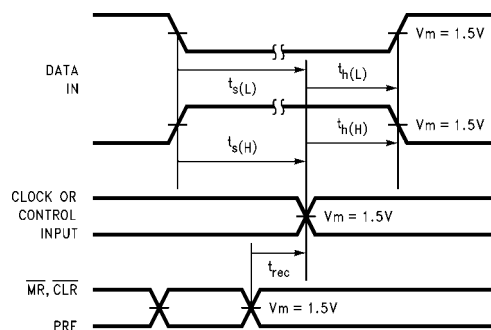
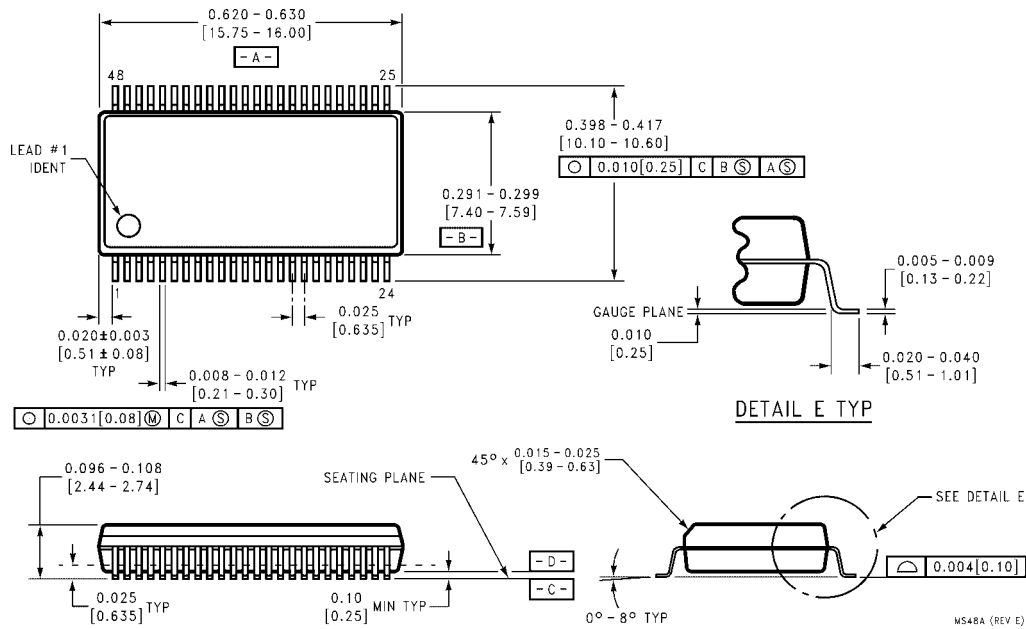


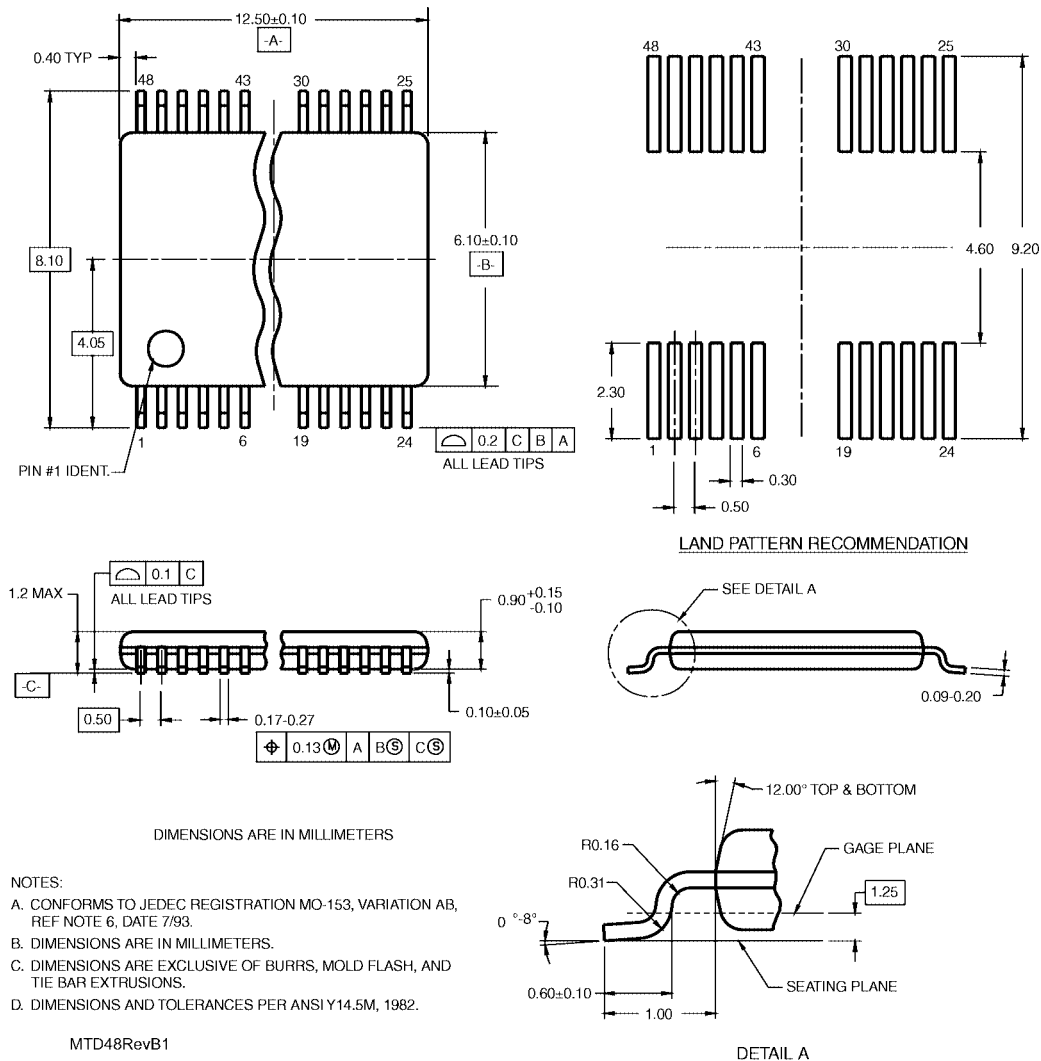
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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