REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02, 03, and 04. Editorial changes throughout.	92-10-02	Monica L. Poelking
B	Changes in accordance with NOR 5962-R061-93.	93-01-07	Monica L. Poelking
C	Add device types 05, 06, 07, and 08 Add case outline X. Modify boilerplate to include class N. Editorial changes throughout.	96-06-28	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	C	C	C	C																
SHEET	15	16	17	18																

REV STATUS OF SHEETS															
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Tim Noh

CHECKED BY
Tim Noh

APPROVED BY
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DRAWING APPROVAL DATE
91-08-29

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS SINGLE CHIP 8-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-91566

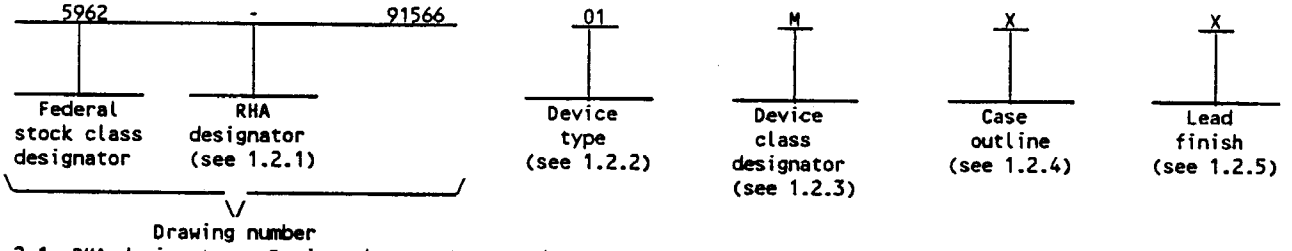
SHEET 1 OF 18

DESC FORM 193
JUL 94

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	87C751	CMOS 8-bit microcontroller with 2 kilobytes EPROM memory
02	87C751	CMOS 8-bit microcontroller with 2 kilobytes one time programmable EPROM memory
03 1/	87C751-16	CMOS 8-bit microcontroller with 2 kilobytes EPROM memory
04	87C751-16	CMOS 8-bit microcontroller with 2 kilobytes one time programmable EPROM memory
05	87C751	CMOS 8-bit microcontroller (3.5 to 12 MHz) one time programmable EPROM memory
06	87C751-16	CMOS 8-bit microcontroller (3.5 to 16 MHz) one time programmable EPROM memory
07	87C751	CMOS 8-bit microcontroller (3.5 to 12 MHz) one time programmable EPROM memory
08	87C751-16	CMOS 8-bit microcontroller (3.5 to 16 MHz) one time programmable EPROM memory

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 2/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L 1/	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
X	MS-001-AF 3/	24	Plastic dual-in-line package
3 1/	CQCC1-N28	28	Square chip carrier package

1/ For device types 01 and 03, lid shall be transparent to permit ultraviolet light erasure.
2/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.
3/ See JEDEC Publication 95.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 4/

Supply voltage range (except P0.2/V_{PP})	-0.5 V to +6.5 V
Voltage (any pin) to V_{SS}	-0.5 V dc to +6.5 V dc
Voltage from (P0.2/V_{PP}) to V_{SS}	-0.5 V to +13 V
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	
Cases L and 3	See MIL-STD-1835
Case X	25°C/W
Maximum junction temperature (T_J)	+175°C
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	5.0 V dc ±10 percent
Case operating temperature range (T_C)	
Device types 01-04	-55°C to +125°C
Device types 05-06	-40°C to +85°C
Device types 07-08	-40°C to +125°C
Maximum low level input voltage:	
All (except SDA, SCL)	0.2 V_{CC} - 0.1 V
SDA and SCL	0.3 V_{CC}
Minimum high level input voltage:	
All (except SDA, SCL, X1, and RST)	0.2 V_{CC} + 1.1 V
SDA and SCL	0.7 V_{CC}
X1 and RST	0.7 V_{CC} + 0.2 V
Oscillator frequency:	
Devices 01, 02, 05, and 07	3.5 MHz to 12 MHz
Devices 03, 04, 06, and 08	3.5 MHz to 16 MHz

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Values will be added when they become available.

2.2 Non-Government publication. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the sloicitaion. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

(Applications for copies should be addressed to the Electronic Industry Association, 2500 Wilson Boulevard, Arlington, VA 2201-3834).

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.11.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output low voltage, ports 1 and 3	V_{OL}	I_{OL} = 1.6 mA	V_{CC} = 4.5 V, V_{IN} = V_{IH} min, V_{IL} max	1,2,3	All		0.45	V
Output low voltage, ports 0.2	V_{OL1}	I_{OL} = 3.2 mA		1,2,3	All		0.45	
Ports 0.0 and 0.1 (I^2C)-drivers, output low voltage	V_{OL2}	I_{OL} = 3 mA (over V_{CC} range)		1,2,3	All		0.4	
Output high voltage, ports 1 and 3	V_{OH}	I_{OH} = -60 µA	V_{CC} = 4.5 V, V_{IN} = V_{IH} min, V_{IL} max	1,2,3	All	2.4		V
		I_{OH} = -25 µA				0.75 V_{CC}		
		I_{OH} = -10 µA				0.90 V_{CC}		
Logic 0 input current, ports 1 and 3	I_{IL}	V_{IN} = 0.45 V, V_{CC} = 5.5 V		1,2,3	All	0	-75	µA
Logic 1 to 0 transition current ports 1 and 3	I_{TL}	V_{IN} = 2.0 V, V_{CC} = 5.5 V				0	-750	
Input leakage current, port 0	I_{LI}	V_{IN} = V_{CC}	V_{CC} = 5.5 V			0	10	
		V_{IN} = 0.45 V				0	-10	
Reset pull down resistor	R_{RST}			1,2,3	All	25	175	kΩ
Power down current	I_{PD} 3/	V_{CC} = 3 V to 5.5 V		1,2,3	All		50	µA
Program voltage	V_{PP} 4/	V_{SS} = 0 V, V_{CC} = 4.5 V to 5.5 V		1	All	12.5	13.0	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Program current	I_{PP} 4/	V_{PP} = 13.0 V		1,2,3	All			mA
Supply current	I_{CC}	$V_{IL} = V_{SS} \pm 0.5$ V $V_{IH} = V_{CC} - 0.5$ V Port 0 = V_{CC}	Active 5/	1,2,3	01,02, 05,07		19	
					03,04, 06,08		22	
			Idle 6/	1,2,3	01,02, 05,07		3.9	
					03,04, 06,08		4.5	
Oscillator freq.	$1/t_{CLCL}$	See figure 3		1,2,3	All	3.5	12	MHz
Reset time (RST pulse width)	RST 7/			1,2,3	All	$24t_{CLCL}$		ns
Pin capacitance	C_{IO}	Test freq. = 1 MHz, see 4.4.1c		4	All		10	pF
Driver, receiver combined capacitance	C_D	See 4.4.1c		4	All		10	pF
Functional tests		See 4.4.1b, V_{CC} = 4.5 V, 5.5 V		7, 8	All			
External clock	t_{CHCX}	High time	freq. = 12 MHz See figure 3	9,10,11	All	20		ns
	t_{CLCX}	Low time				20		
	t_{CLCH} 4/	Rise time					20	
	t_{CHCL} 4/	Fall time					20	

1/ Load capacitance for ports is 80 pF. All test shall be performed under the worst-case conditions unless otherwise specified.
2/ For operating temperatures see 1.4.
3/ Power down I_{CC} is measured with all output pins disconnected; port 0 = V_{CC}; X2, X1 = no connect; RST = V_{SS}.
4/ Guaranteed to the limits specified, if not tested.
5/ I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5 ns, X2 = no connect, RST = V_{CC}. I_{CC} will be slightly higher if a crystal is used. When idle I_{CC} is measured, set RST = V_{SS}.
6/ Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = SNS, X2 = no connect, RST = V_{SS}.
7/ To ensure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up plus $24t_{CLCL}$. Guaranteed to the limit specified herein.

Device type	All	
Case outline	L, X	3
Terminal number	Terminal symbol	
1	P3.4/A4	P3.4/A4
2	P3.3/A3	P3.3/A3
3	P3.2/A2/A10	P3.2/A2/A10
4	P3.1/A1/A9	P3.1/A1/A9
5	P3.0/A0/A8	NC
6	P0.2/V_{PP}	P3.0/A0/A8
7	P0.1/SDA/$\overline{OE}$	P0.2/V_{PP}
8	P0.0/SCL/ASEL	P0.1/SDA/$\overline{OE}$
9	RST	P0.0/SCL/ASEL
10	X2	NC
11	X1	RST
12	V_{SS}	X2
13	P1.0/D0	X1
14	P1.1/D1	V_{SS}
15	P1.2/D2	P1.0/D0
16	P1.3/D3	P1.1/D1
17	P1.4/D4	P1.2/D2
18	P1.5/$\overline{INT0}$/D5	P1.3/D3
19	P1.6/$\overline{INT1}$/D6	P1.4/D4
20	P1.7/T0/D7	P1.5/$\overline{INT0}$/D5
21	P3.7/A7	NC
22	P3.6/A6	NC
23	P3.5/A5	P1.6/$\overline{INT1}$/D6
24	V_{CC}	P1.7/T0/D7
25	---	P3.7/A7
26	---	P3.6/A6
27	---	P3.5/A5
28	---	V_{CC}

FIGURE 1. Terminal connections.

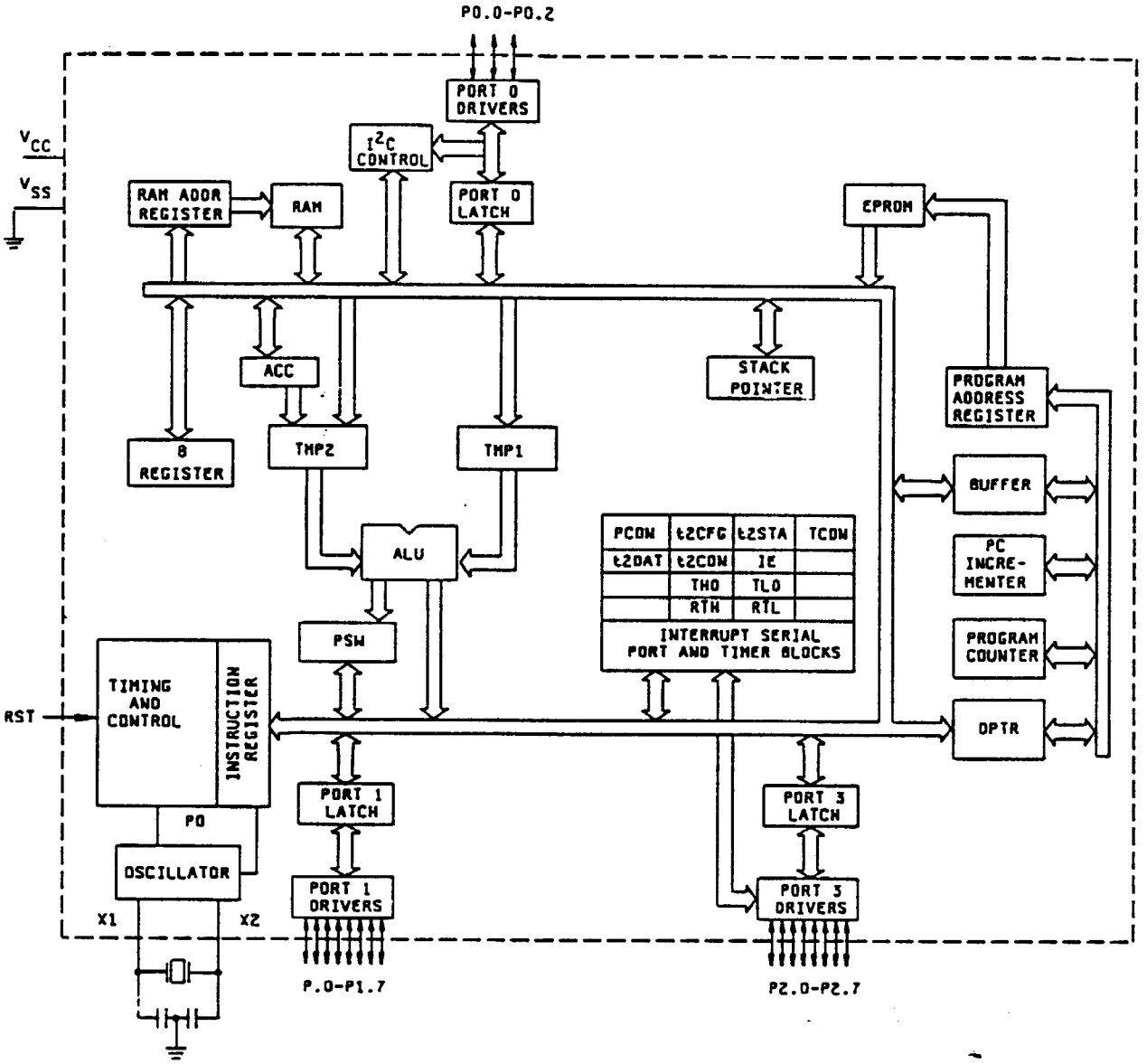
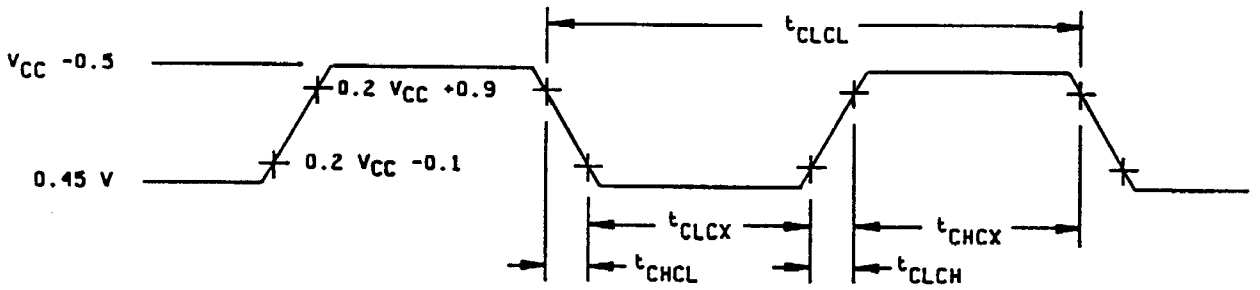
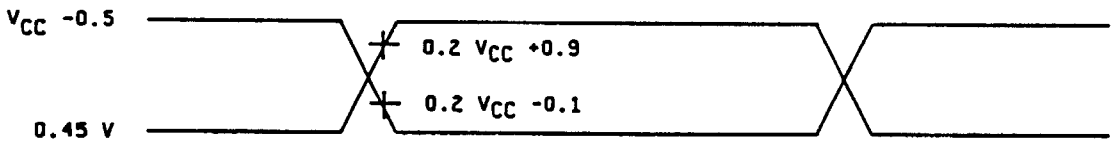


FIGURE 2. Block diagram.



EXTERNAL CLOCK DRIVE WAVEFORM



AC TESTING INPUT AND OUTPUT WAVEFORM

FIGURE 3. Timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at 140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = 5.9 V at 25°C using loose timing (i.e., T_{ACC} > 1 µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_m = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B.

(1) Program at +25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_m = 5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table IIA.

(6) For device types 01 and 03, program 100 percent of the bits and verify (see 3.11.2).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA. For device types 02, 04, 05, 06, 07 and 08, the virgin state of the device must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01 and 03, erase. Devices may be submitted for groups B, C, and D at this time.

(11) For device types 01 and 03, verify erasure (see 3.11.3). Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IO} and C_D measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. For device type 01 and 03, all devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. For device types 02, 04, 05 - 08, unprogrammed devices shall be tested for programmability and functionality compliant to the requirements of group A, subgroups 7 and 8, by one of the following methods:

(1) Testing the entire lot using additional built in test circuitry which allows the manufacturer to verify programmability and functionality without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 7 and 8, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 7 and 8. Twelve devices shall be submitted to programming. If more than 2 device fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. (Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 7 and 8. If more than 2 total devices fail, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. For devices 01 and 03, all devices selected for testing shall be programmed with a checkerboard parrern or equivalent. after completion of all testing, the devices shall be erased and verified.

e. For devices 02, 04, 05 - 08, the virgin state of the device must be verified.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 $W·s/cm^2$. Exposing the EPROM to an ultraviolet lamp of 12,000 $\mu W/cm^2$ rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 4) for programming. The waveforms of figures 5, and 6, and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

TABLE III. EPROM programming and verification characteristics.

Parameter	Symbol	Conditions	Limits		Unit
			Min	Max	
Programming supply voltage	V_{PP}	See figure 6, T_A = 21°C to 27°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V	12.5	13.0	V
Programming supply current	I_{PP}			10	mA
Oscillator frequency	$1/t_{CLCL}$		4	6	MHz
Address setup to PROG low	t_{AVGL} 1/		10 µs+24t_{CLCL}		ns
Address hold after PROG	t_{GHAX}		48t_{CLCL}		
Data setup to $\overline{PROG}$ low	t_{DVGL}		38t_{CLCL}		
Data hold after PROG	t_{GHDX}		36t_{CLCL}		
V_{PP} setup to $\overline{PROG}$ low	t_{SHGL}		10		µs
V_{PP} hold after $\overline{PROG}$	t_{GHSL}		10		
$\overline{PROG}$ width	t_{GLGH}		90	110	
V_{PP} low to data valid	t_{AVQV} 2/			48t_{CLCL}	ns
$\overline{PROG}$ high to $\overline{PROG}$ low	t_{GHGL}		10		µs
P0.0 (sync pulse) low	t_{SYNL}		4t_{CLCL}		ns
P0.0 (sync pulse) high	t_{SYNH}		8t_{CLCL}		ns

1/ Address should be valid at least 24t_{CLCL} before rising edge of p0.2(V_{PP}).

2/ For a pure verify mode; i.e., no program mode in between, t_{AVQV} is 14t_{CLCL} maximum.

3/ P0.1 is indicated with $\overline{PROG}$.

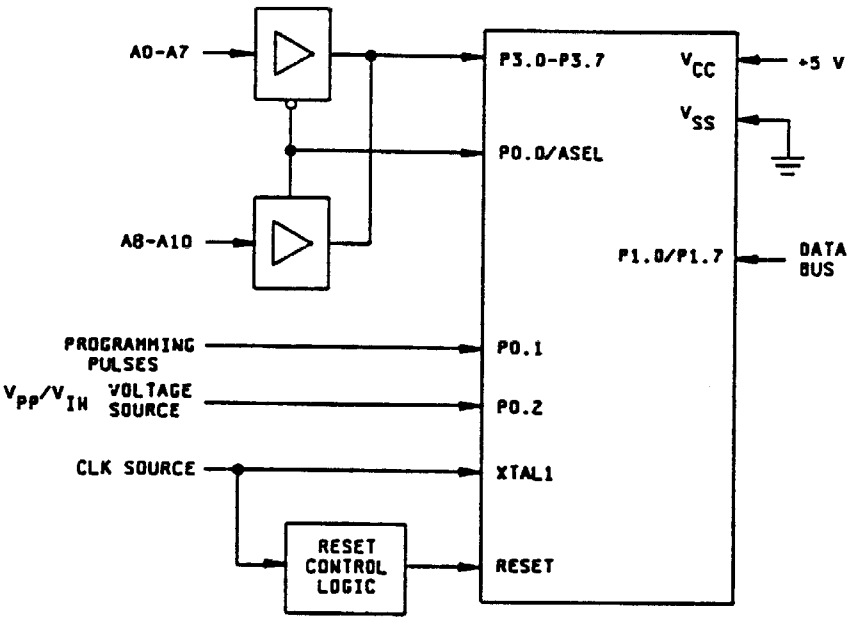


FIGURE 4. Programming configuration.

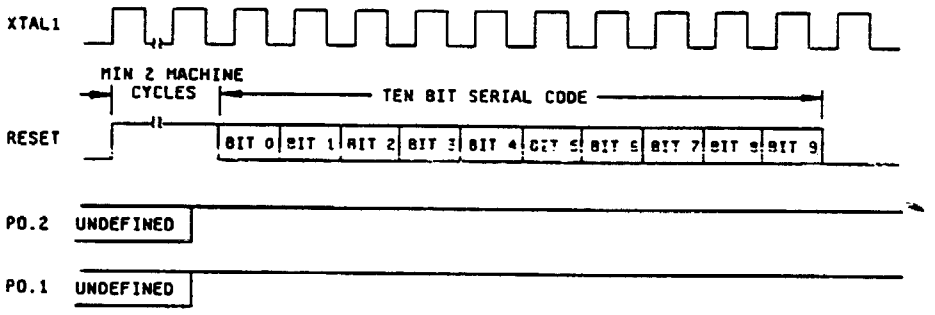
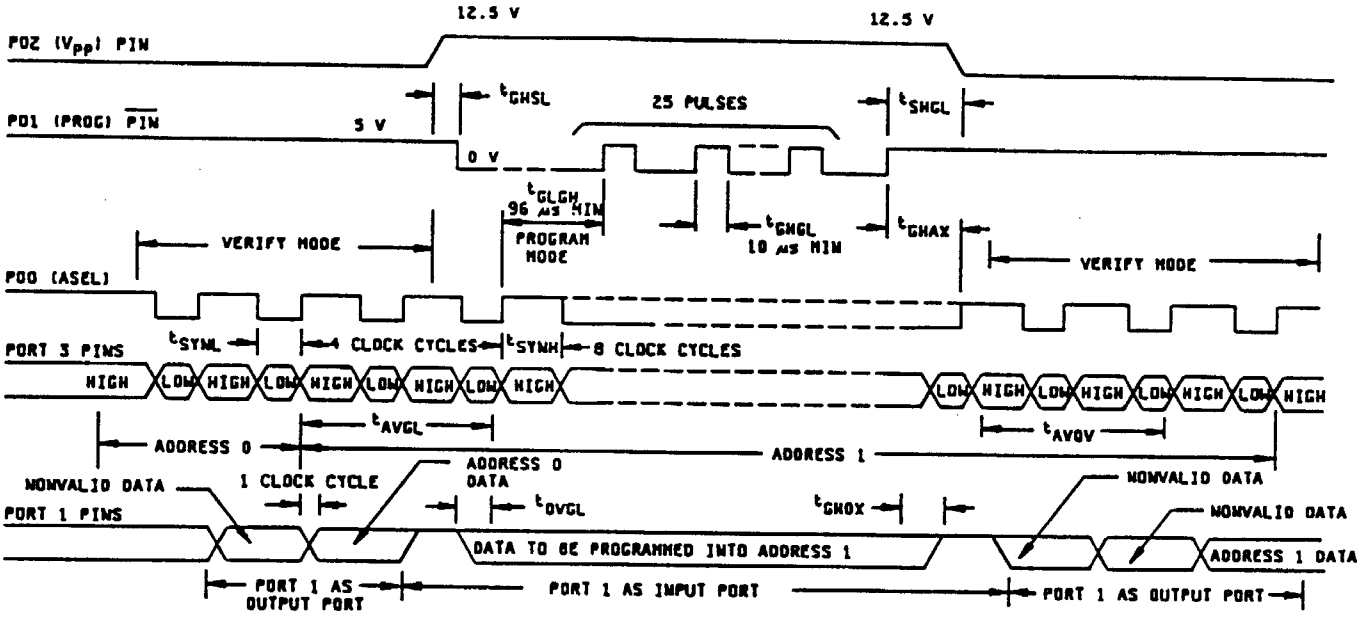


FIGURE 5. Entry into program verify modes.



NOTE:
1. Assume address 0 is programmed in previous cycle. The waveforms shown above consist of:
   a. Verify the data programmed in address 0 in previous program cycle.
   b. Program a data byte in address 1.
   c. Verify the data porgrammed in address 1.

FIGURE 6. Program/verify cycle.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Port 0. Port 0 is an 3-bit open drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 also serves as the serial I^2C interface as shown in the pinout diagram. When this feature is activated by software, SCL and SDA are driven low in accordance with the I^2C protocol. These pins are driven low if the port register bit is written with a 0 or if the I^2C system presents a 0. The state of the pin can always be read from the port register by the program. Port 1 also receives the low-order address bytes during program verification.

To comply with the specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from standard TTL characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-I^2C applications.

SPA (P0.1) I^2C data.
SCL (P0.0) I^2C clock.
Port 0 also provides alternate functions for programming the EPROM memory as follows.

P0.0/ASEL - output which selects which byte of the EPROM address is to be applied to port 3.
P0.0-0 presents the low address byte to port 3.
P0.0-1 presents the high address byte to port 3(only the three least significant bits are used).

P0.1/OE/PGM - input, OE/PGM, which specifies verify mode (output enable) or the program mode.
OE/PGM - 1 output enabled (verify mode).
OE/PGM - 0 program mode.

P0.2/V_{pp} programming voltage input.

6.5.2 Port 1. Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups. Port 1 also serves the special function features as listed below:

$\overline{INT0}$ (P1.5): External interrupt
INT1 (P1.6): External interrupt
T0 (P1.7): Timer 0 external input

Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode.

6.5.3 Port 3. Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in the state can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups. Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 11-bit address is multiplexed into this port as specified by P0.0.

6.5.4 RST. Reset: A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to reset places the device in the programming state allowing programming address, data and V_{PP} to be applied for programming or verification purposes. The reset serial sequence must be synchronized with the X1 input.

6.5.5 X1. Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into reset to place the device in the programming state.

6.5.6 X2. Crystal 2: Output from the inverting oscillator amplifier.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-06-28

Approved sources of supply for SMD 5962-91566 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9156601MLA 5962-9156601M3A	18324	87C751/BLA 87C751/B3A
5962-9156602MLA 5962-9156602M3A	18324	87C751/BLA-OT 87C751/B3A-OT
5962-9156603MLA 5962-9156603M3A	18324	87C751-16/BLA 87C751-16/B3A
5962-9156604MLA	18324	87C751-16/BLAOT
5962-9156605NXA	18324	87C751/IN24A
5962-9156606NXA	18324	87C751-16/IN24A
5962-9156607NXA	18324	87C751/CN24A
5962-9156608NXA	18324	87C751-16/CN24A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Philips Semiconductor 990 Benecia Ave Sunnyvale CA 94086 Point of contact: 811 E. Arques Avenue Sunnyvale, CA 94086