

# PROCESS CP316

## Small Signal Transistor

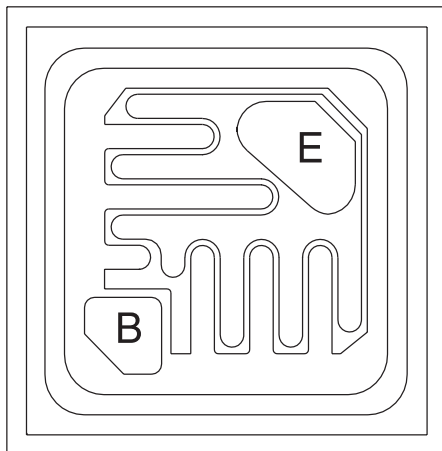
[查询"NPN"供应商](#) High Voltage Transistor Chip

**Central**<sup>TM</sup>  
Semiconductor Corp.

### PROCESS DETAILS

|                          |                  |
|--------------------------|------------------|
| Process                  | EPITAXIAL PLANAR |
| Die Size                 | 20 x 20 MILS     |
| Die Thickness            | 9.0 MILS         |
| Base Bonding Pad Area    | 4.0 x 4.0 MILS   |
| Emitter Bonding Pad Area | 4.7 x 4.7 MILS   |
| Top Side Metalization    | Al - 30,000Å     |
| Back Side Metalization   | Au - 18,000Å     |

### GEOMETRY



BACKSIDE COLLECTOR R0

### GROSS DIE PER 4 INCH WAFER

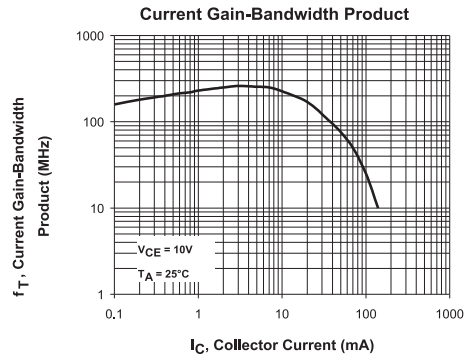
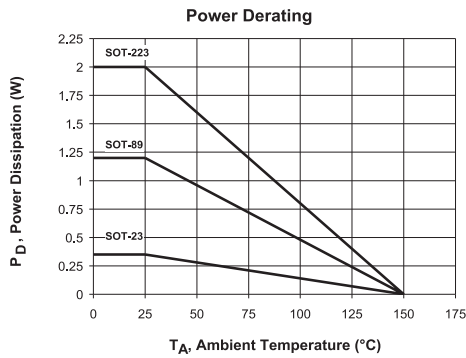
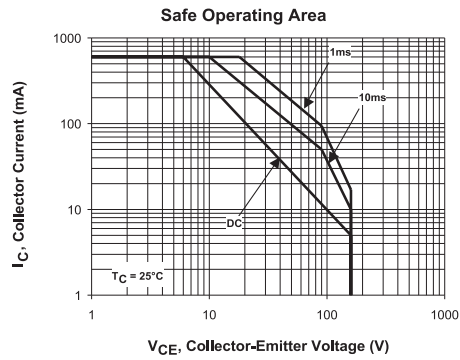
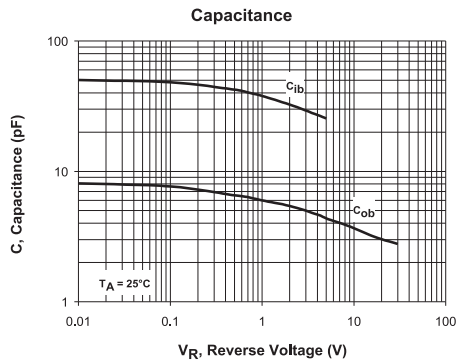
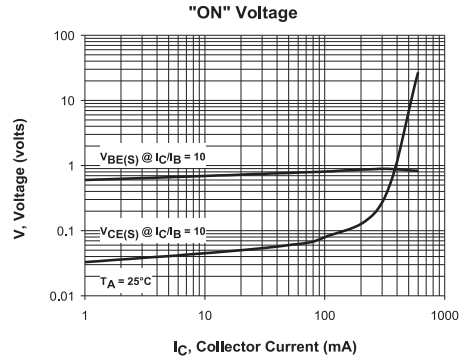
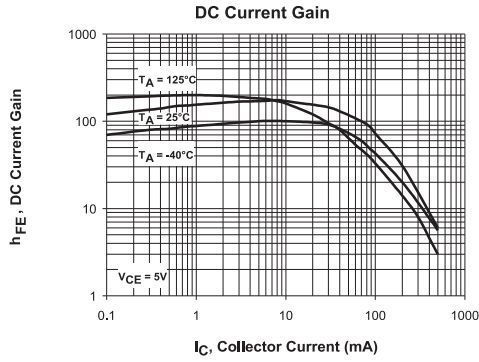
29,250

### PRINCIPAL DEVICE TYPES

CMPT5551  
CXT5551  
CZT5551  
2N5551

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