11.3 Gbps Limiting Transimpedance Amplifier With RSSI

Check for Samples: ONET8501T

FEATURES

- 10 GHz Bandwidth
- 7 kΩ Differential Small Signal Transimpedance
- 2.5 mA$_{PP}$ Input Overload Current
- Received Signal Strength Indication (RSSI)
- 100mW Typical Power Dissipation
- CML Data Outputs With On-Chip 50Ω Back-Termination
- On Chip Supply Filter Capacitor
- Single 3.3V Supply
- Die Size: 940 × 1195 μm

APPLICATIONS

- SONET OC-192
- SFP+ Optical Receivers
- 10x Fibre Channel Optical Receivers
- 10G Ethernet Receivers
- PIN Preamplifier-Receivers
- APD Preamplifier Receivers

DESCRIPTION

The ONET8501T is a high-speed, high gain, limiting transimpedance amplifier used in optical receivers with data rates up to 12.5Gbps. It features low input referred noise, 10GHz bandwidth, 7kΩ small signal transimpedance, and a received signal strength indicator (RSSI).

The ONET8501T is available in die form, includes an on-chip V$_{CC}$ bypass capacitor and is optimized for packaging in a TO can.

The ONET8501T requires a single 3.3V ±10% supply and its power efficient design typically dissipates less than 105mW. The device is characterized for operation from −40°C to 100°C case (IC back side) temperature.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM

A simplified block diagram of the ONET8501T is shown in Figure 1.

The ONET8501T consists of the signal path, supply filters, a control block for dc input bias, automatic gain control (AGC) and received signal strength indication (RSSI). The RSSI provides the bias for the TIA stage and the control for the AGC.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered V_{CC} for the PIN photodiode and for the transimpedance amplifier.

The DC input bias circuit and automatic gain control use internal low pass filters to cancel the dc current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry to monitor the received signal strength is provided.
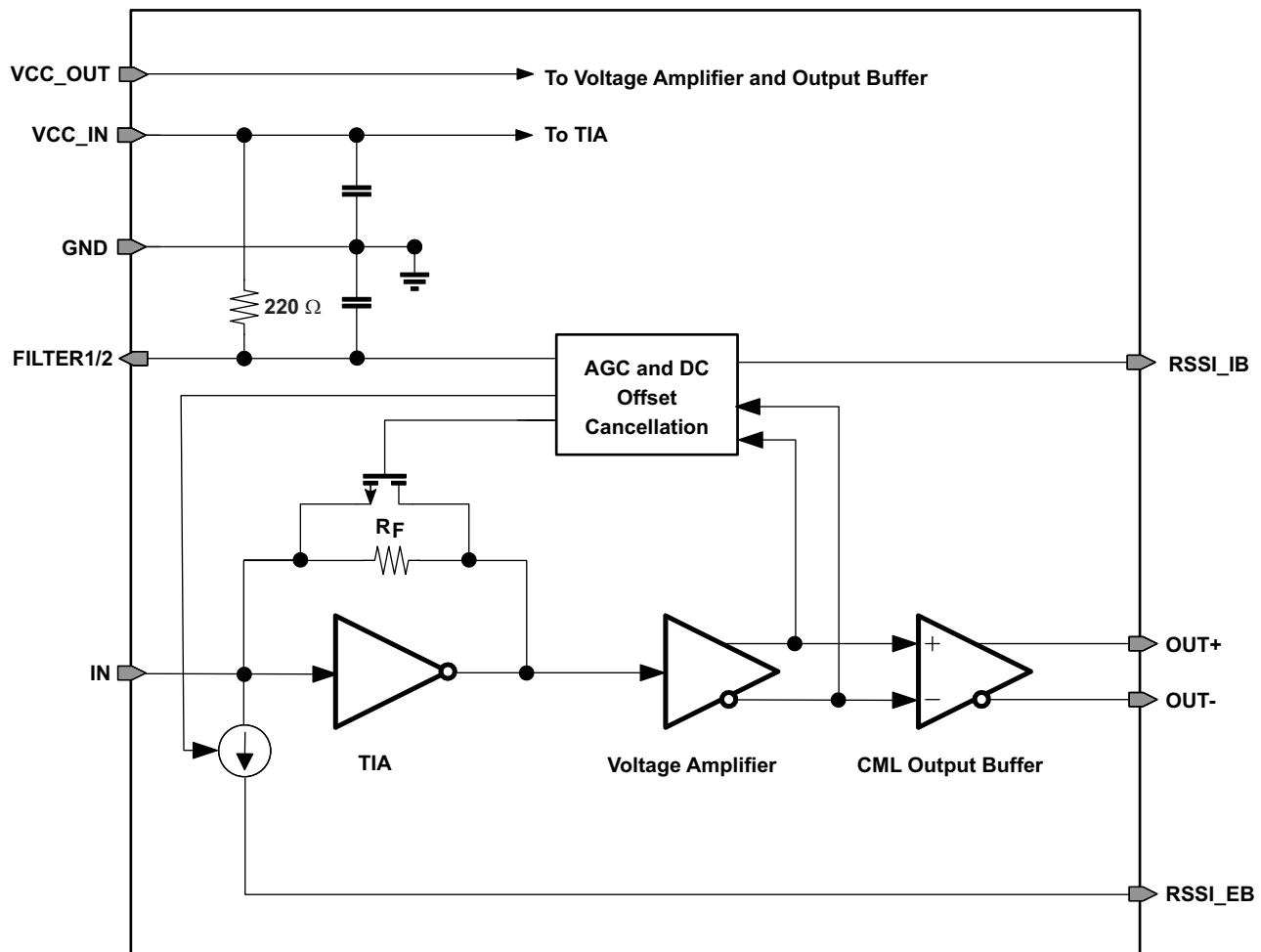

Figure 1. Simplified Block Diagram of the ONET8501T

Product Folder Link(s): *ONET8501T*

BOND PAD ASSIGNMENT

The ONET8501T is available in die form. The locations of the bondpads are shown in Figure 2.
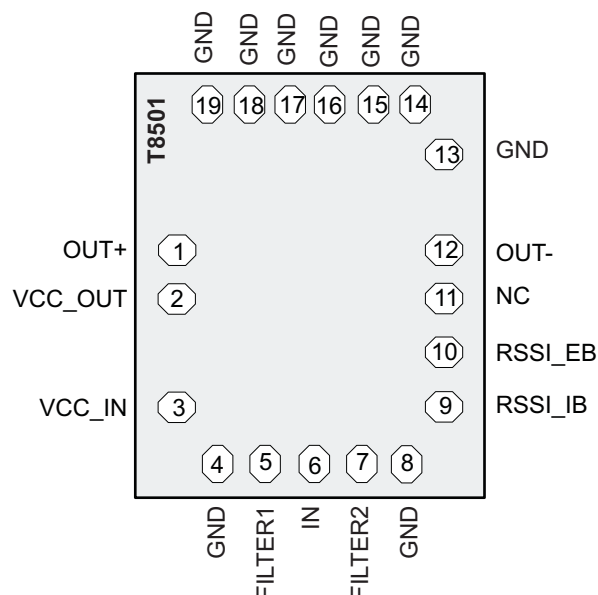
Figure 2. Bond Pad Assignment of ONET8501T

PIN FUNCTIONS

PIN NAME	PIN NO.	TYPE	DESCRIPTION
GND	4, 8, 13–19	Supply	Circuit ground. All GND pads are connected on die. Bonding all pads is optional; however, for optimum performance a good ground connection is mandatory.
OUT+	1	Analog output	Non-inverted CML data output. On-chip 50Ω back-terminated to V_{CC}.
VCC_OUT	2	Supply	2.97V–3.63V supply voltage for the voltage and CML amplifiers.
VCC_IN	3	Supply	2.97V–3.63V supply voltage for input TIA stage.
FILTER	5, 7	Analog	Bias voltage for photodiode cathode. These pads are internally connected to an 220Ω resistor to V_{CC} and a filter capacitor to ground (GND).
IN	6	Analog input	Data input to TIA (photodiode anode).
RSSI_EB	10	Analog output	Optional use when operated with external PD bias (e.g. APD). Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC} – 0.65V. If the RSSI feature is not used this pad should be left open.
RSSI_IB	9	Analog output	Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI) if the photo diode is biased from the TIA. Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC} – 0.65V. If the RSSI feature is not used this pad should be left open.
OUT–	12	Analog output	Inverted CML data output. On-chip 50Ω back-terminated to V_{CC}.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
V_I	Supply voltage[2] at VCC_IN, VCC_OUT	–0.3 to 4.0	V
	Voltage at FILTER1, FILTER2, OUT+, OUT–, RSSI_IB, RSSI_EB[2]	–0.3 to 4.0	V
I_I	Current into IN	–0.7 to 3.5	mA
	Current into FILTER1, FILTER2	–8 to 8	mA
I_O	Continuous current at outputs at OUT+, OUT-	–8 to 8	mA
ESD	ESD rating at all pins except input IN, RSSI_IB, and RSSI_EB	2	kV (HBM)
	ESD rating at RSSI_IB and RSSI_EB	1	kV(HBM)
	ESD rating at input IN	0.5	kV(HBM)
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
T_A	Operating backside die temperature		–40		100[1]	°C
L	Wire-bond inductor at pins FILTER and IN			0.3	0.5	nH
C_{PD}	Photodiode Capacitance			0.2		pF

(1) 105°C maximum junction temperature

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{CC}	Supply current	Input current I_{IN} < 1500 µA$_{PP}$	21	28	41[1]	mA
		Input current I_{IN} < 2500 µA$_{PP}$			44[1]	
V_{IN}	Input bias voltage		0.75	0.85	0.98	V
$R_{(OUT)}$	Output resistance	Single-ended to V_{CC}	40	50	60	Ω
$R_{(FILTER)}$	Photodiode filter resistance			220		Ω

(1) Including RSSI current

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V_{CC} = +3.3 V and T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Z	Small signal transimpedance	Differential output; Input current i_{IN} = 20 µA$_{PP}$	5,000	7,000	10,000	Ω
$f_{(HSS,3dB)}$	Small signal bandwidth	i_{IN} = 16 µA$_{PP}$ [1]	7	10		GHz
$f_{(L,3dB)}$	Low frequency −3 dB bandwidth	16 µA < i_{IN} < 2000 µA$_{PP}$		30	100	kHz
$i_{(N,IN)}$	Input referred RMS noise	10 GHz bandwidth [2]		0.9	1.6	µA
$S_{(US)}$	Unstressed sensitivity	10.3125 Gbps, PRBS31 pattern, 850 nm, BER 10^{-12}		−14		dBm
D_J	Deterministic jitter	16 µA$_{PP}$ < i_{IN} < 500 µA$_{PP}$ (10.3125 Gbps, PRBS31 pattern)		6	11	ps$_{PP}$
		500 µA$_{PP}$ < i_{IN} < 2000 µA$_{PP}$ (10.3125 Gbps, PRBS31 pattern)		6	13	
$D_{J(OL)}$	Overload deterministic jitter	2000 µA$_{PP}$ < i_{IN} < 2500 µA$_{PP}$ (K28.5 pattern)		6	15	ps$_{PP}$
$V_{OUT,D,MAX}$	Maximum differential output voltage	Input current i_{IN} = 200 µA$_{PP}$	240	280	350	mV$_{PP}$
A_{RSSI_IB}	RSSI gain internal bias	Resistive load to GND [3]	0.48	0.5	0.52	A/A
	RSSI internal bias output offset current (no light) [4]		3.5	10	16	µA
A_{RSSI_EB}	RSSI gain external bias	Resistive load to GND [3]	0.43		0.6	A/A
	RSSI external bias output offset current (no light)			25		µA
PSNR	Power supply noise rejection	F < 10 MHz [5], supply filtering according to SFF8431		−15		dB

(1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF and the bond-wire inductance is 0.3 nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
(2) Input referred RMS noise is (RMS output noise)/ (gain at 100 MHz).
(3) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSI does not exceed V_{CC} − 0.65V.
(4) Offset is added to improve accuracy below 5µA. When measured without input current (no light) the offset can be subtracted as a constant offset from RSSI measurements.
(5) PSNR is the differential output amplitude divided by the voltage ripple on supply; no input current at IN.

DETAILED DESCRIPTION

SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier which converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip 50Ω back-termination to V_{CC}.

FILTER CIRCUITRY

The FILTER pins provide a filtered V_{CC} for a PIN photodiode bias. The on-chip low pass filter for the photodiode is implemented using a filter resistor of 220Ω and a capacitor. The corresponding corner frequency is below 5MHz. The supply voltages for the transimpedance amplifier are filtered by means of on-chip capacitors, thus avoiding the necessity to use an external supply filter capacitor. The input stage has a separate V_{CC} supply (VCC_IN) which is not connected on chip to the supply of the limiting and CML stages (VCC_OUT).

AGC AND RSSI

The voltage drop across the internal photodiode supply-filter resistor is monitored by the bias and RSSI control circuit block in the case where a PIN diode is biased using the FILTER pins.

If the dc input current exceeds a certain level then it is partially cancelled by means of a controlled current source. This keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance.

The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally this circuit block senses the current through the filter resistor and generates a mirrored current that is proportional to the input signal strength. The mirrored current is available at the RSSI_IB output and can be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSI_IB pad does not exceed $V_{CC} - 0.65V$.

If an APD or PIN photodiode is used with an external bias then the RSSI_EB pin should be used. However, for greater accuracy under external photo diode biasing conditions, it is recommended to derive the RSSI from the external bias circuitry.

![Texas Instruments]

TYPICAL OPERATION CHARACTERISTICS

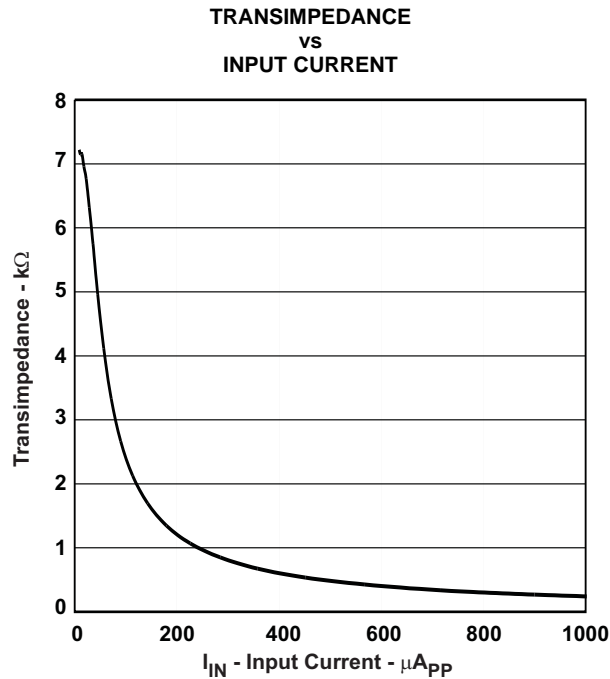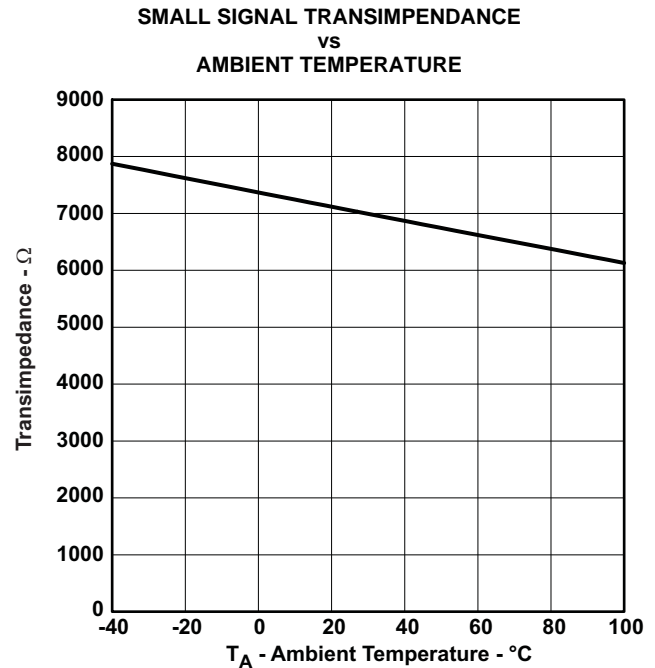Typical Operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

**TRANSIMPEDANCE
vs
INPUT CURRENT**

Figure 3.

**SMALL SIGNAL TRANSIMPENDANCE
vs
AMBIENT TEMPERATURE**

Figure 4.

**SMALL SIGNAL TRANSFER
CHARACTERISTICS**

Figure 5.

**SMALL SIGNAL BANDWIDTH
vs
AMBIENT TEMPERATURE**
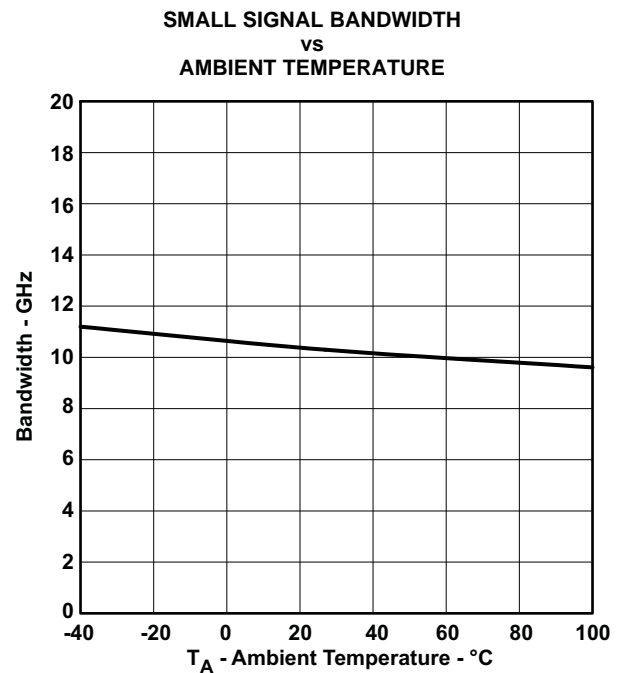

Figure 6.

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TYPICAL OPERATION CHARACTERISTICS (continued)

Typical Operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

OUTPUT VOLTAGE
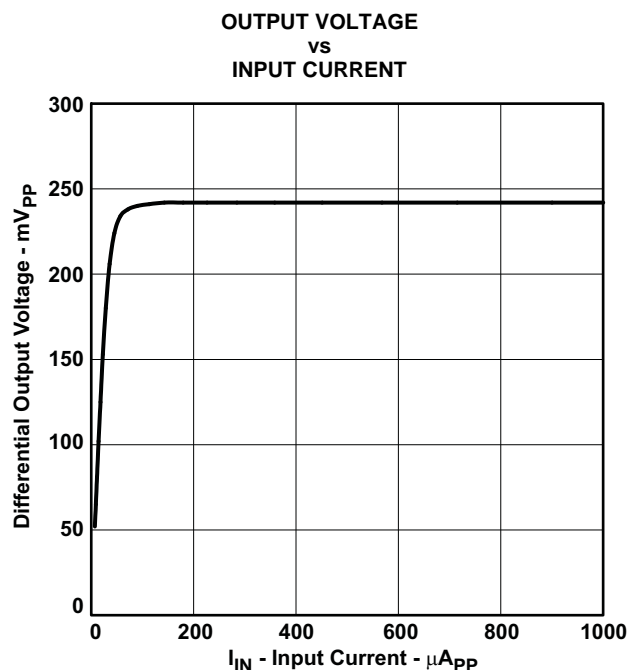**vs**
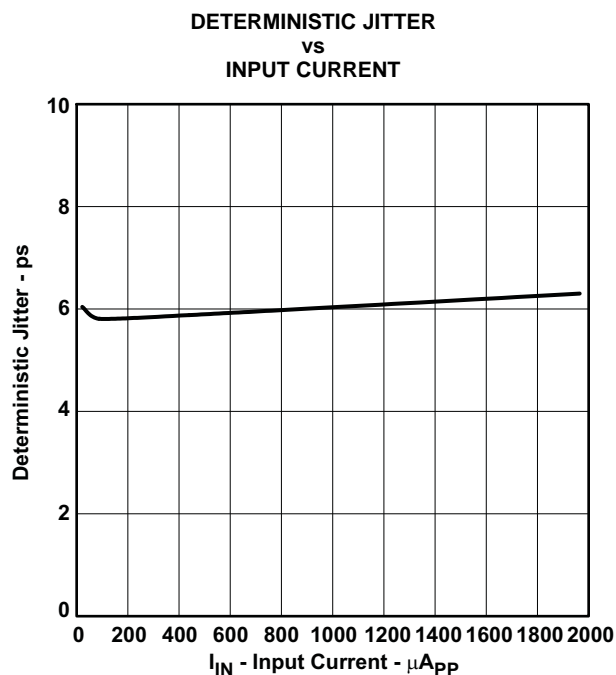**INPUT CURRENT**

Figure 7.

DETERMINISTIC JITTER
vs
INPUT CURRENT

Figure 8.

RSSI_IB OUTPUT CURRENT
vs
AVERAGE INPUT CURRENT

Figure 9.

POWER SUPPLY NOISE REJECTION
vs
FREQUENCY

Figure 10.

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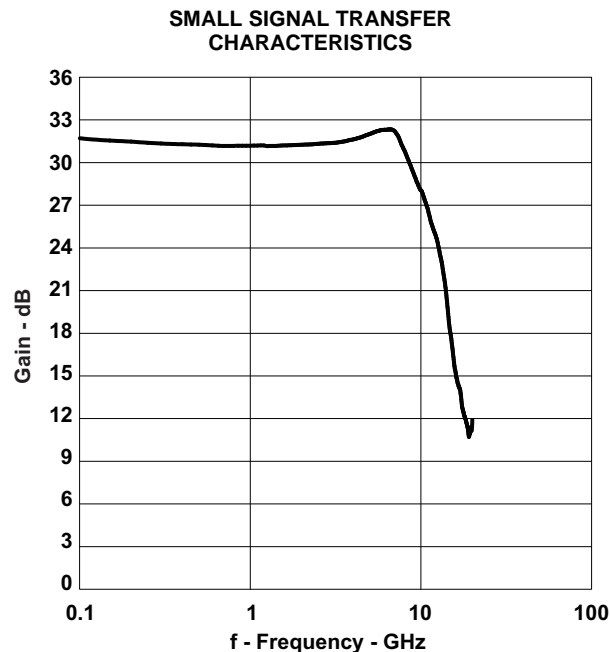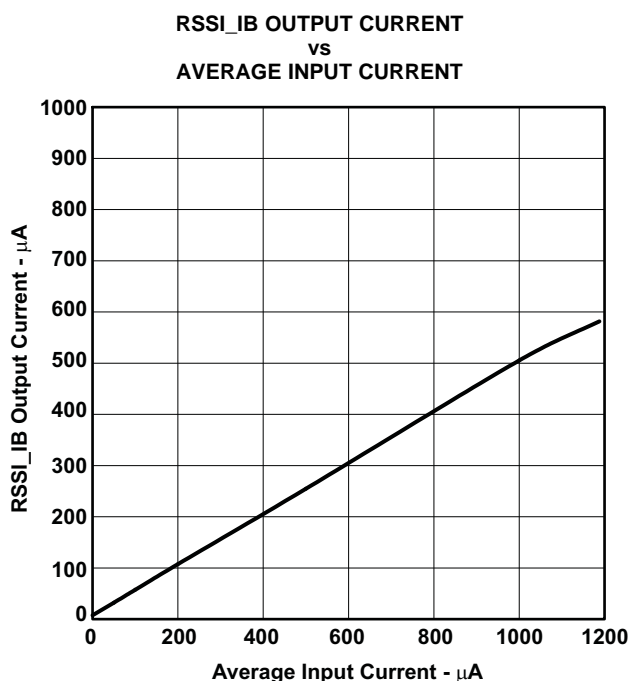
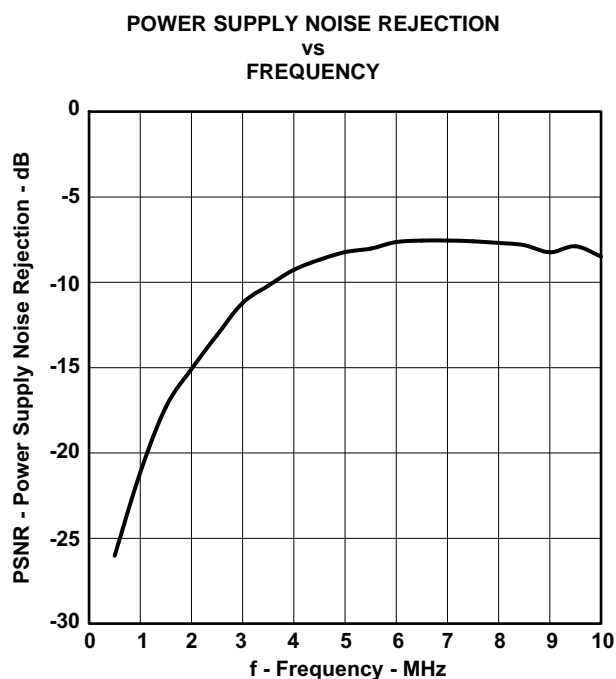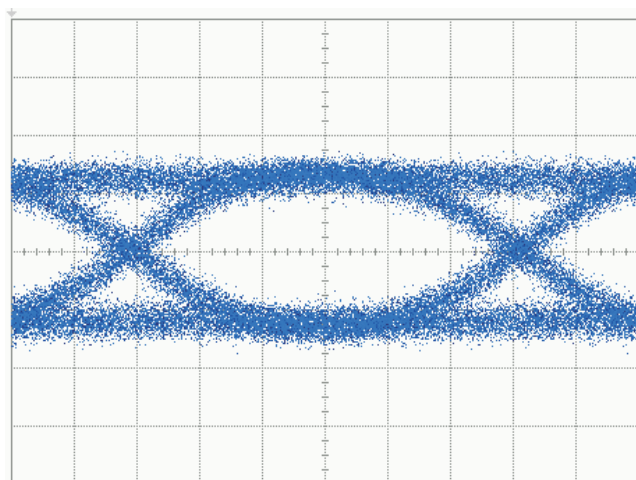## TYPICAL OPERATION CHARACTERISTICS (continued)

Typical Operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS
AND 20 μA$_{PP}$ INPUT CURRENT**

60 mVdiv   15.6 ps/div

Figure 11.

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS
AND 100 μA$_{PP}$ INPUT CURRENT**

100 mV/div   15.6 ps/div

Figure 12.

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS
AND 500 μA$_{PP}$ INPUT CURRENT**

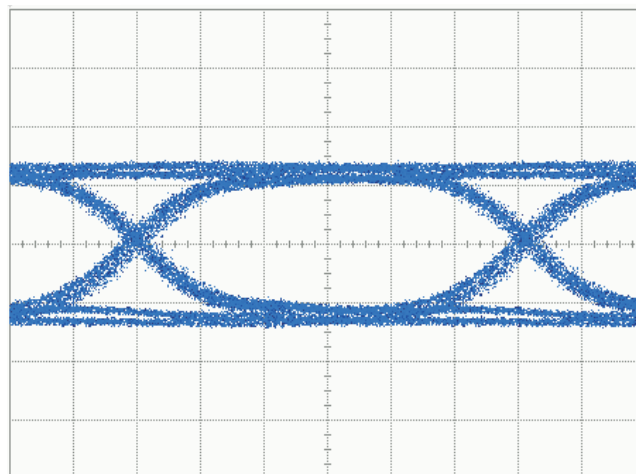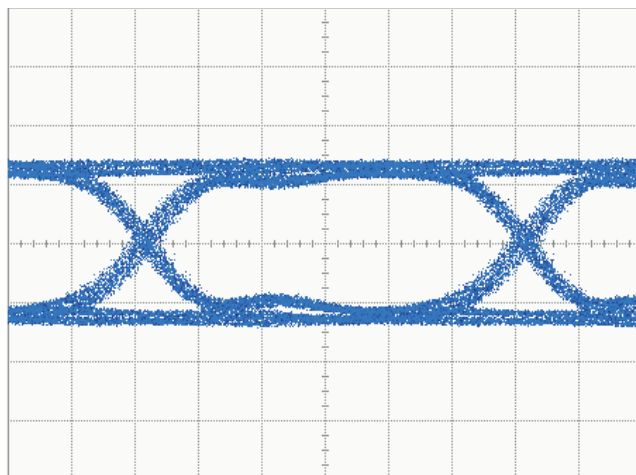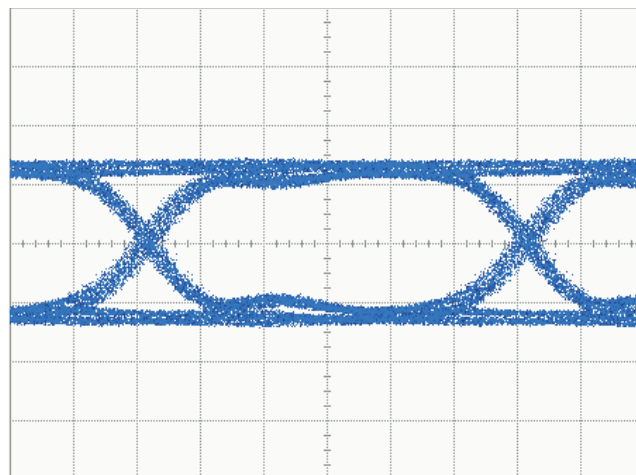100 mV/div   15.6 ps/div

Figure 13.

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS
AND 2 mA$_{PP}$ INPUT CURRENT**

100 mV/div   15.6 ps/div

Figure 14.

APPLICATION INFORMATION

Figure 15 shows the ONET8501T used in a typical fiber optic receiver using the internal photodiode bias. The ONET8501T converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER inputs provide a dc bias voltage for the PIN that is low pass filtered by the combination of an internal 220Ω resistor and a capacitor. Because the voltage drop across the 220Ω resistor is sensed and used by the bias circuit, the photodiode must be connected to the FILTER pads for the bias to function correctly.

The RSSI output is used to mirror the photodiode output current and can be connected via a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET8501T, ensure that the voltage at RSSI never exceeds $V_{CC} - 0.65V$. If the RSSI output is not used while operating with internal PD bias, it should be left open.

The OUT+ and OUT– pins are internally terminated by 50Ω pull-up resisters to V_{CC}. The outputs must be ac coupled, for example by using 0.1μF capacitors, to the succeeding device.
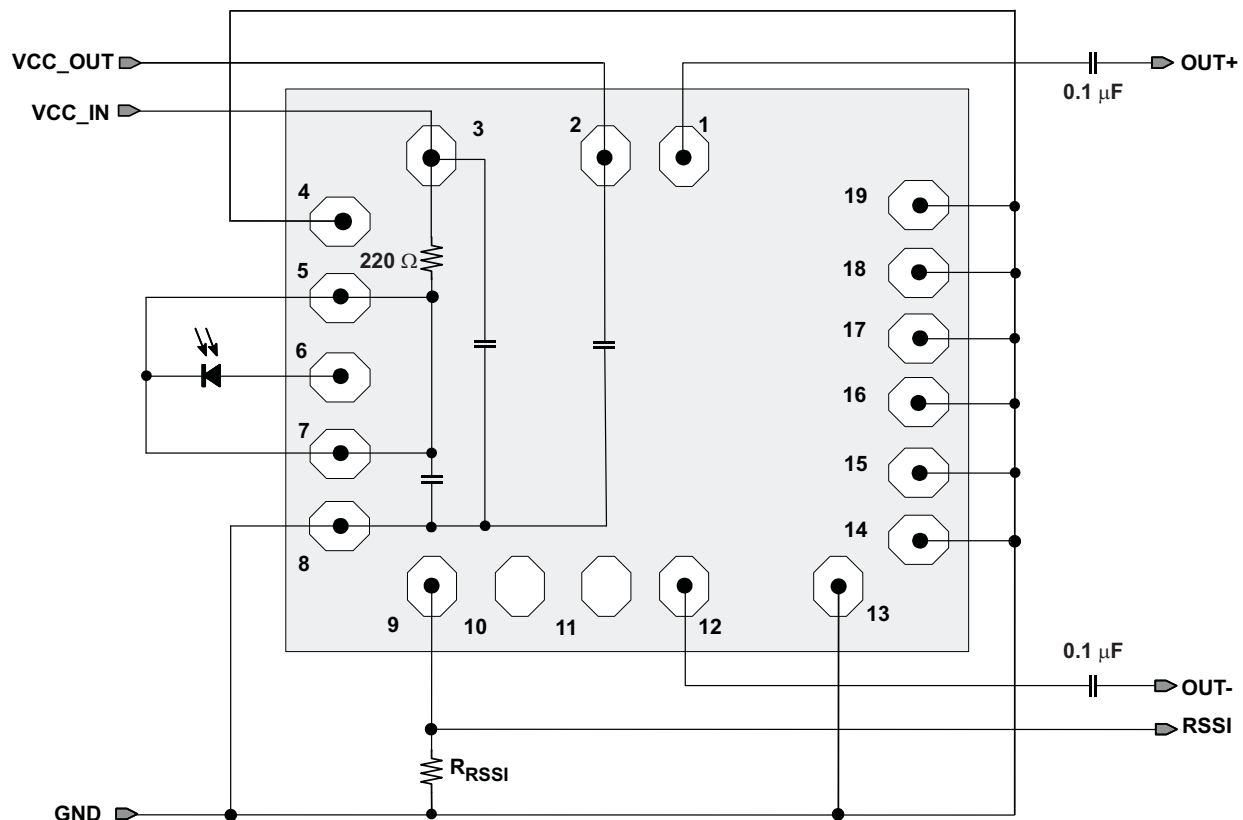

Figure 15. Basic Application Circuit for PIN Receivers

Product Folder Link(s): *ONET8501T*

Figure 16 shows the ONET8501T being used in a typical fiber optic receiver using an external photodiode bias for an APD photodiode. This configuration can also be used for a PIN diode if desired. The external bias RSSI signal is based on a dc offset value and is not as accurate as the internal bias RSSI signal which is based upon the photodiode current.
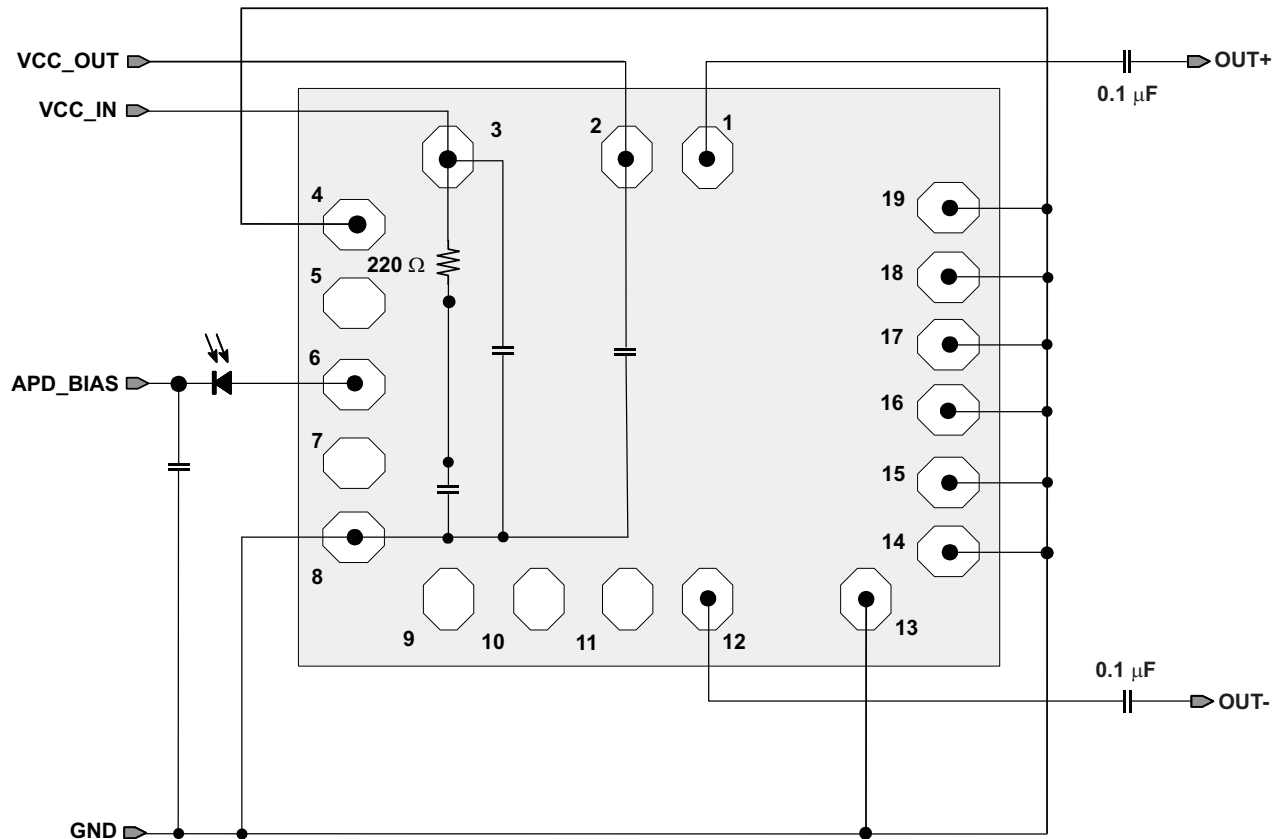

Figure 16. Basic Application Circuit for APD Receivers

ASSEMBLY RECOMMENDATIONS

Careful attention to assembly parasitics and external components is necessary to achieve optimal performance.

Recommendations that optimize performance include:

1. Minimize the total capacitance on the IN pad by using a low capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET8501T die in order to minimize the bond wire length and thus the parasitic inductance.
2. Use identical termination and symmetrical transmission lines at the ac coupled differential output pins OUT+ and OUT−.
3. Use short bond wire connections for the supply terminals VCC_IN, VCC_OUT and GND. Supply voltage filtering is provided on chip but filtering may be improved by using an additional external capacitor.

CHIP DIMENSIONS AND PAD LOCATIONS
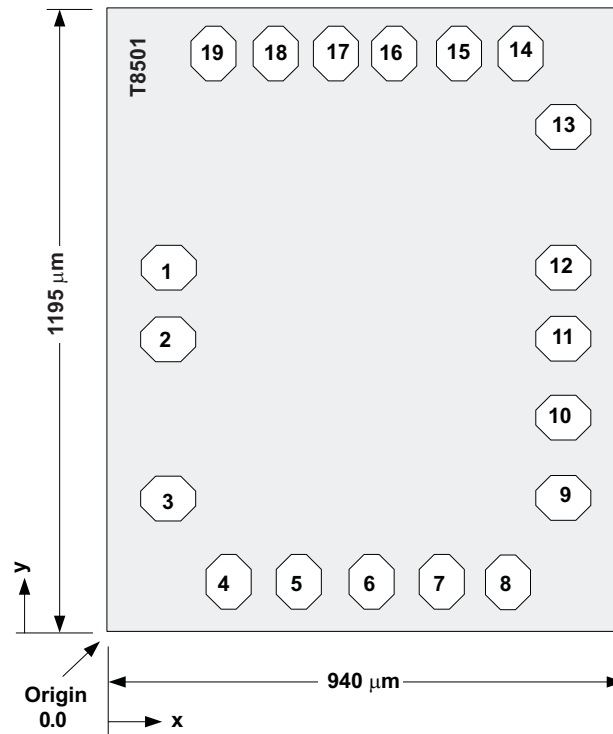
Die Thickness: 203 ± 13 µm

Pad Dimensions: 105 × 65 µm

Die Size: 940 ± 20 µm × 1195 ± 20 µm

PAD	COORDINATES		SYMBOL	TYPE	DESCRIPTION
	x (µm)	y (µm)			
1	116	739	OUT+	Analog output	Non-inverted data output
2	116	575	VCC_OUT	Supply	3.3V supply voltage
3	116	289	VCC_IN	Supply	3.3V supply voltage
4	243	136	GND	Supply	Circuit ground
5	358	136	FILTER1	Analog	Bias voltage for photodiode
6	473	136	IN	Analog input	Data input to TIA
7	588	136	FILTER2	Analog	Bias voltage for photodiode
8	703	136	GND	Supply	Circuit ground
9	828	289	RSSI_IB	Analog output	RSSI output signal for internally biased receivers
10	828	404	RSSI_EB	Analog output	RSSI output signal for externally biased receivers
11	828	575	NC		Not connected
12	828	739	OUT–	Analog output	Inverted data output
13	828	910	GND	Supply	Circuit ground
14	760	1063	GND	Supply	Circuit ground
15	645	1063	GND	Supply	Circuit ground
16	530	1063	GND	Supply	Circuit ground
17	415	1063	GND	Supply	Circuit ground
18	300	1063	GND	Supply	Circuit ground
19	185	1063	GND	Supply	Circuit ground

Product Folder Link(s): *ONET8501T*

TO46 LAYOUT EXAMPLE

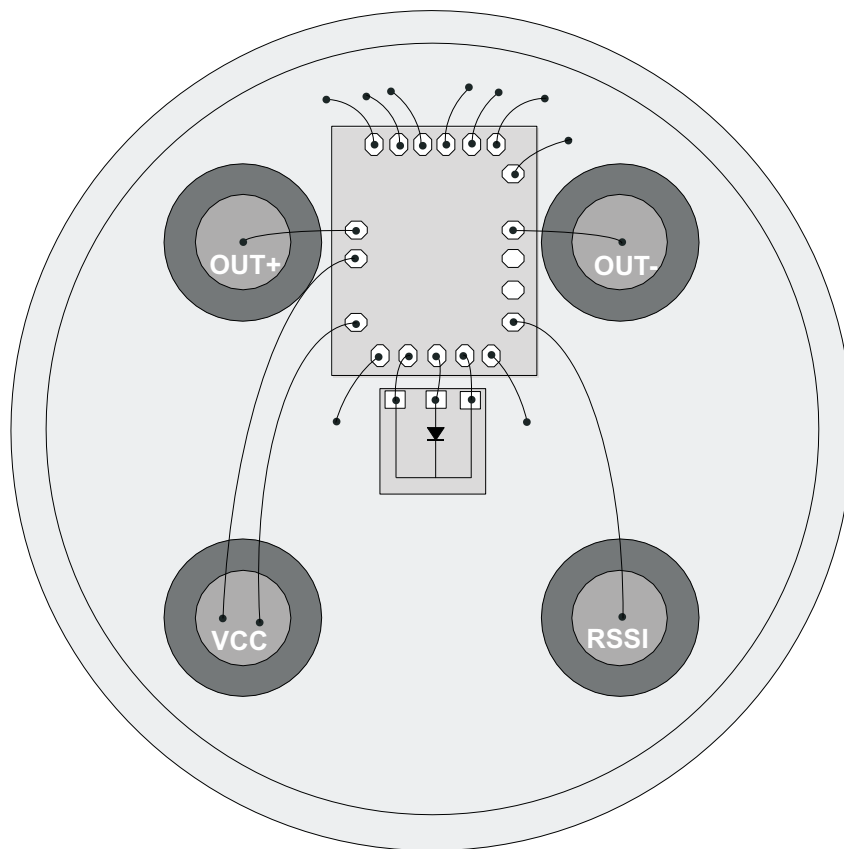An example for a layout (top view) in a 5 pin TO46 can is shown in Figure 17.

Figure 17. TO46 5 Pin Layout Using the ONET8501T With Dual Cathode PIN Diode

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ONET8501TY	ACTIVE	DIESALE	Y	0	360	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type
ONET8501TYS	ACTIVE	DIESALE	Y	0	4500	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type

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OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Interface	interface.ti.com	Energy	www.ti.com/energy
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