

August 1998

100363 Low Power Dual 8-Input Multiplexer

General Description

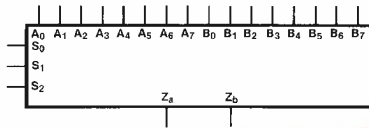
The 100363 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b , respectively). The same bit (0–7) will be selected for both the Z_a and Z_b output. All inputs have 50 k Ω pulldown resistors.

- 2000V ESD protection
- Pin/function compatible with 100163
- Voltage compensated operating range = -4.2V to -5.7V
- Standard Microcircuit Drawing (SMD) 5962-9165501

Features

- 50% power reduction of the 100163

Logic Symbol

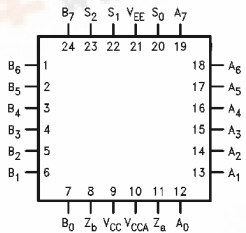


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Pin Names	Description
S_0 – S_2	Data Select Inputs
A_0 – A_7	A Data Inputs
B_0 – B_7	B Data Inputs
Z_a , Z_b	Data Outputs

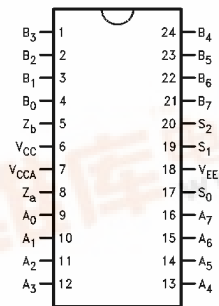
Connection Diagrams

24-Pin Quad Cerpak



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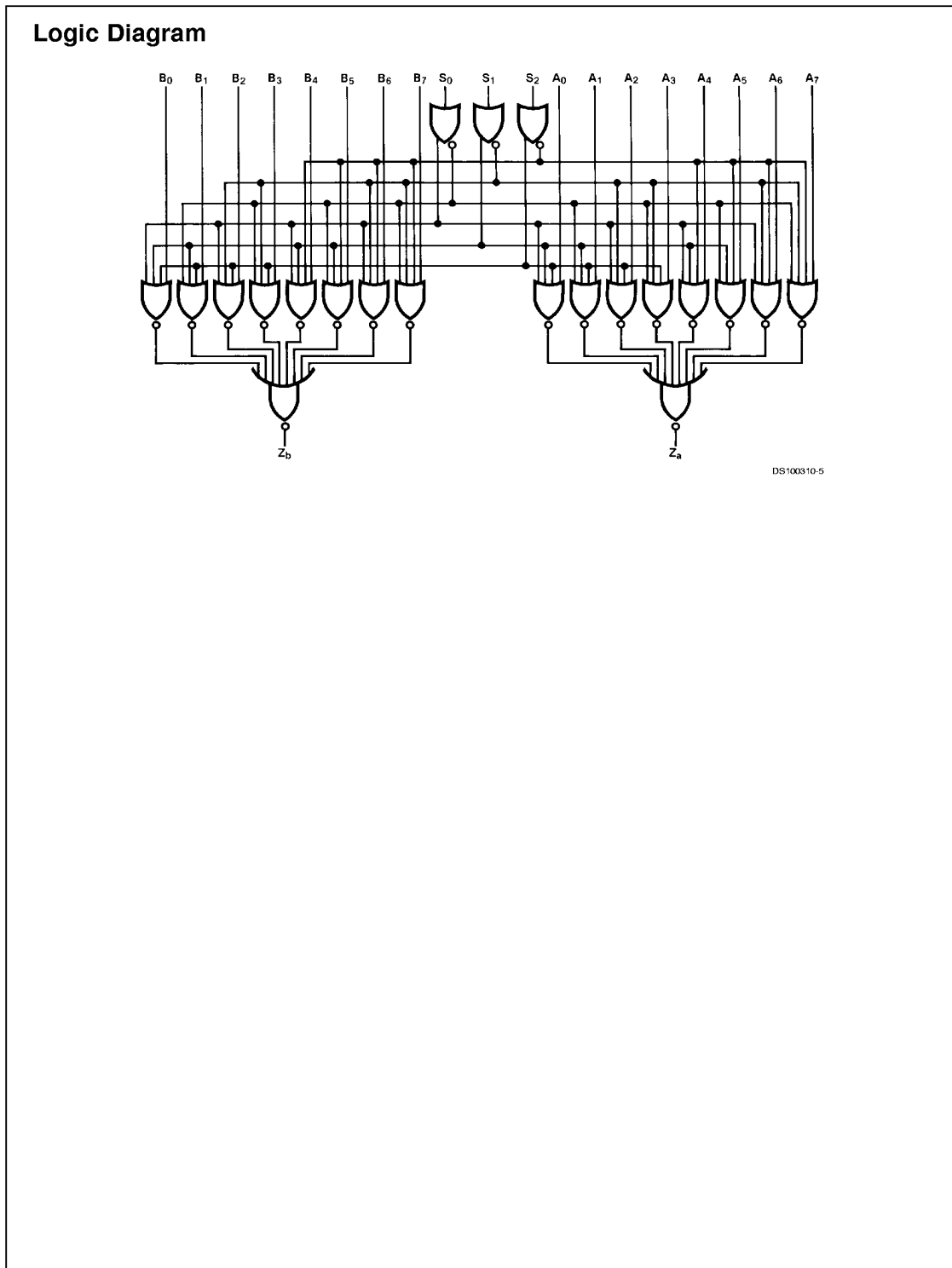
24-Pin DIP



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100363 Low Power Dual 8-Input Multiplexer





Truth Table

Select			Inputs									Outputs	
S ₂	S ₁	S ₀	Data									Z _a	Z _b
			A ₇ B ₇	A ₆ B ₆	A ₅ B ₅	A ₄ B ₄	A ₃ B ₃	A ₂ B ₂	A ₁ B ₁	A ₀ B ₀			
L	L	L										L	L
L	L	L										H	H
L	L	H									L		L
L	L	H								H			H
L	H	L							L				L
L	H	L							H				H
L	H	H						L					L
L	H	H						H					H
H	L	L				L							L
H	L	L				H							H
H	L	H			L								L
H	L	H			H								H
H	H	L		L									L
H	H	L		H									H
H	H	H	L										L
H	H	H	H										H

H = HIGH Voltage Level
 L = LOW Voltage Level
 Blank = X = Don't Care

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.50	2.40	0.60	2.30	0.70	3.00	ns	Figure 1 and Figure 2	(Notes 7, 8, 9)
t_{PHL}	A_0-A_7, B_0-B_7 to Output									
t_{PLH}	Propagation Delay	0.80	3.00	0.90	2.80	0.80	3.40			
t_{PHL}	S_0-S_2 to Output									(Note 10)
t_{TLH}	Transition Time	0.30	1.90	0.30	1.80	0.30	2.10	ns		
t_{THL}	20% to 80%, 80% to 20%									

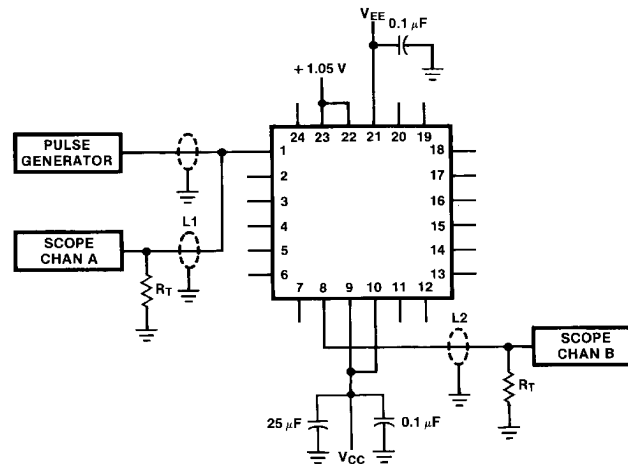
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$, temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry



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Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}

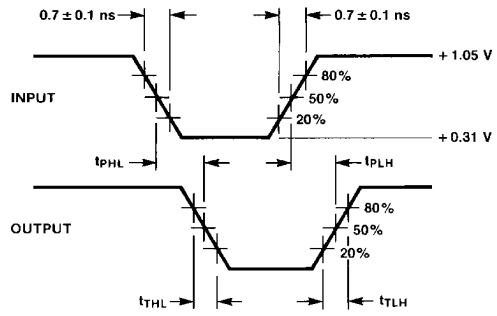
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

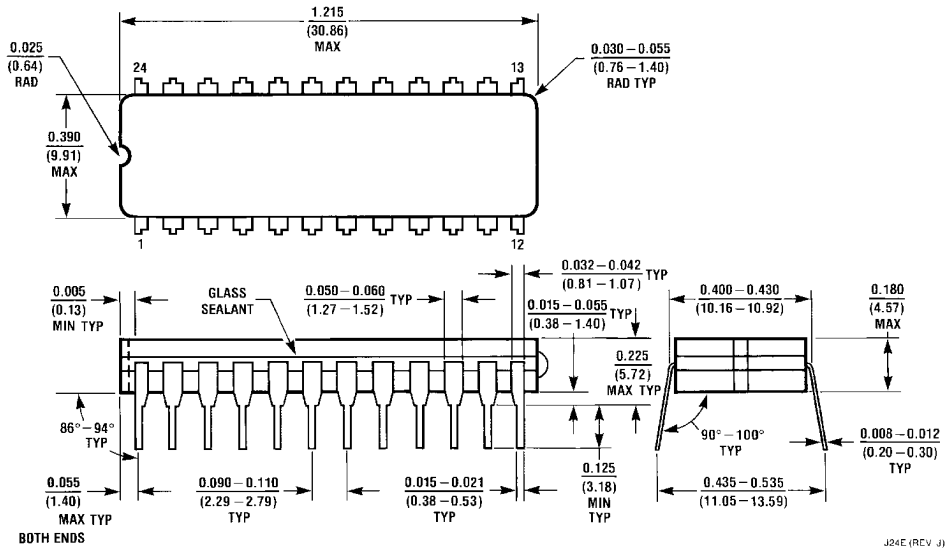
Switching Waveforms



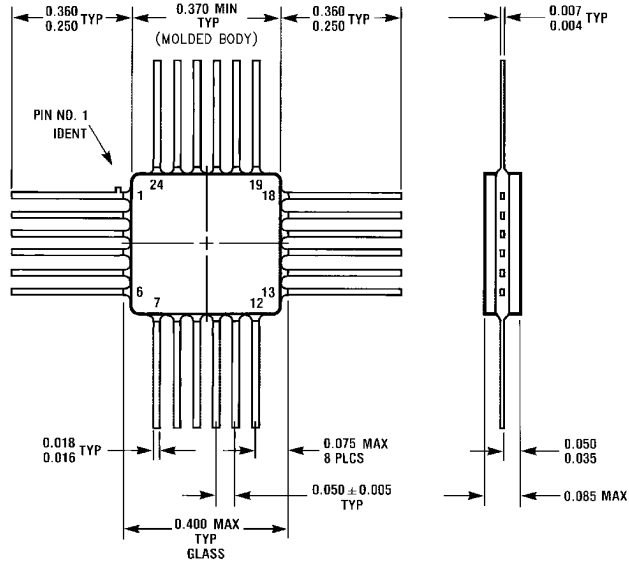
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FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Pin Quad Cerpak (F)
NS Package Number W24B