High-Speed, Fully Differential, Programmable-Gain Amplifier

Check for Samples: PGA870

FEATURES

- **Wideband +5-V Operation: 650-MHz Bandwidth**
- **Low Impedance, Voltage Mode Output**
- **Wide Gain Range: –11.5 dB to +20 dB**
- **Precise 0.5-dB Gain Steps**
  Step-to-Step Gain Error = ±0.03 dB
- **HD_2: –93 dBc at 100 MHz**
- **HD_3: –88 dBc at 100 MHz**
- **IMD_3: –98 dBc at 100 MHz, –95 dBc at 200 MHz**
- **OIP3: +47 dBm at 100 MHz;**
  Exceeds +45 dBm for Frequencies to 300 MHz
- **Flexible Gain Control Interface:**
  - **Supports latched and unlatched options**
  - **Gain may be set in power-down state**
  - **Fast setup and hold times: 2.5 ns**
- **Low Disable Current: 2 mA**
- **Pb-Free (RoHS-Compliant) and Green Package**

APPLICATIONS

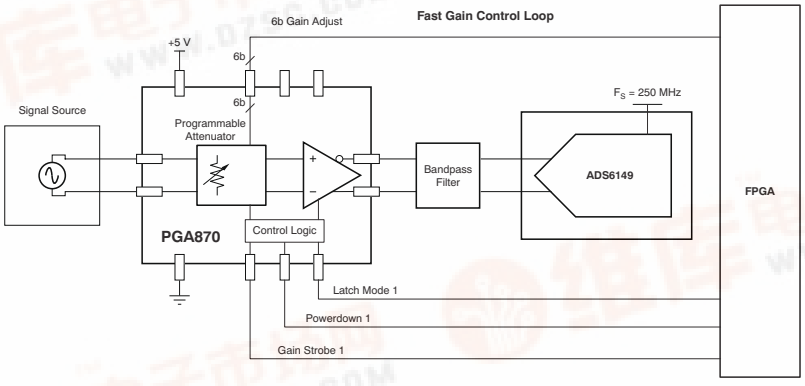
- **Programmable Gain IF Amplifier:**
  - **Differential signal chains**
  - **Single-ended to differential conversion**
- **Fast Gain Control Loops for:**
  - **Test/measurement**
  - **Digital radio signal chains**
- **ADC Driver for Wireless Base Station Signal Chains: GSM, WCDMA, MC-GSM**
- **Radar/Ranging Systems**

DESCRIPTION

The PGA870 is a wideband programmable-gain amplifier (PGA) for high-speed signal chain and data acquisition systems. The PGA870 has been optimized to provide high bandwidth, low distortion, and low noise, making it ideally suited as a 14-bit analog-to-digital converter (ADC) driver for wireless base station signal chain applications. The wide gain range of –11.5 dB to +20 dB can be adjusted in 0.5-dB gain steps through a 6-bit control word applied to the parallel interface. The gain control interface may be configured as a level-triggered latch or an edge-triggered latch, or it may be placed in an unlatched (transparent) mode. In addition to the 6-bit gain control, the PGA870 contains a power-down pin (PD) that can be used to put the device into a low-current, power-down mode. In this mode, the quiescent current drops to 2 mA, but the gain control circuitry remains active, allowing the gain of the PGA870 to be set before device power-up. The PGA870 is offered in a QFN-28 PowerPAD™ package.

RELATED PRODUCTS

DEVICE	DESCRIPTION
THS4509	Wideband, low-noise, low-distortion, fully differential amplifier
THS7700	High-speed, fully differential 16-bit ADC driver
THS9000	50-MHz to 400-MHz IF/RF Amplifier
ADS6149	14-Bit, 250-MSPS ADC with DDR LVDS/CMOS Outputs
ADS6145	14-Bit, 125-MSPS ADC with DDR LVDS/CMOS Outputs



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA870	QFN-28	RHD	–40°C to +85°C	PGA870	PGA870IRHDT	Tape and Reel, 250
				PGA870	PGA870IRHDR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		PGA870	UNIT
Power supply		6	V
Internal power dissipation		See Thermal Characteristics	
Input voltage range		V_S	V
Storage temperature range		–40 to +125	°C
Maximum junction temperature (T_J)		+150	°C
Maximum junction temperature (T_J), continuous operation, long-term reliability		+140	°C
ESD rating	Human body model (HBM)	2000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

DISSIPATION RATINGS(1)

PACKAGE	θ_{JP}(°C/W)	θ_{JA}(°C/W)	POWER RATING(2) (T_J= +125°C)	
			T_A= +25°C	T_A= +85°C
QFN-28	4.1	35	2.9 W	0.87 W

(1) These data were taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, θ_{JA} is 350°C/W.
(2) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final printed circuit board should strive to keep the junction temperature at or below +125° C for best performance and reliability.

ELECTRICAL CHARACTERISTICS: V_{S+}= +5 V

Boldface limits are tested at +25°C.

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L= 200 Ω differential, G = 20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

PARAMETER	CONDITIONS			PGA870IRHD MIN	PGA870IRHD TYP	PGA870IRHD MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE								
Small-signal bandwidth	G = 20 dB, V_O = 100 mV_{PP}				650		MHz	C
Large-signal bandwidth	G = 20 dB, V_O = 2 V_{PP}				650		MHz	C
Bandwidth for 0.1-dB flatness					100		MHz	C
Slew rate (differential)	2-V step				2900		V/µs	C
Rise time	2-V step				0.55		ns	C
Fall time	2-V step				0.55		ns	C
Settling time to 1%	2-V step				3		ns	C
Settling time to 0.1%	2-V step				5		ns	C
HARMONIC DISTORTION	**Gain = +20 dB, V_O = 2 V_{PP}, R_L = 200 Ω**							
Second-order harmonic distortion	f = 50 MHz				–108		dBc	C
	f = 100 MHz				–93		dBc	C
	f = 200 MHz				–71		dBc	C
Third-order harmonic distortion	f = 50 MHz				–95		dBc	C
	f = 100 MHz				–88		dBc	C
	f = 200 MHz				–75		dBc	C
Second-order intermodulation distortion	2-MHz tone spacing	f_1(MHz)	f_2(MHz)					C
		49	51		-87		dBc	C
		99	101		-90		dBc	C
		199	201		-89		dBc	C
Third-order intermodulation distortion	2-MHz tone spacing	49	51		-103		dBc	C
		99	101		–98		dBc	C
		199	201		–95		dBc	C
Output third-order intercept	V_{OUT} = 2 V_{PP}, R_L = 200 Ω	49	51		50		dBm	C
		99	101		47		dBm	C
		199	201		45		dBm	C
Noise figure	150-Ω system, Gain = +20 dB, f = 100 MHz				13		dB	C
DC								
Output offset voltage	T_A= +25°C			**–30**	±5	**30**	mV	A
	T_A= –40°C to +85°C			–35		35	mV	B
Average offset voltage drift	T_A= –40°C to +85°C				20		µV/°C	B
INPUT								
Input return loss	Z_{SYS}= 150 Ω, frequency < 300MHz				-40		dB	B
Differential input resistance				129	150	173	Ω	B
Differential input capacitance					1.2		pF	C
Single-ended input resistance					141		Ω	B
Common-mode rejection ratio	T_A= +25°C, Gain = 20 dB			**54**	76		dB	A

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value; only for information.

ELECTRICAL CHARACTERISTICS: V_{S+}= +5 V (continued)

Boldface limits are tested at +25°C.

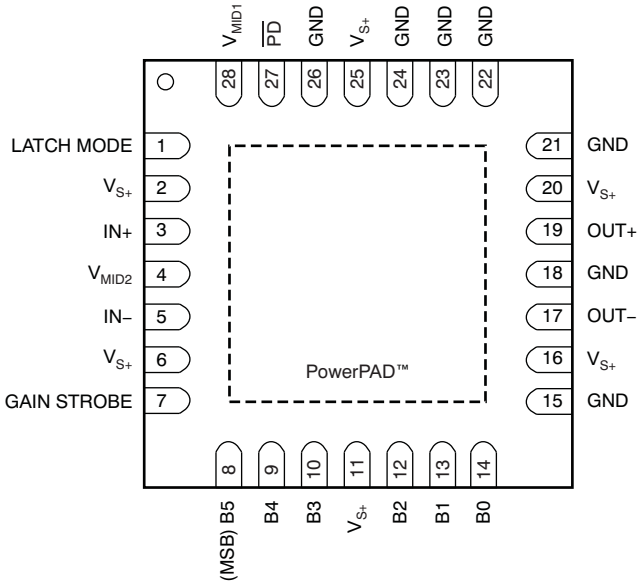
At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L= 200 Ω differential, G = 20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

PARAMETER	CONDITIONS		PGA870IRHD MIN	PGA870IRHD TYP	PGA870IRHD MAX	UNITS	TEST LEVEL(1)
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to midsupply	T_A= +25°C	**3.5**	3.7		V	A
		T_A= –40°C to +85°C	3.4			V	B
Minimum output voltage low		T_A= +25°C		1.3	**1.5**	V	A
		T_A= –40°C to +85°C			1.6	V	B
Differential output voltage swing	T_A= +25°C, R_L = 200 Ω		4	4.8		V_{PP}	B
	T_A= –40°C to +85°C		3.6			V_{PP}	B
Differential output current drive	T_A= +25°C, R_L = 20 Ω		**40**	50		mA_P	A
Output common-mode offset from midsupply	T_A= +25°C, R_L = 20 Ω		**–60**	±10	**60**	mV	A
Differential output impedance	f = 100 MHz			3.5 / 87		Ω / °	B
Differential output impedance model	Series $R_{OUT,EQ}$, $L_{OUT,EQ}$			0.3 / 3.8		Ω / nH	B
POWER SUPPLY							
Specified operating voltage			4.75	5	5.25	V	C
Quiescent current	T_A= +25°C		**138**	143	**148**	mA	A
	T_A= –40°C to +85°C		136		150	mA	B
Power-supply rejection ratio (PSRR)	T_A= +25°C, Gain = 20 dB(2)		**54**	76		dB	A
POWER DOWN							
Device power-up voltage threshold	Ensured on above 2.1 V		**2.1**			V	A
Device power-down voltage threshold	Ensured off below 0.9 V				**0.9**	V	A
Power-down quiescent current	T_A= +25°C			2	**4**	mA	A
	T_A= –40°C to +85°C				4.8	mA	B
Forward isolation in power-down state	f = 100 MHz			-110		dB	C
$\overline{PD}$ pin input bias current	P_D= $V_{S–}$			0.5		µA	B
$\overline{PD}$ pin input impedance				20 || 0.5		kΩ || pF	C
Turn-on time delay	Measured to output on			16		ns	C
Turn-off time delay	Measured to output off			60		ns	C
GAIN SETTING							
Gain range			**–11.5**		**+20**	dB	A
Gain control: G0 to G5				6		Bits	B
Gain step size	–11.5 dB ≤ Gain ≤ +20 dB			**0.50**		dB	A
Gain error over entire gain range	Absolute gain error		**–0.35**	±0.05	**0.35**	dB	A
	Step to step gain error		**–0.10**	±0.03	**0.10**	dB	A
Gain temp coefficient			0.0018	0.0022	0.0026	dB/°C	B
Gain settling time			5			ns	B
DIGITAL INPUTS	**B0 to B5 and Latch**						
Digital threshold low					**0.9**	V	A
Digital threshold high			**2.1**			V	A
Current into/out of digital pins				±20		nA	C
Data set up time to GAIN STROBE low				2.5		ns	C
Data hold time after GAIN STROBE low				0		ns	C
Latency time				6.4		ns	C

(2) PSRR is defined with respect to a differential output.

PIN CONFIGURATION

QFN-28
RHD PACKAGE
(TOP VIEW)



PIN ASSIGNMENTS

PIN NUMBER	PIN NAME	DESCRIPTION
1	LATCH MODE	Controls latched and unlatched acquisition of the gain control word (B0 to B5). See the application section *Gain Control Modes* for a detailed description.
2, 6, 11, 16, 20, 25	V_{S+}	+5V power supply
3	IN+	Noninverting input
4	V_{MID2}	Buffer output for the internal midsupply reference. This point is the output of an active buffer which is not intended to drive an external load. It should be bypassed by a 0.1-µF capacitor.
5	IN–	Inverting input
7	GAIN STROBE	Gain latch clock pin
8	B5 (MSB)	Gain control MSB
9	B4	Gain control bit 4
10	B3	Gain control bit 3
12	B2	Gain control bit 2
13	B1	Gain control bit 1
14	B0 (LSB)	Gain control bit 0
17	OUT–	Inverting output
15, 18, 21, 22, 23, 24, 26	GND	Ground
19	OUT+	Noninverting output
27	$\overline{PD}$	Active low power-down for device analog circuitry. Gain control CMOS circuitry is still active when $\overline{PD}$ is low.
28	V_{MID1}	Chip bypass pin for internal midsupply reference. This point is the midpoint of a resistive voltage divider and is not intended to function as an input. It should be bypassed with a 0.1-µF capacitor.
Thermal Pad	PowerPAD	Thermal contact for heat dissipation. The thermal pad must be connected to electrical ground.

TYPICAL CHARACTERISTICS

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

SMALL-SIGNAL AC RESPONSE
Gain Adjusted from –11.5 dB to +5 dB

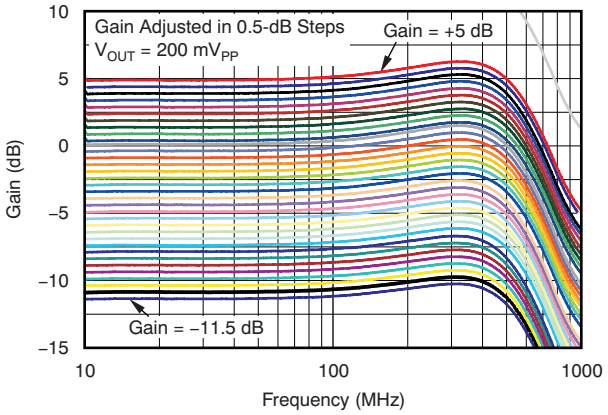


Figure 1.

SMALL-SIGNAL AC RESPONSE
Gain Adjusted from +5.5 dB to +20 dB

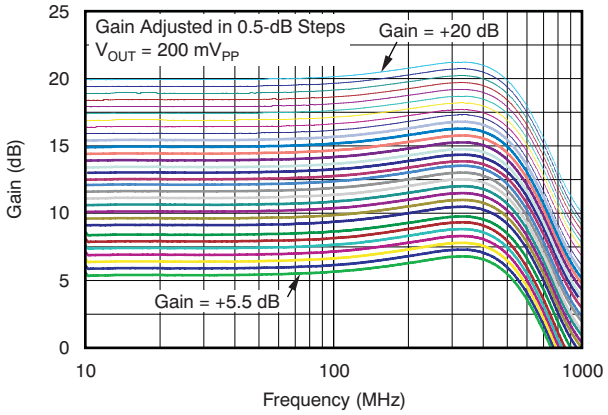


Figure 2.

LARGE-SIGNAL AC RESPONSE AT FOUR GAINS
DIFFERENTIAL INPUT

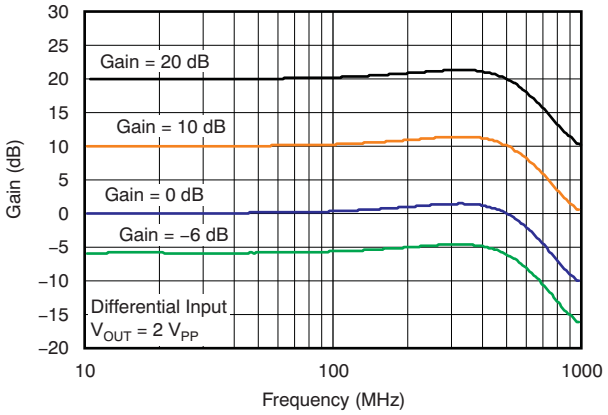


Figure 3.

LARGE-SIGNAL AC RESPONSE AT FOUR GAINS
SINGLE-ENDED INPUT

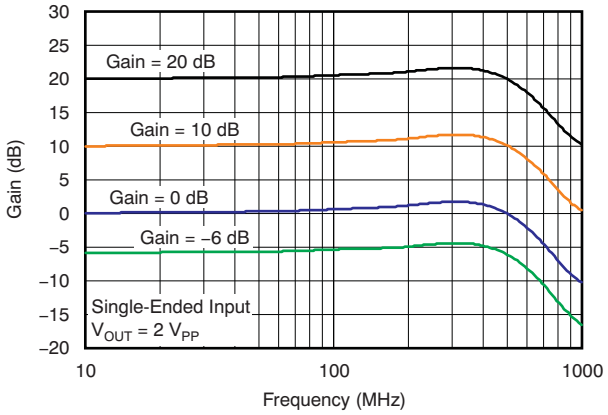


Figure 4.

DIFFERENTIAL FREQUENCY RESPONSE vs CAPACITIVE LOAD

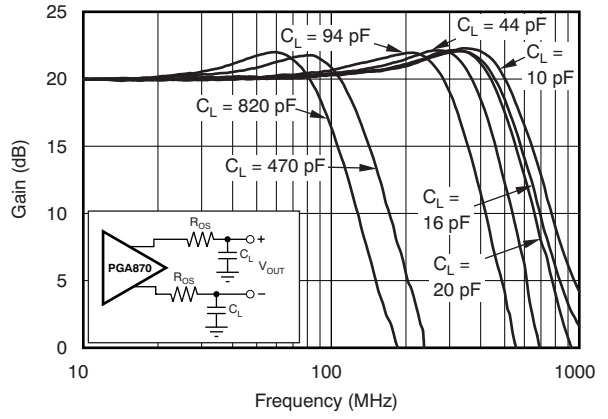


Figure 5.

R_{OS} vs CAPACITIVE LOAD

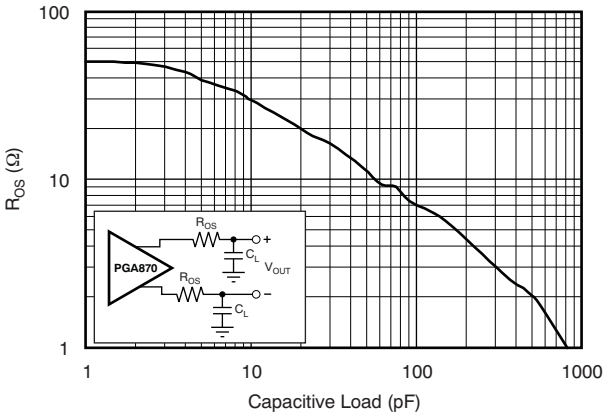


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

LARGE-SIGNAL GAIN vs GAIN SETTING

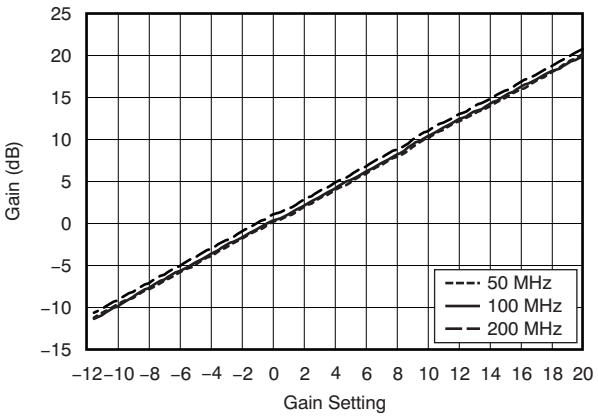


Figure 7.

STEP-TO-STEP GAIN ERROR vs GAIN SETTING OVER TEMPERATURE

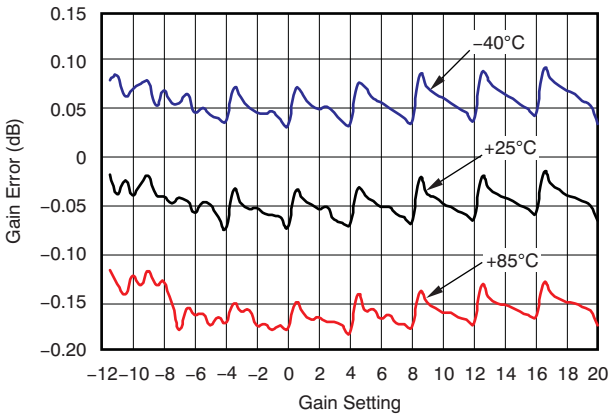


Figure 8.

STEP-TO-STEP GAIN ERROR vs GAIN SETTING OVER FREQUENCY

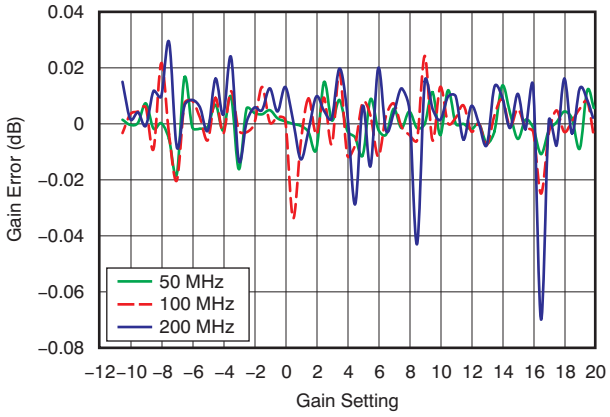


Figure 9.

GAIN STEP RESPONSE: NO LATCH

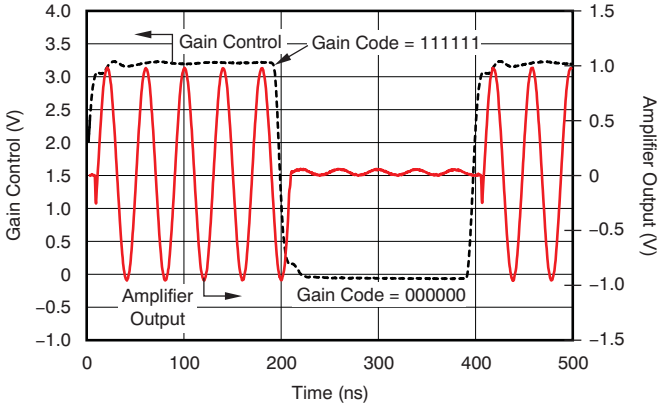


Figure 10.

GAIN STEP RESPONSE: LEVEL-TRIGGERED GAIN LATCH

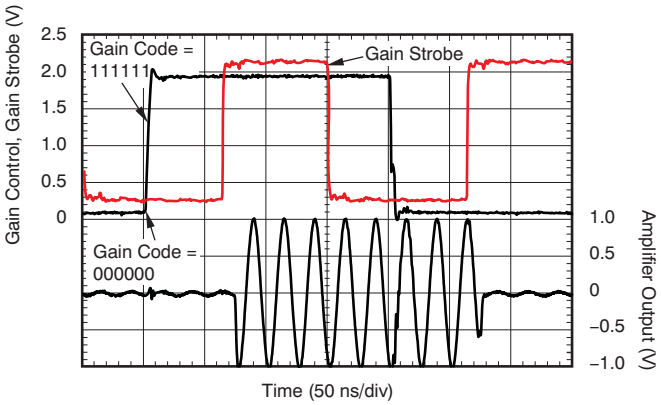


Figure 11.

GAIN STEP RESPONSE: EDGE-TRIGGERED LATCH

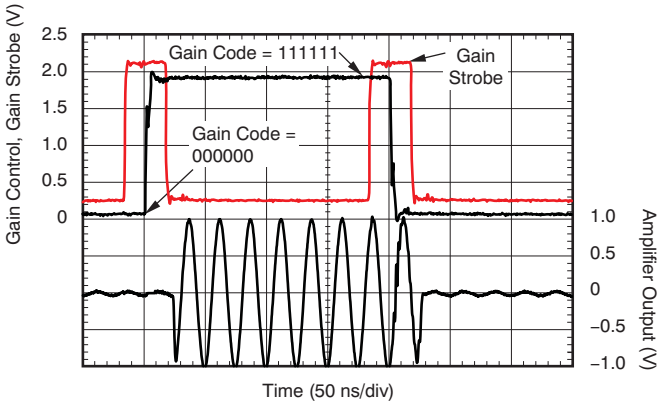


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

SECOND-ORDER INTERMODULATION DISTORTION FOR FOUR OUTPUT LOADS (V_{OUT} = 2 V_{PP})

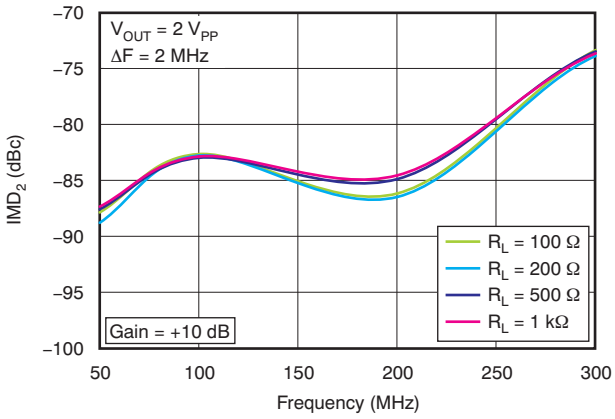


Figure 13.

THIRD-ORDER INTERMODULATION DISTORTION FOR TWO GAINS AND FOUR OUTPUT LOADS (V_{OUT} = 2 V_{PP})

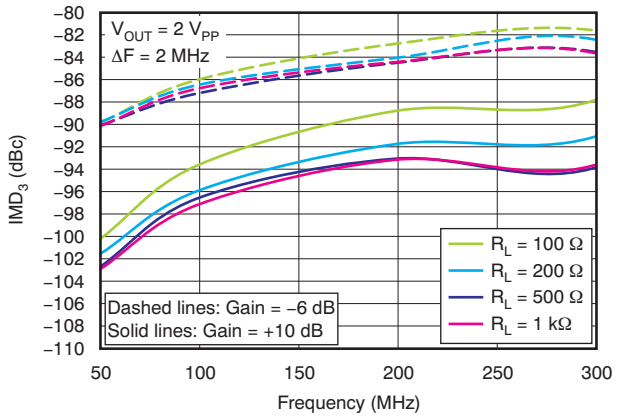


Figure 14.

SECOND-ORDER INTERMODULATION DISTORTION FOR FOUR OUTPUT LOADS (V_{OUT} = 2 V_{PP})

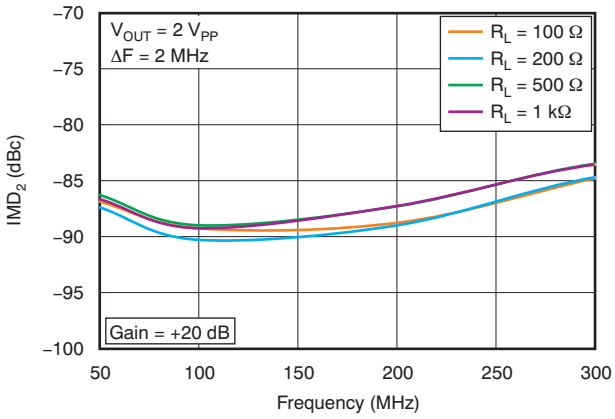


Figure 15.

THIRD-ORDER INTERMODULATION DISTORTION FOR TWO GAINS AND FOUR OUTPUT LOADS (V_{OUT} = 2 V_{PP})

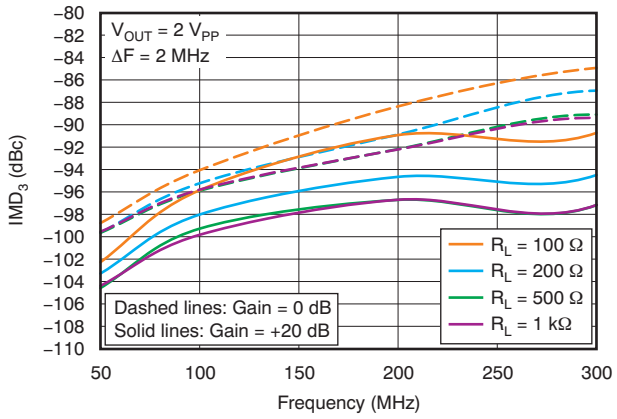


Figure 16.

OUTPUT THIRD-ORDER INTERCEPT vs FREQUENCY (V_{OUT} = 2 V_{PP})

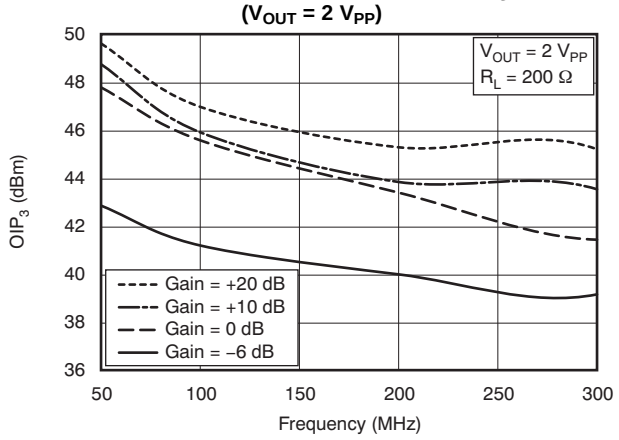


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

SECOND-ORDER INTERMODULATION DISTORTION FOR FOUR OUTPUT LOADS (V_{OUT} = 3 V_{PP})

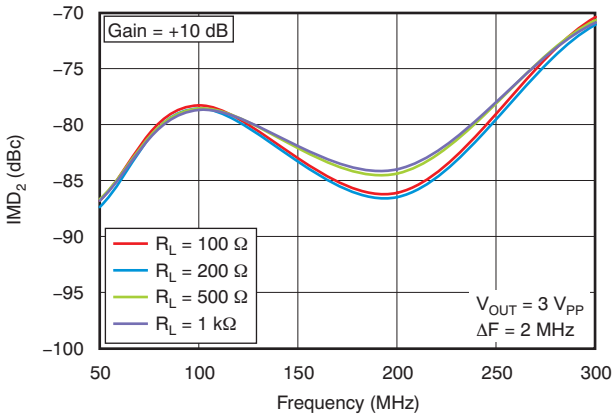


Figure 18.

THIRD-ORDER INTERMODULATION DISTORTION FOR TWO GAINS AND FOUR OUTPUT LOADS (V_{OUT} = 3 V_{PP})

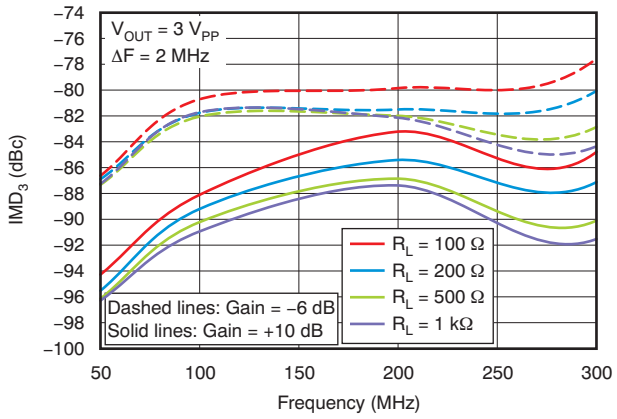


Figure 19.

SECOND-ORDER INTERMODULATION DISTORTION FOR FOUR OUTPUT LOADS (V_{OUT} = 3 V_{PP})

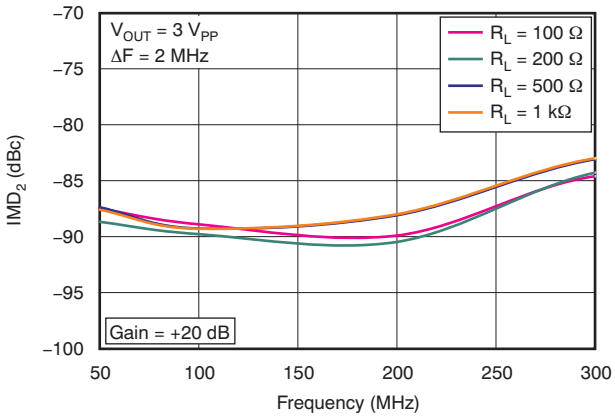


Figure 20.

THIRD-ORDER INTERMODULATION DISTORTION FOR TWO GAINS AND FOUR OUTPUT LOADS (V_{OUT} = 3 V_{PP})

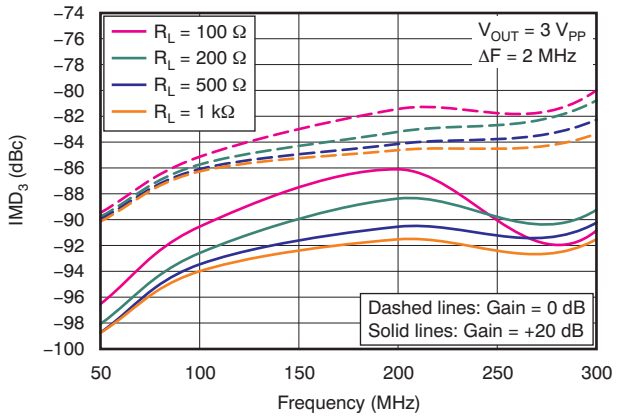


Figure 21.

OUTPUT THIRD-ORDER INTERCEPT vs FREQUENCY (V_{OUT} = 3 V_{PP})

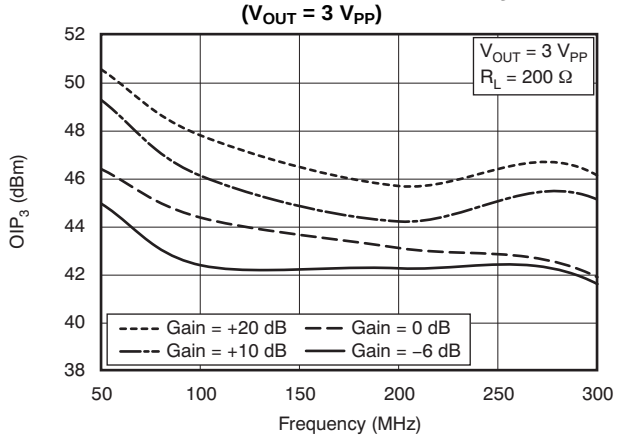


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 2 V_{PP})

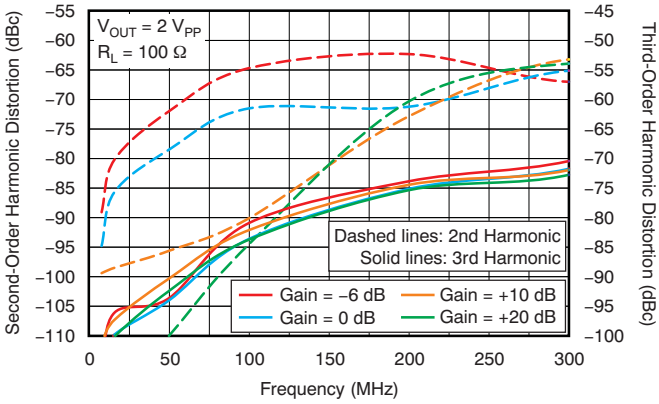


Figure 23.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 2 V_{PP})

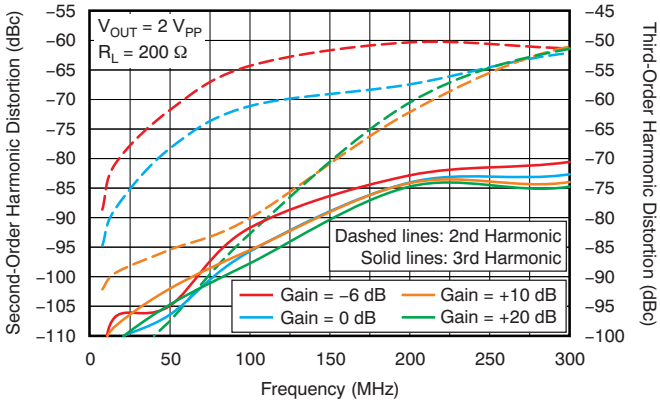


Figure 24.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 2 V_{PP})

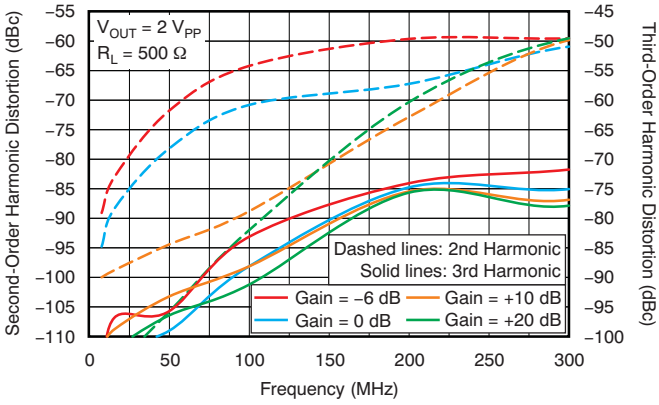


Figure 25.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 2 V_{PP})

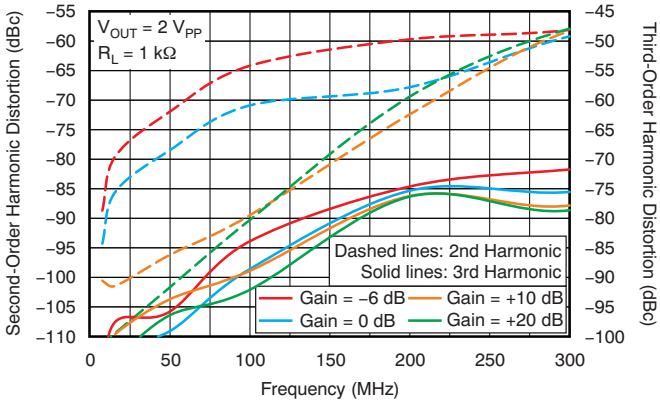


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 3 V_{PP})

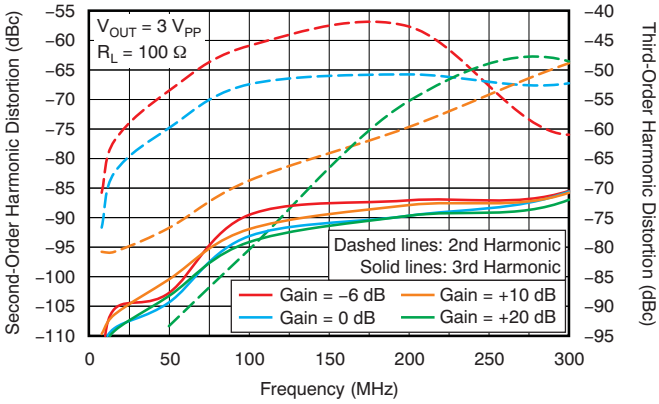


Figure 27.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 3 V_{PP})

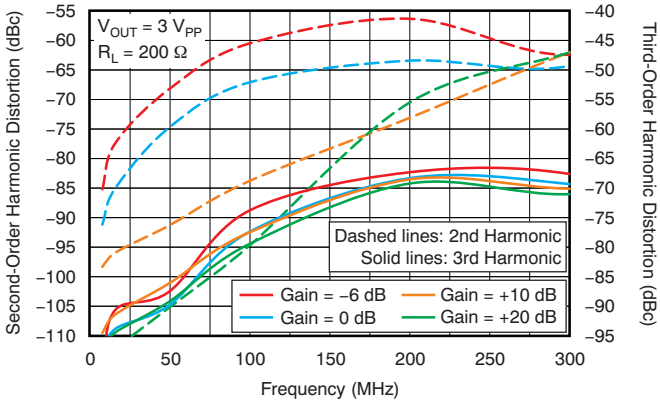


Figure 28.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 3 V_{PP})

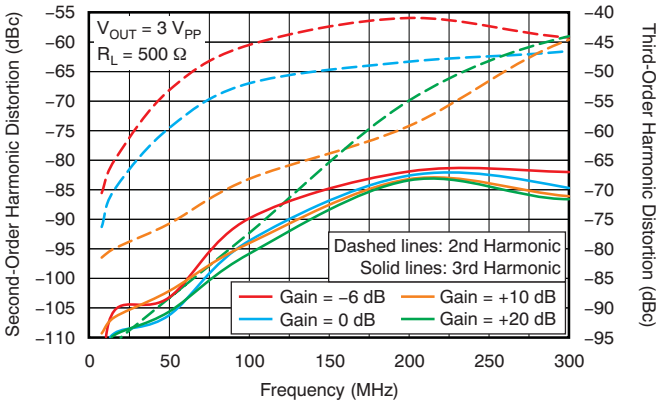


Figure 29.

HARMONIC DISTORTION vs FREQUENCY (V_{OUT} = 3 V_{PP})

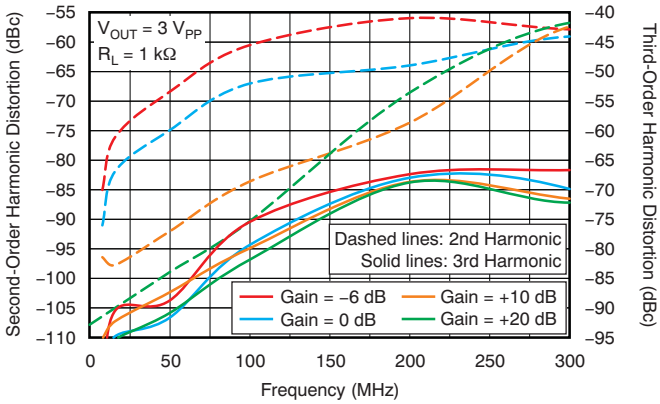


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

NOISE FIGURE vs GAIN

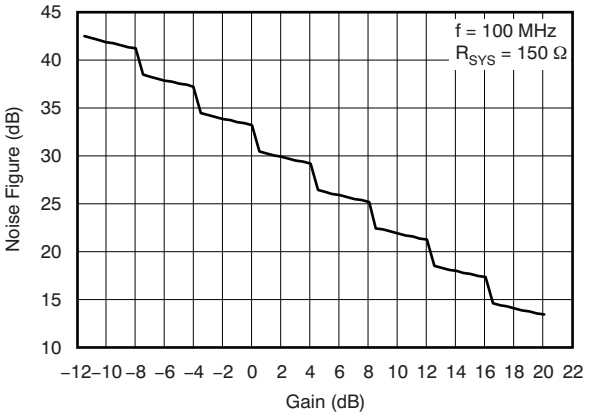


Figure 31.

DISABLE STEP RESPONSE

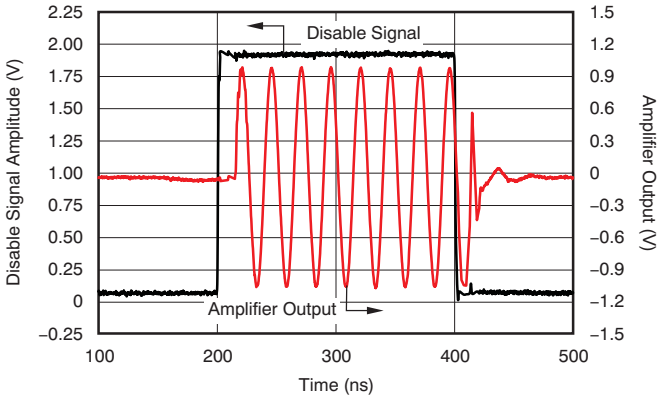


Figure 32.

LARGE- AND SMALL-SIGNAL DIFFERENTIAL PULSE RESPONSE

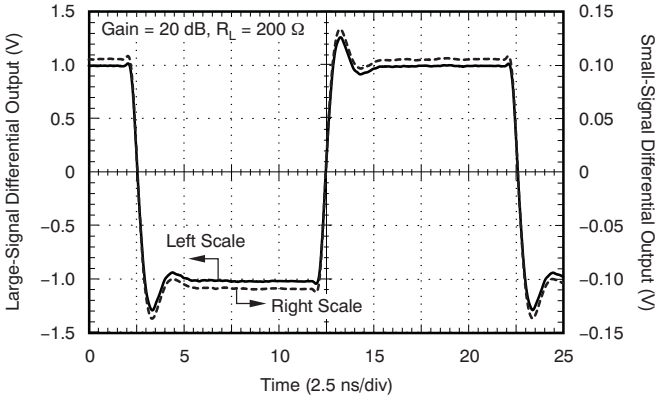


Figure 33.

FORWARD ISOLATION vs FREQUENCY IN DISABLED MODE

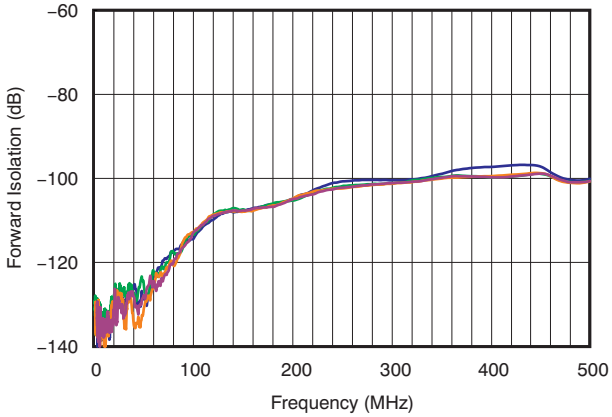


Figure 34.

DIFFERENTIAL INPUT IMPEDANCE

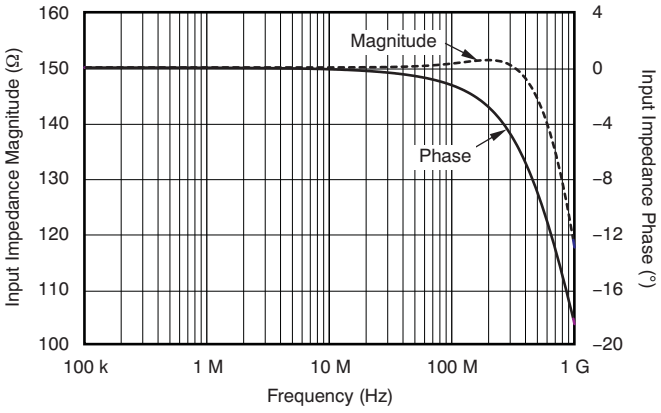


Figure 35.

DIFFERENTIAL INPUT RETURN LOSS vs FREQUENCY

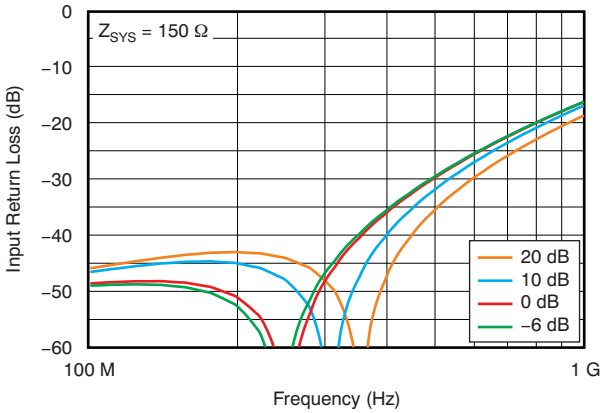


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A= +25°C, V_{S+}= +5 V, differential input signal, differential V_{OUT} = 2 V_{PP}, R_L = 200 Ω differential, G = +20 dB, and input and output common-mode at internal midsupply reference, unless otherwise noted.

SINGLE-ENDED INPUT RETURN LOSS vs FREQUENCY

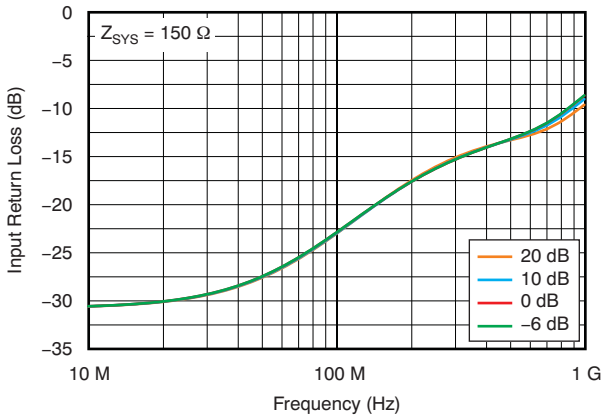


Figure 37.

DIFFERENTIAL OUTPUT IMPEDANCE

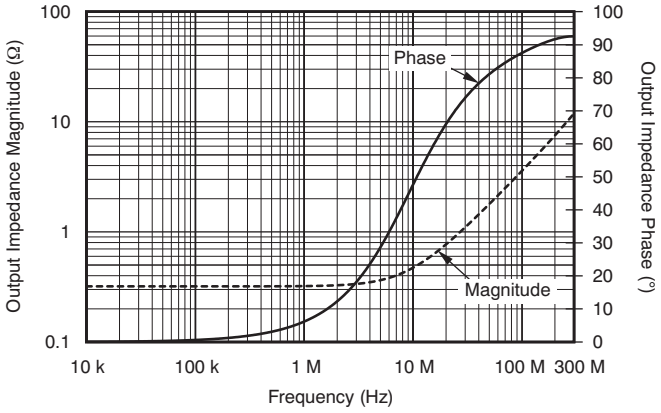


Figure 38.

DIFFERENTIAL OUTPUT SWING vs R_{LOAD}

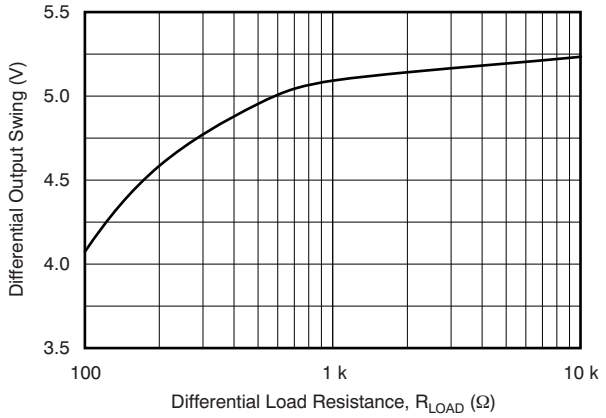


Figure 39.

PSRR AND CMRR vs FREQUENCY

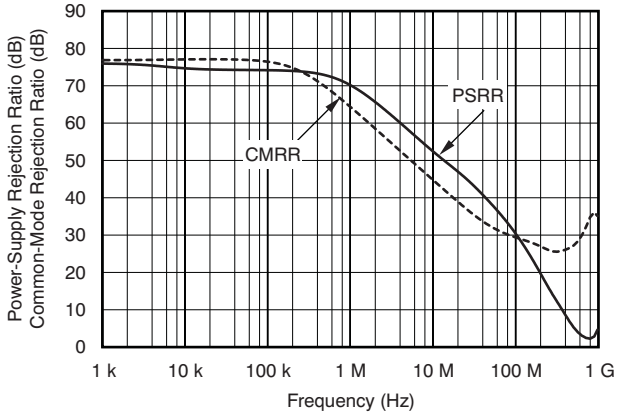


Figure 40.

APPLICATION INFORMATION

Device Operation

The PGA870 is a wideband, fully differential, programmable-gain amplifier. Looking at the block diagram in Figure 41, the PGA870 can be separated into the following functional blocks:

- Input Attenuator
- Buffered MUX
- Output Amplifier
- 8-bit digital interface
- Power function

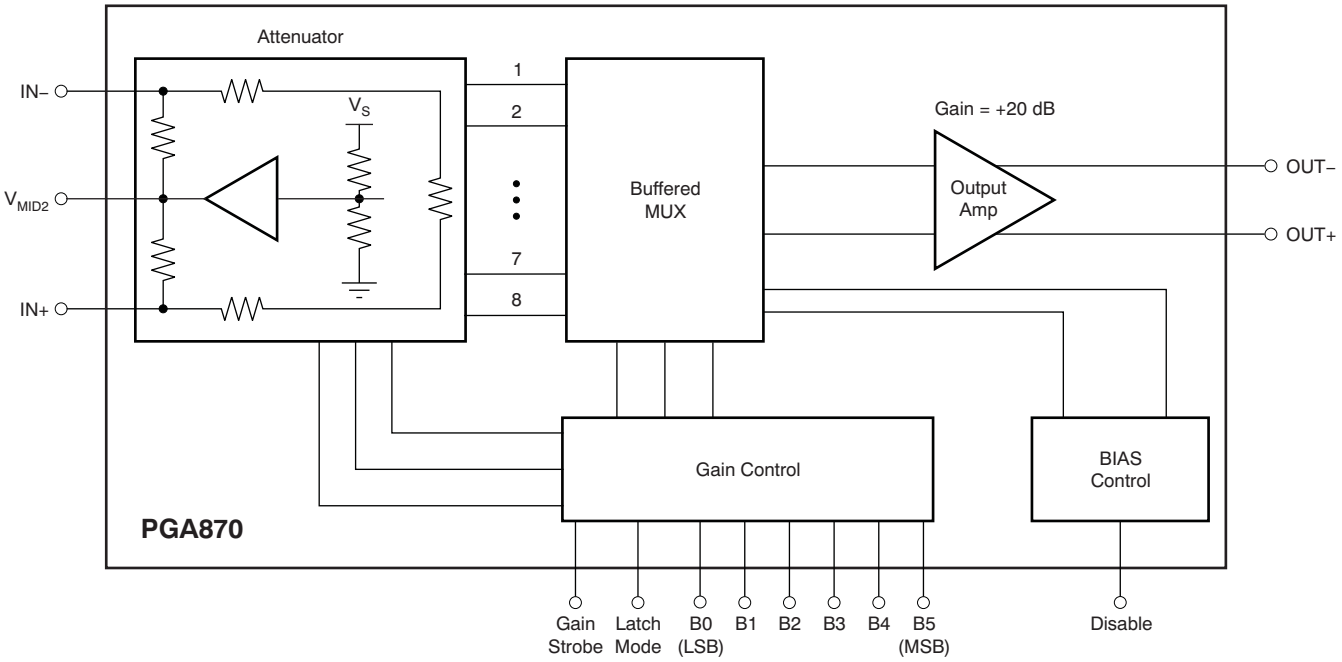


Figure 41. PGA870 Block Diagram

Input Attenuator

The input stage of the PGA870 consists of a logarithmic R2R ladder and presents a 150-Ω load to the previous stage. To minimize input return loss and noise figure, it is recommended to provide a 150-Ω matching for that input. This input can be driven either differentially or single-ended.

This resistive input network is internally biased to midsupply by an internal buffer (V_{MID2} on pin 4). Proper bypassing is required on this node (0.1 µF). The buffer midsupply is generated by a passive resistor network (V_{MID1} on pin 28). A 0.1-µF capacitor is expected on V_{MID1} for adequate bypassing. Although V_{MID1} and V_{MID2} are externally accessible, neither of these pins is intended to be externally driven. Additionally, V_{MID2} is not intended to drive the midsupply reference to another chip, but can source approximately 200 µA if required.

During power-down operation, the input maintains its nominal differential resistance. However, V_{MD1} and V_{MID2} fall to 0 V.

The input attenuator is controlled via the three most significant bits (MSBs) of the gain control. Refer to Table 1 for the step size of each of these three MSBs.

Input Amplifier and Buffered MUX

Following the input attenuator is a programmable buffer stage; the gain of the programmable buffer is controlled by the three least significant bits (LSBs) of the gain-control word. Refer to Table 1 for the step size of each of these three LSBs.

Table 1. Gain Bits and Corresponding Gain Step Sizes (in dB)

(MSB) B5	B4	B3	B2	B1	(LSB) B0
16	8	4	2	1	0.5

Output Amplifier

The PGA870 has a differential, voltage-mode output stage with a differential output resistance of approximately 0.3 Ω and an inductive reactance equivalent to 3.8 nH. The common-mode output voltage has a nominal value of V_{MID2}. This output amplifier has a nominal gain of +20 dB.

The nominal load is 200 Ω, but the PGA870 can drive loads as low as 100 Ω with only minor changes to the device distortion.

The output pins go to a high-impedance state when the device is the power-down state (that is, when $\overline{PD}$ is low).

8-bit Digital Interface

The 8-bit digital interface is composed of six bits: three MSBs that control the input attenuation and three LSBs that control the input amplifier and buffered MUX. For more information on this parallel interface, refer to the *Gain Control and Latch Modes* section.

Power function

The PGA870 features a low-power disabled state for the analog circuitry when the power-down ($\overline{PD}$) pin is low. In the disabled state, the digital circuitry remains active, which allows the gain to be set before device power-up. There is no internal circuitry to provide a nominal bias to this pin. If this pin is to be left open, it must be biased with an external pull-up resistor.

Note that when the PGA870 is in this low-power mode, the gain can be programmed using the 8-bit digital interface, the output pins go to a high-impedance state, and the voltage on the midsupply pins biasing the attenuator (pin 4 and pin 28) goes to 0 V.

Gain Control and Latch Modes

The PGA870 has six bits of gain control (B5 to B0) that give an extended gain range from a maximum gain of 20 dB to a minimum gain of –11.5 dB. The LSB (B0) represents a minimum gain change (step size) of 0.5 dB, and the LSB (B5) represents a gain change of 16 dB. The equivalent gain step size of each gain control bit is shown in Table 1. The device voltage gain can be expressed by the following equation:

$$Gain_{dB} = 20\ dB - 0.5\ dB \times (N_G - 63)$$

N_G is the equivalent base-10 integer number that corresponds to the binary gain control word. A summary of the 63 possible device gains versus NG and the values of B0 to B5 are shown in Table 2.

The high and low voltage thresholds allow all of the gain control pins to be controlled by CMOS circuitry. There are no internal pull-up resistors on the gain-control pins. If the pins are to be left open, they must be biased with external pull-up resistors.

The PGA870 can be configured so the device gain is controlled by only the six gain bits (*no latch*) when the GAIN STROBE pin and the GAIN MODE pin are both held high. In this operating mode, the device voltage gain follows the signals on pins B0 to B5. Transients on the six gain bits can cause changes to the PGA870 gain while in this mode, as well. To combat this possibility, the PGA870 also supports two gain modes where the gain bit data are acquired and latched by signals on the GAIN STROBE pin.

The device is configured for a *level-triggered latch* when the LATCH MODE pin is high; this configuration allows the six gain bits to be acquired and latched only on a high signal on the GAIN STROBE. When the GAIN STROBE signal goes low, the gain-control data are latched and the PGA870 gain is independent of the six gain bits until the GAIN STROBE goes high again.

If the PGA870 LATCH MODE pin is low, the device is configured for an *edge-triggered latch* that acquires and latches the six gain-control bits only on the falling edge of the GAIN STROBE signal.

Table 2. PGA870 Gain and Corresponding Gain Word Values

Gain State NG	Gain (dB)	(MSB) B5	B4	B3	B2	B1	(LSB) B0	Gain State NG	Gain (dB)	(MSB) B5	B4	B3	B2	B1	(LSB) B0
63	20	1	1	1	1	1	1	31	4	0	1	1	1	1	1
62	19.5	1	1	1	1	1	0	30	3.5	0	1	1	1	1	0
61	19	1	1	1	1	0	1	29	3	0	1	1	1	0	1
60	18.5	1	1	1	1	0	0	28	2.5	0	1	1	1	0	0
59	18	1	1	1	0	1	1	27	2	0	1	1	0	1	1
58	17.5	1	1	1	0	1	0	26	1.5	0	1	1	0	1	0
57	17	1	1	1	0	0	1	25	1	0	1	1	0	0	1
56	16.5	1	1	1	0	0	0	24	0.5	0	1	1	0	0	0
55	16	1	1	0	1	1	1	23	0	0	1	0	1	1	1
54	15.5	1	1	0	1	1	0	22	-0.5	0	1	0	1	1	0
53	15	1	1	0	1	0	1	21	-1	0	1	0	1	0	1
52	14.5	1	1	0	1	0	0	20	-1.5	0	1	0	1	0	0
51	14	1	1	0	0	1	1	19	-2	0	1	0	0	1	1
50	13.5	1	1	0	0	1	0	18	-2.5	0	1	0	0	1	0
49	13	1	1	0	0	0	1	17	-3	0	1	0	0	0	1
48	12.5	1	1	0	0	0	0	16	-3.5	0	1	0	0	0	0
47	12	1	0	1	1	1	1	15	-4	0	0	1	1	1	1
46	11.5	1	0	1	1	1	0	14	-4.5	0	0	1	1	1	0
45	11	1	0	1	1	0	1	13	-5	0	0	1	1	0	1
44	10.5	1	0	1	1	0	0	12	-5.5	0	0	1	1	0	0
43	10	1	0	1	0	1	1	11	-6	0	0	1	0	1	1
42	9.5	1	0	1	0	1	0	10	-6.5	0	0	1	0	1	0
41	9	1	0	1	0	0	1	9	-7	0	0	1	0	0	1
40	8.5	1	0	1	0	0	0	8	-7.5	0	0	1	0	0	0
39	8	1	0	0	1	1	1	7	-8	0	0	0	1	1	1
38	7.5	1	0	0	1	1	0	6	-8.5	0	0	0	1	1	0
37	7	1	0	0	1	0	1	5	-9	0	0	0	1	0	1
36	6.5	1	0	0	1	0	0	4	-9.5	0	0	0	1	0	0
35	6	1	0	0	0	1	1	3	-10	0	0	0	0	1	1
34	5.5	1	0	0	0	1	0	2	-10.5	0	0	0	0	1	0
33	5	1	0	0	0	0	1	1	-11	0	0	0	0	0	1
32	4.5	1	0	0	0	0	0	0	-11.5	0	0	0	0	0	0

Table 3. Gain Control Signals and Latch Modes

Latch Mode	GAIN STROBE	LATCH MODE	CONDITION
Edge-triggered latch	Falling edge	Low	Device gain follows and latches gain control word (B0 to B5) only on GAIN STROBE falling edge.
Level-triggered latch	Low	High	Device gain follows gain control word (B0 to B5) when GAIN STROBE and LATCH MODE are both high. Device gain latches when GAIN STROBE goes low.
No latch	High	High	Device gain is level-triggered on the gain-control word (B0 to B5) when LATCH MODE is high and GAIN STROBE remains high.

Table 3 and Figure 42 show a summary table and timing diagrams of the gain modes, respectively. Figure 43 illustrates a timing diagram that defines the transitions and timing of the set-up and hold times for both level-triggered and edge-triggered latch modes.

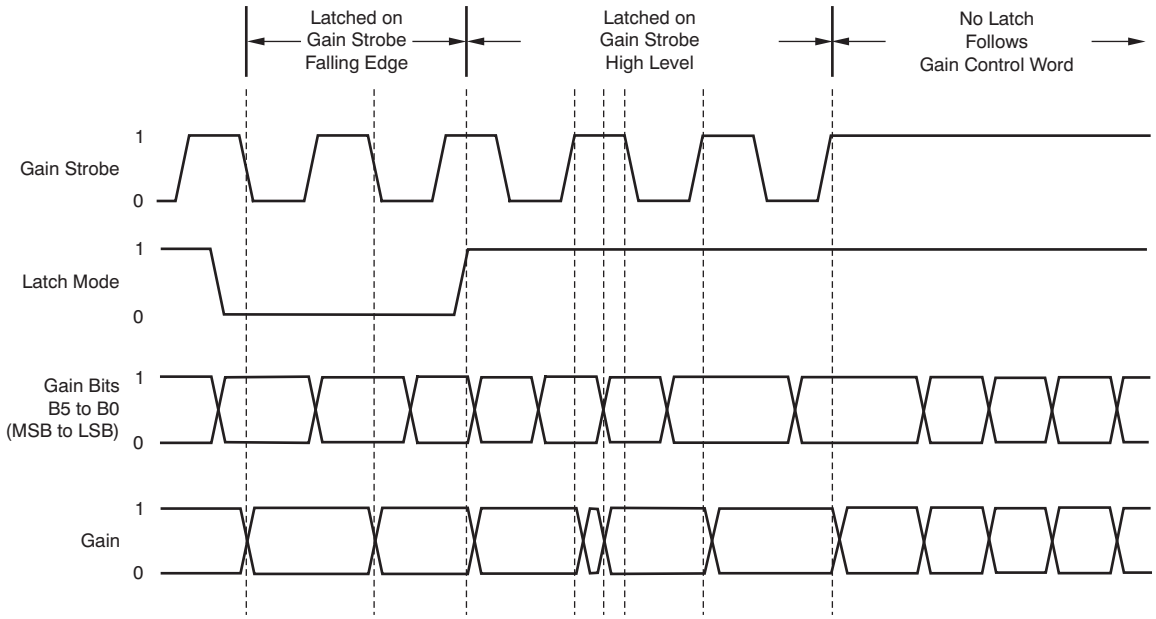


Figure 42. Gain Mode Timing

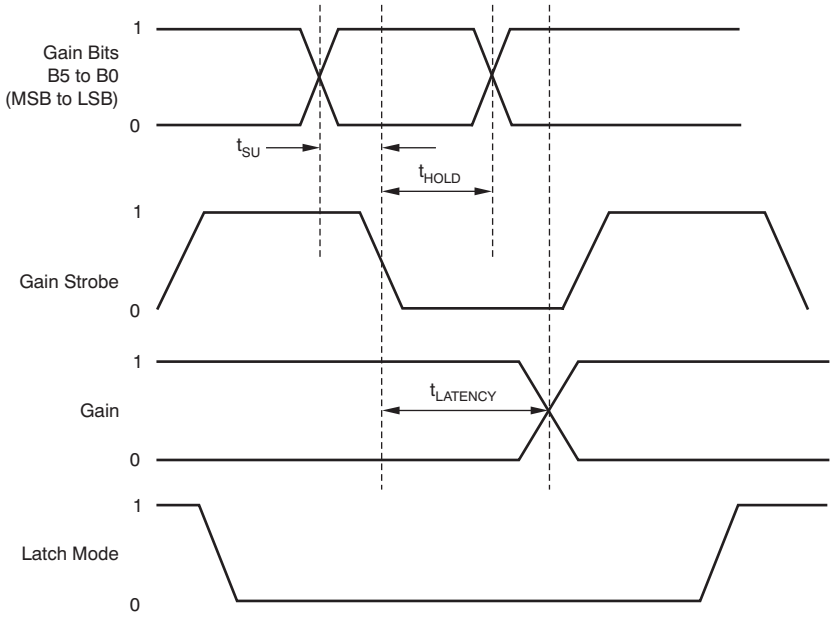
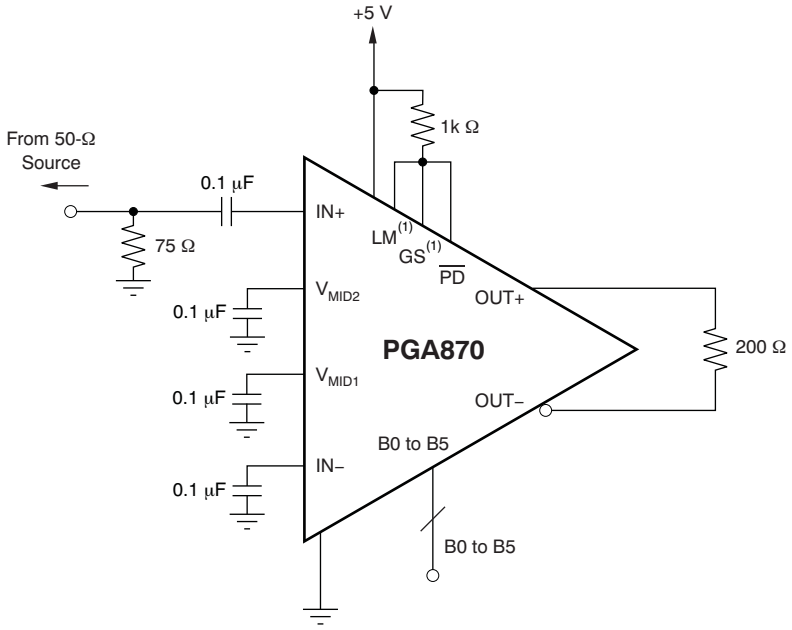


Figure 43. Set-Up and Hold Times: Level-Triggered and Edge-Triggered Latch Modes

Single-Ended to Differential Operation

Figure 44 represents a single-ended to differential conversion test configuration with a 50-Ω source and a 200-Ω load. The midsupply pins V_{MID1} and V_{MID2} are properly bypassed; because this circuit is ac-coupled, these pins provide the biasing voltage required by the PGA870 input stage. The LATCH MODE, GAIN STROBE, and $\overline{PD}$ pins are connected to the supply voltage through a pull-up resistor. The $\overline{PD}$ pin set high powers up the PGA870, while setting the LATCH MODE and GAIN STROBE pins high bypasses the latch mode, allowing instantaneous gain changes as B5 to B0 change. On the noninverting input, a 75-Ω resistance was added to adapt the 150 Ω to 50 Ω and match the 50-Ω source.

If a differential signal source is to be dc-coupled to the device, it should have a common-mode voltage that is within 0.2 V of the midsupply reference. If the input common-mode/dc voltage is greater than 0.2 V from midsupply, then increased distortion and reduced performance can result. The non-driven input pin of the PGA870 should be ac-coupled to ground through a capacitor. If a single-ended signal source is dc-coupled to an input pin, and the non-driven input pin is grounded, the PGA870 amplifies the desired signal as well as the difference between the offset from the PGA870 midsupply reference, V_{MID1}.

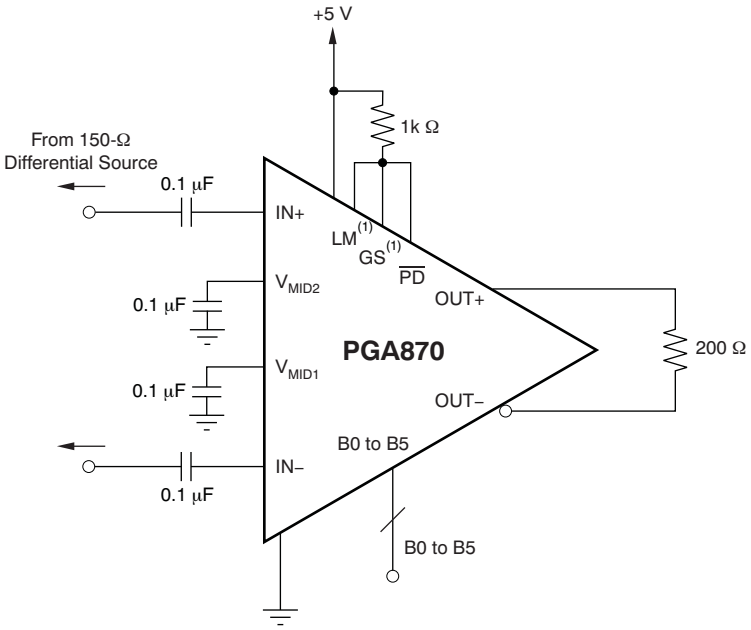


(1) LM = LATCH MODE pin (pin 1), GS = GAIN STROBE pin (pin 7).

Figure 44. Basic Connections for Single-Ended to Differential Conversion

Differential-to-Differential Operation

Differential operation of PGA870 is shown in Figure 45. In this example, both input pins are connected to a differential 150-Ω source. The PGA870 is driving a typical 200-Ω load. Both midsupply voltage pins V_{MID1} and V_{MID2} are bypassed with a 0.1-µF capacitor. The LATCH MODE, GAIN STROBE, and $\overline{PD}$ pins are connected to the power supply using a 1-kΩ pull-up resistor. The $\overline{PD}$ pin set high powers up the PGA870, while setting the Latch Mode and the Gain Strobe pins high bypasses the latch mode, allowing instantaneous gain changes as B5 to B0 change.



(1) LM = LATCH MODE pin (pin 1), GS = GAIN STROBE pin (pin 7).

Figure 45. Basic Connections for Fully Differential Operation

PCB Layout Recommendations

Complete information about the PGA870EVM is found in the PGA870EVM User Guide, available for download through the PGA870 product folder on the TI web site. Printed circuit board (PCB) layout should follow these general guidelines:

1. Signal routing should be direct and as short as possible into and out of the device input and output pins. Routing the signal path between layers using vias should be avoided if possible.
2. The device PowerPAD should be connected to a solid ground plane with multiple vias. The PowerPAD must be connected to electrical ground. Consult the PGA870EVM User Guide for a layout example.
3. Ground or power planes should be removed from directly under the amplifier output pins.
4. A 0.1-µF capacitor should be placed between the V_{MID}pin and ground near to the pin.
5. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
6. Two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
7. Two 10-µF power-supply decoupling capacitors should be placed within 1 in (2,54 cm) of the device.
8. The digital control pins use CMOS logic levels for high and low signals, but can tolerate being pulled high to a +5-V power supply. The digital control pins do not have internal pull-up resistors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PGA870IRHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA870IRHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

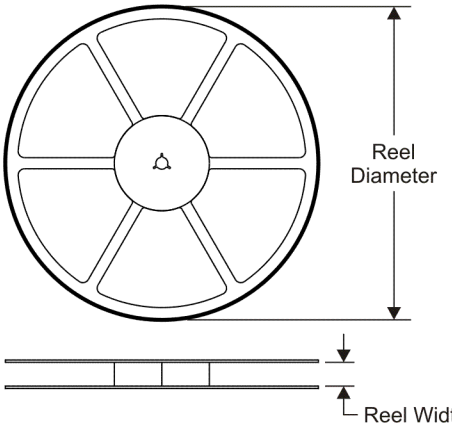
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

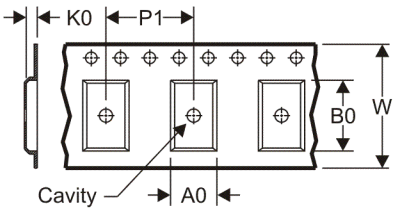
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

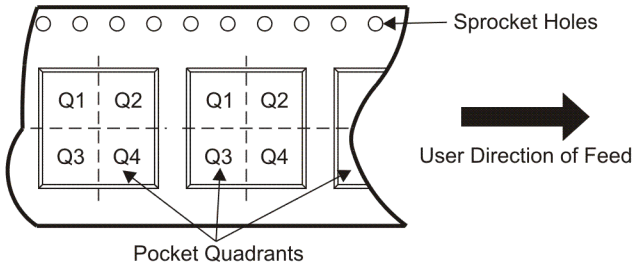


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

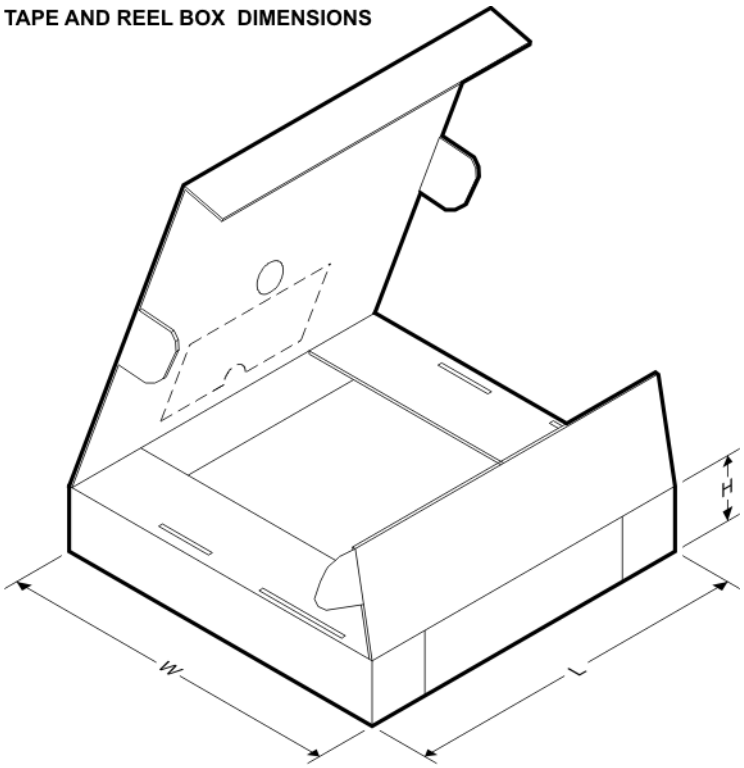
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA870IRHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
PGA870IRHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

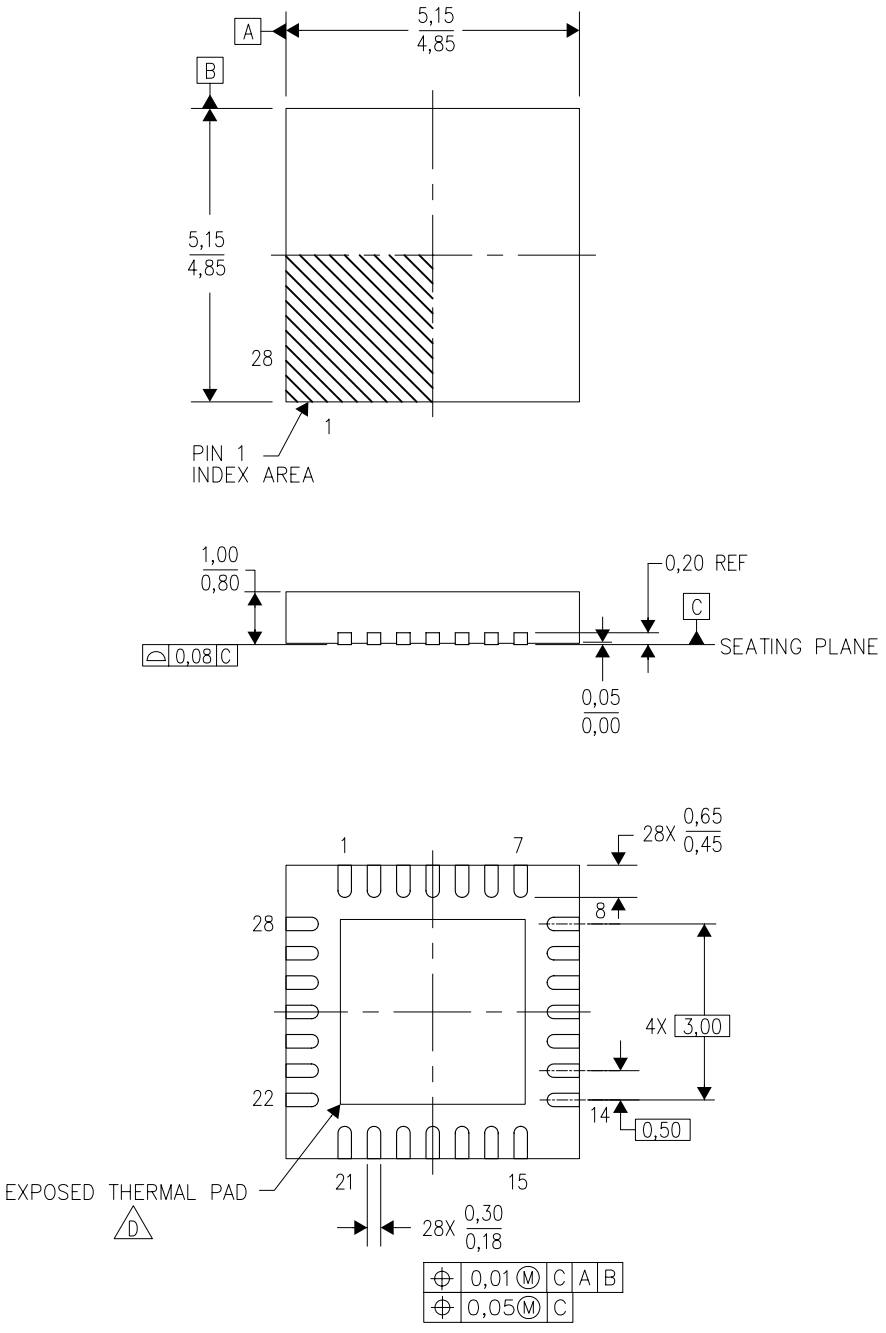
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA870IRHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
PGA870IRHDT	VQFN	RHD	28	250	190.5	212.7	31.8

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/D 06/10

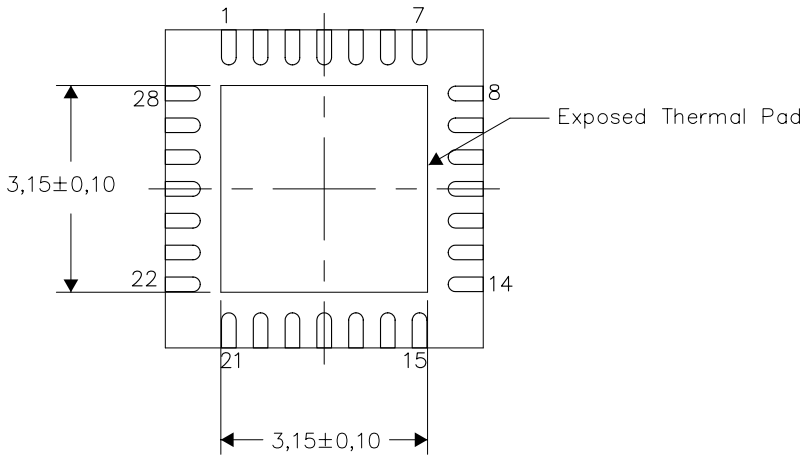
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

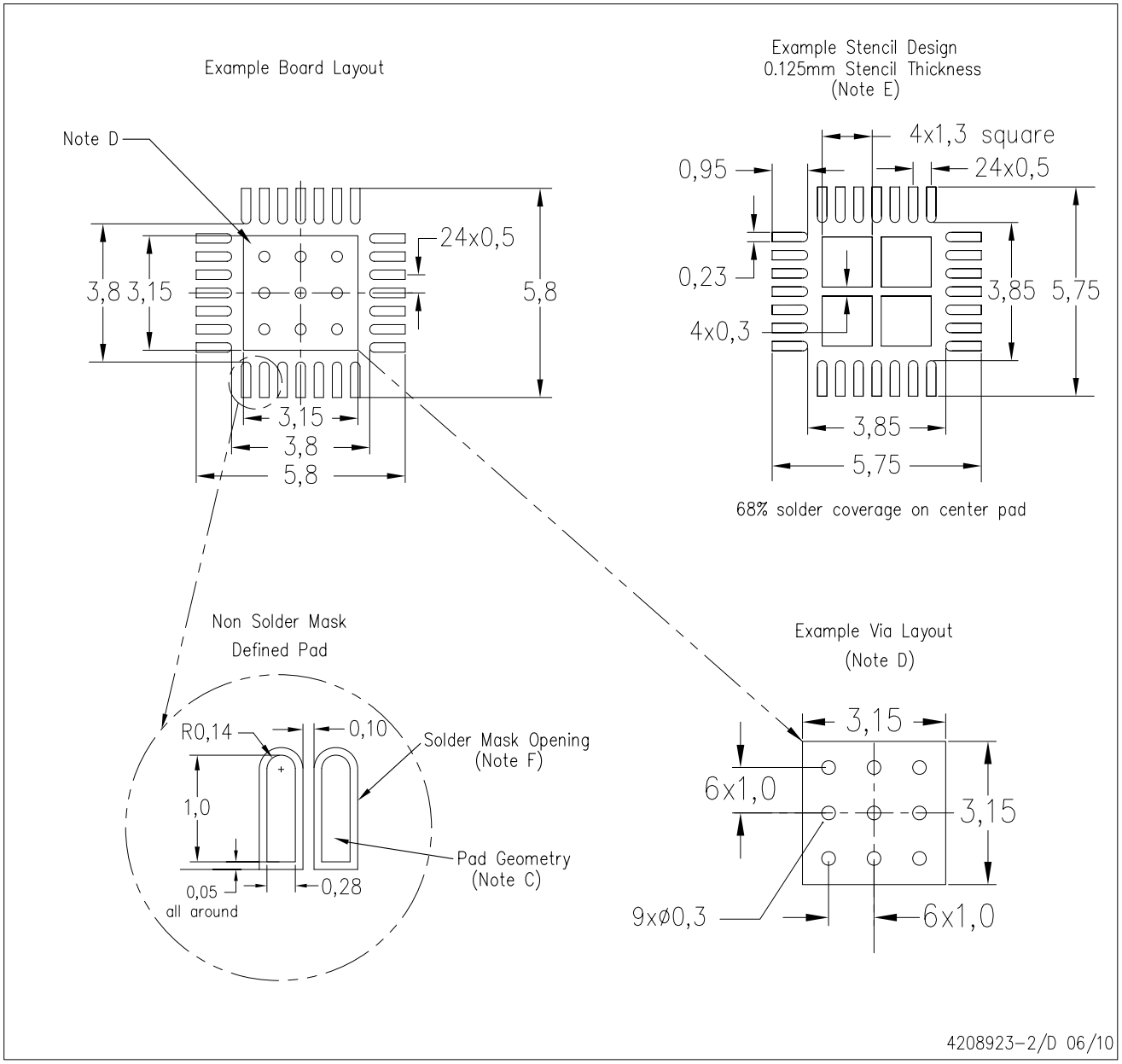


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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