NEC



# MOS FIELD EFFECT TRANSISTOR
# 2SK3635

## SWITCHING
## N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK3635 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

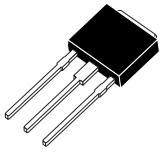
### ★ ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SK3635 | TO-251 (MP-3) |
| 2SK3635-Z | TO-252 (MP-3Z) |

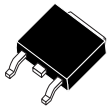
### FEATURES

- High voltage: $V_{DSS}$ = 200 V
- Gate voltage rating: ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.43 Ω MAX. ($V_{GS}$ = 10 V, $I_D$ = 4.0 A)
- Low $C_{iss}$: $C_{iss}$ = 390 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package
- Avalanche capability rated

(TO-251)



(TO-252)



### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 200 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±30 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ±8.0 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±24 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T1}$ | 24 | W |
| Total Power Dissipation ($T_A$ = 25°C) | $P_{T2}$ | 1.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current Note2 | $I_{AS}$ | 8 | A |
| Single Avalanche Energy Note2 | $E_{AS}$ | 6.4 | mJ |
| Repetitive Avalanche Current Note3 | $I_{AR}$ | 8 | A |
| Repetitive Avalanche Energy Note3 | $E_{AR}$ | 2.4 | mJ |

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = 100 V, $R_G$ = 25 Ω, $V_{GS}$ = 20 → 0 V, L = 100 μH

**3.** $T_{ch}$ ≤ 125°C, $R_G$ = 25 Ω, $V_{DD}$ = 100 V



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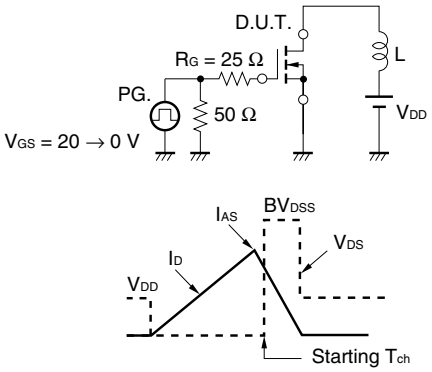
**The mark ★ shows major revised points.**

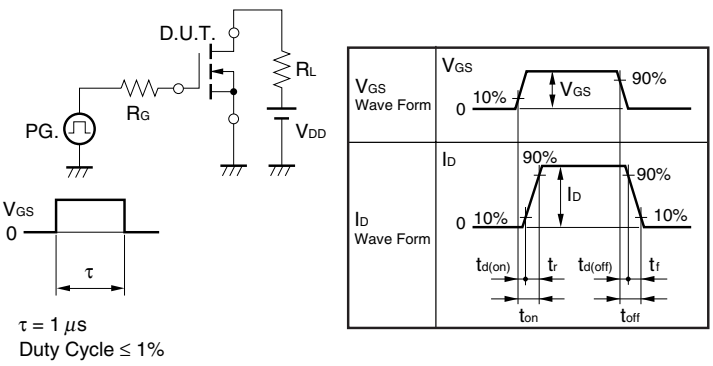
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 2.5 | 3.5 | 4.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 4.0 A | 3 | 5 | | S |
| Drain to Source On-state Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 4.0 A | | 0.34 | 0.43 | Ω |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 390 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 95 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 45 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 100 V, $I_D$ = 4.0 A | | 5 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 10 V | | 7 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 0 Ω | | 19 | | ns |
| Fall Time | $t_f$ | | | 6 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 160 V | | 12 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V | | 2 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 8.0 A | | 6 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 8 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 8 A, $V_{GS}$ = 0 V | | 110 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 360 | | nC |

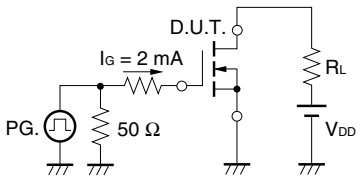
### TEST CIRCUIT 1 AVALANCHE CAPABILITY




### TEST CIRCUIT 2 SWITCHING TIME

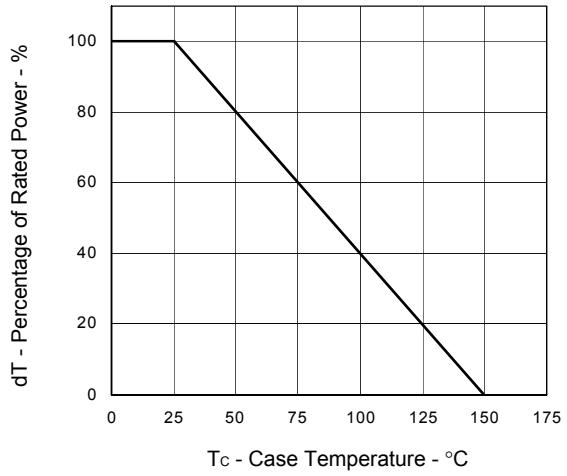



### TEST CIRCUIT 3 GATE CHARGE

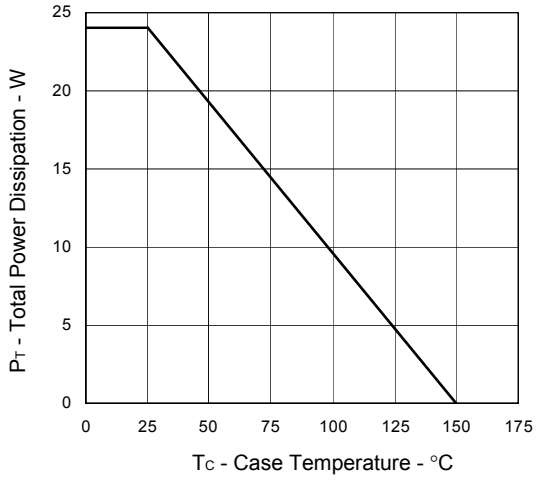


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

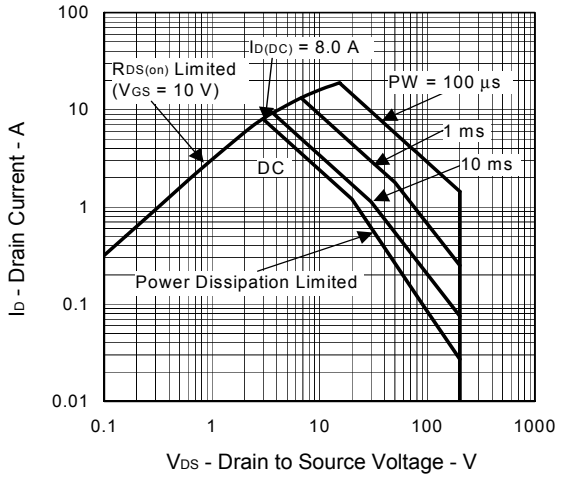
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



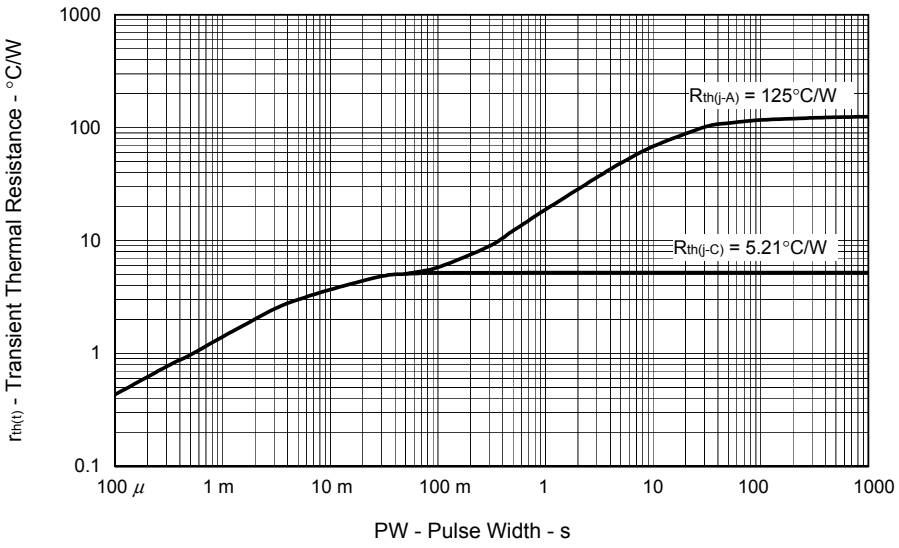

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



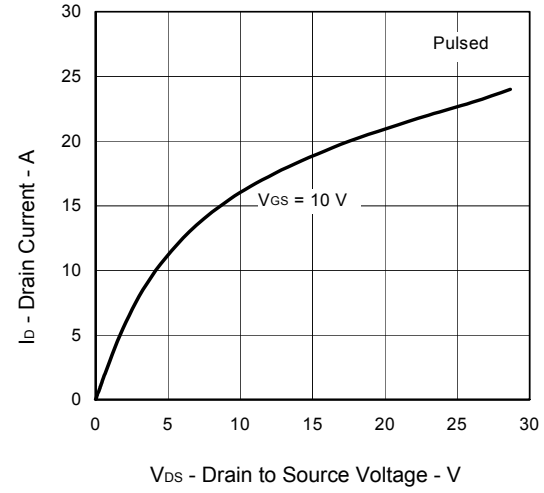

FORWARD BIAS SAFE OPERATING AREA



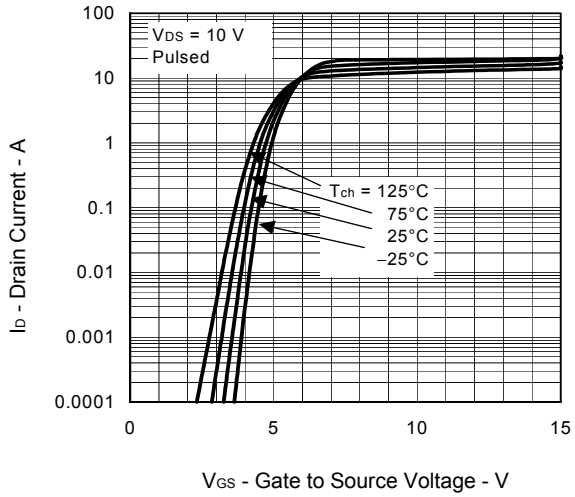

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



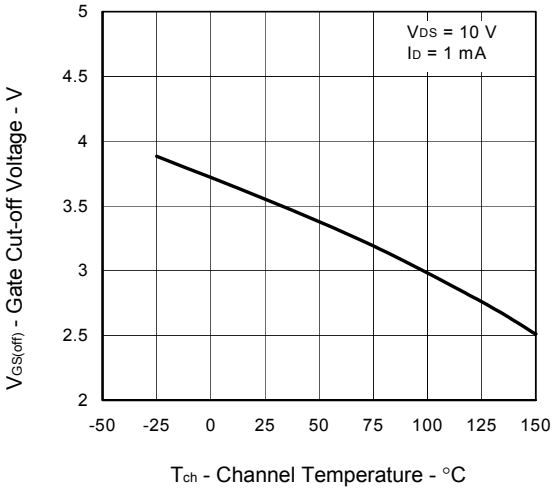
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



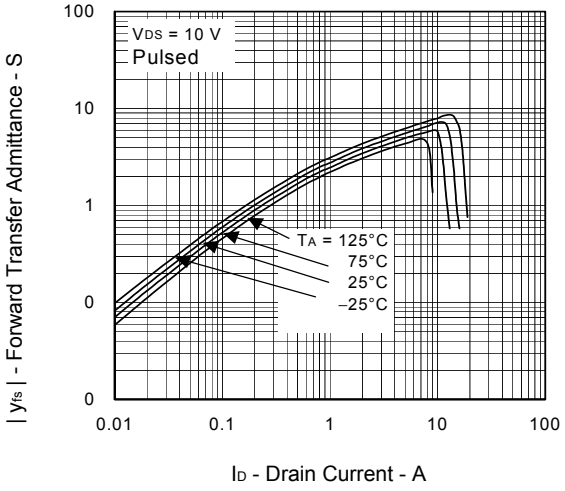

FORWARD TRANSFER CHARACTERISTICS



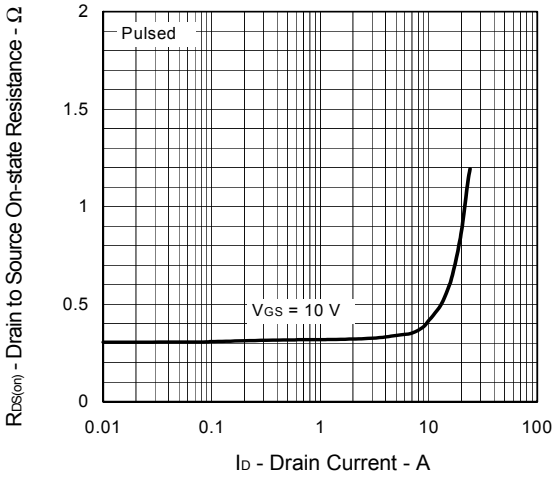

GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



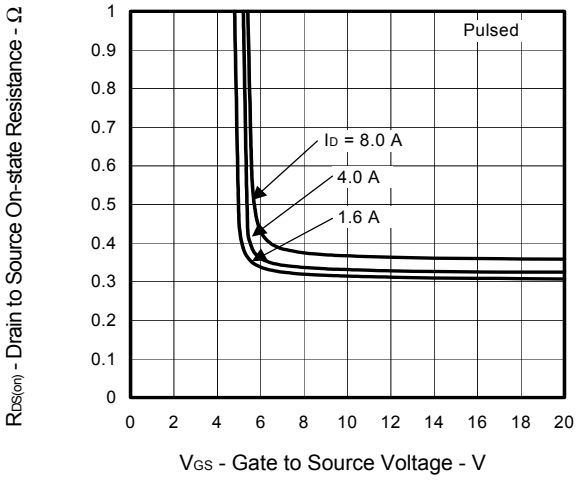

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



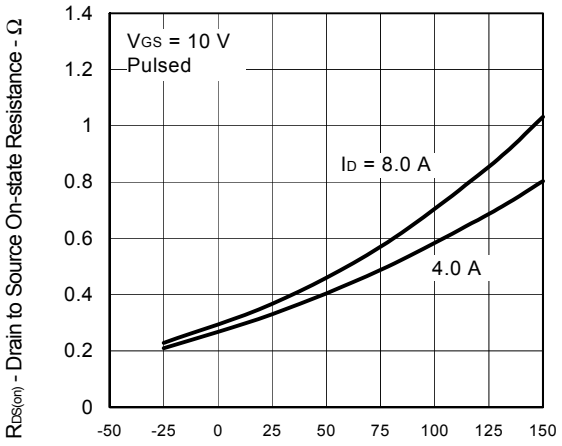

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



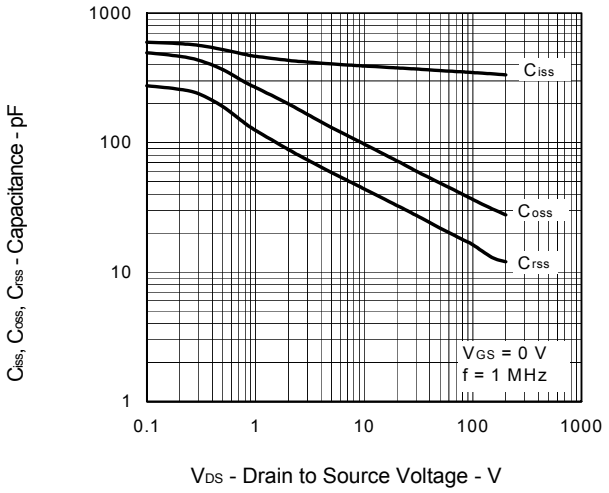

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



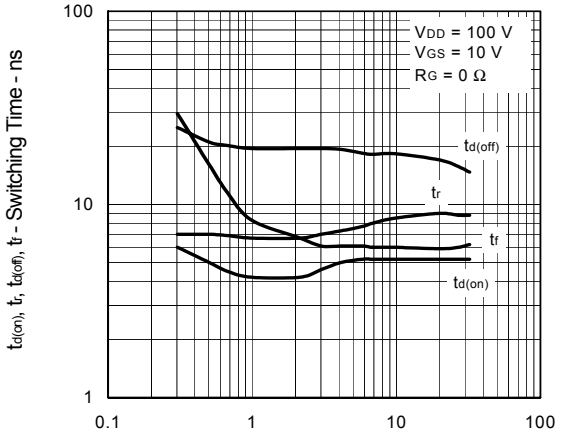
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



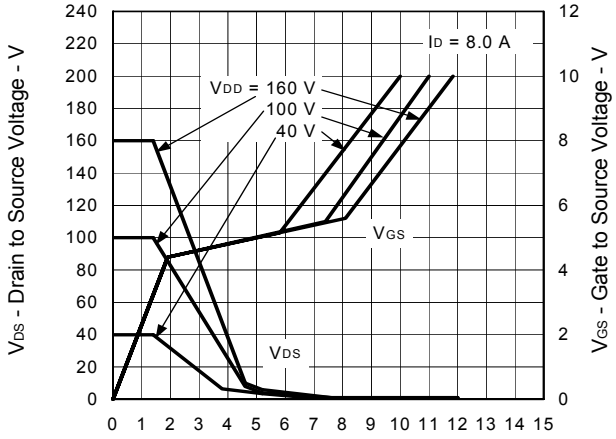

CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



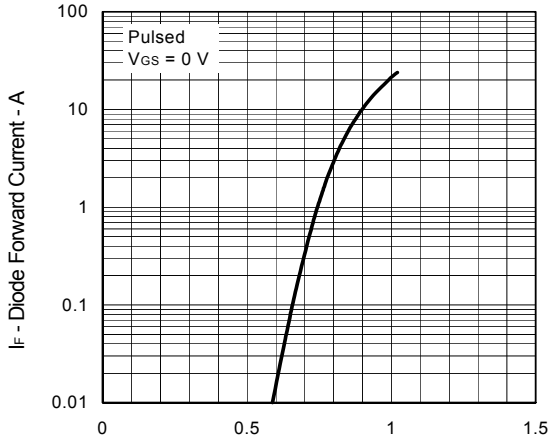

SWITCHING CHARACTERISTICS



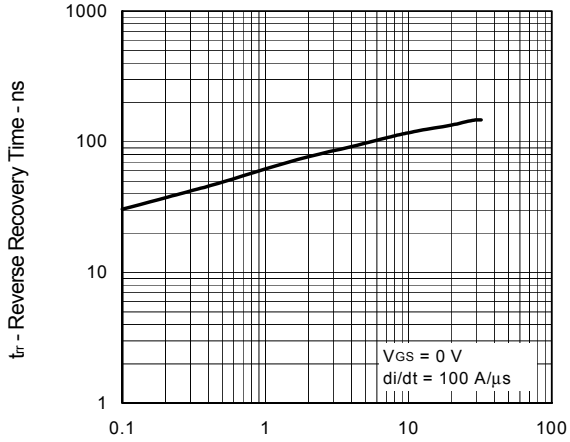

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



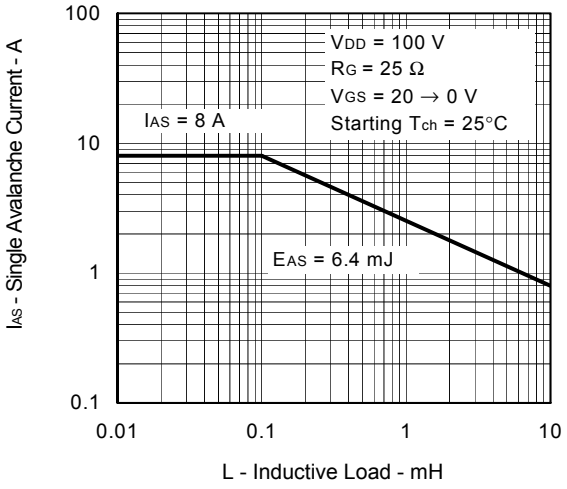

SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



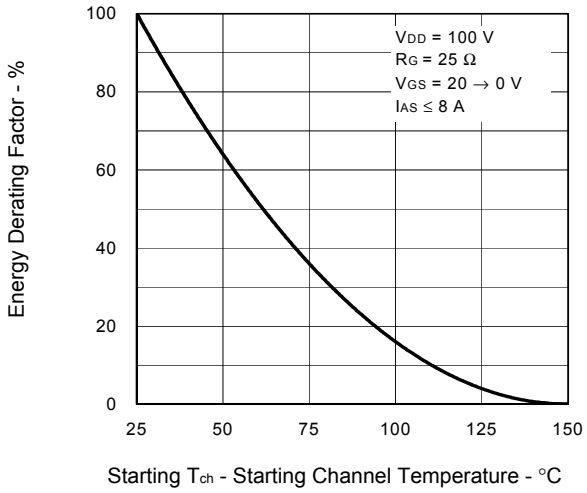

REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

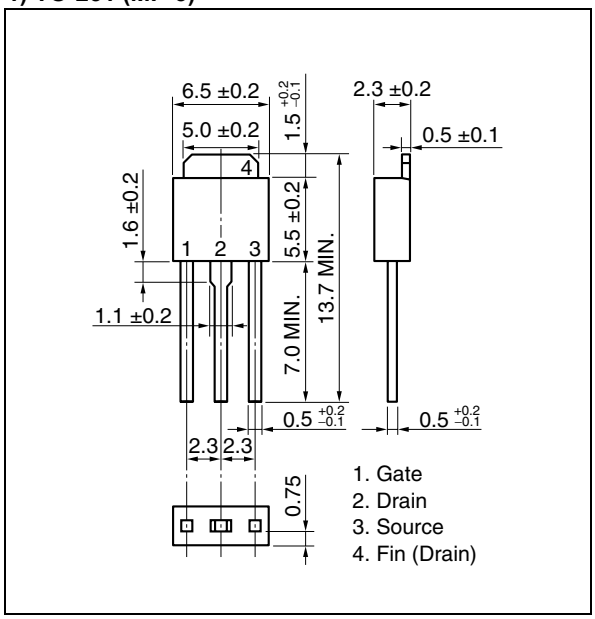



SINGLE AVALANCHE ENERGY DERATING FACTOR

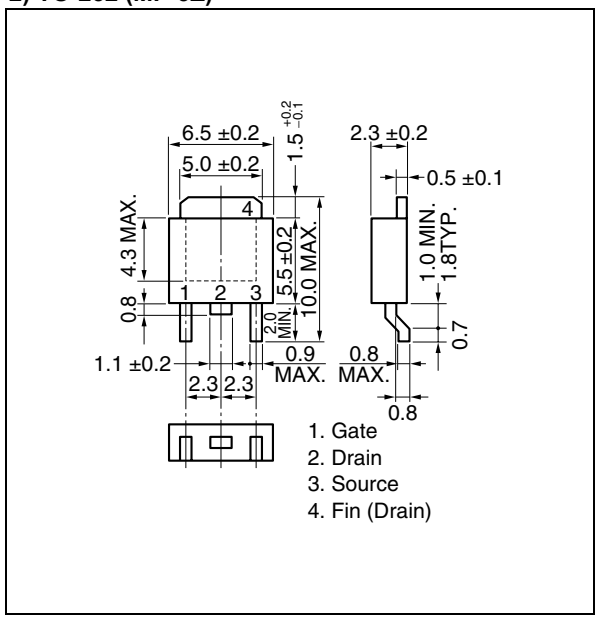


## ★ PACKAGE DRAWINGS (Unit: mm)

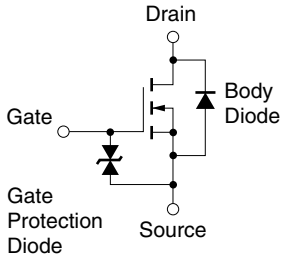
**1) TO-251 (MP-3)**




**2) TO-252 (MP-3Z)**




## EQUIVALENT CIRCUIT




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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